RDL and Interposer Design for DiRAM4 Interfaces

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***Abstract*—This paper presents results of signal integrity study conducted on two packaging designs: redistribution layer (RDL) for face-to-face stacking and 2.5D interposer for lateral connection of four processor chips with high performance memory die having a bandwidth of 4Tb/s .**

Keywords— RDL;Interposer; signal integrity;

I. INTRODUCTION

In today's high performance computing systems, interconnect speed and bandwidth between processor and memory present major constraint for optimal operation. A great deal of research work has been done to develop new technologies to alleviate this problem [1]. Two of the contemporary packaging technologies that are the subject of this paper are: face-to-face stacking using redistribution layer (RDL) as interface [2] and Interposer for side-by-side connection [3].

The scope of this study includes designing interconnect channel to link four processor chips with 3D Dis-integrated RAM (DiRAM) developed by Tezzaron. DiRAM is a high bandwidth memory formed by stacking wafers vertically using tungsten vias with very small diameter and fine pitch to allow more vertical interconnect per unit area.

DiRAM4 is a fourth generation DiRAM which contains 64 independent ports. Each of the four processor chips interface with 16 ports of DiRAM4. There are ~6400 signal pads on a DiRAM4 chip. The size of the DiRAM4 die is 12mm X 14mm, whereas each processor chip is sized to be 5mm X 5mm. The following sections deal with design, simulation and analysis of results for both RDL and interposer.

II. RDL FOR FACE-TO-FACE STACKING

The RDL serves as an interface between processor and DiRAM4 die as shown in Fig. 1. Signal pads on the DiRAM4 side have wider pitch compared to that of the processor. Therefore, the design process involves generating a wiring layout that will produce array of signal pads that match the processor's finer pad pitch.

The process of forming RDL on a DiRAM4 wafer involves a back end of line(BEOL) processing. In this study, a thin film polymer, Benzocyclobutene(BCB), was used as dielectric material due to its low dielectric constant(Er=2.65) which is desirable for high speed transmission of signals [4].

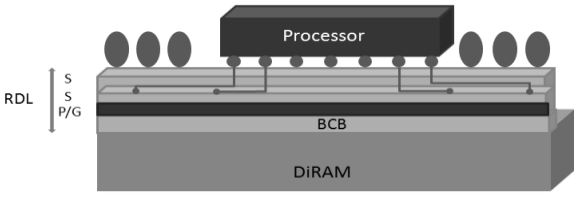


Fig.1. DiRAM and processor face-to-face connection through RDL

After RDL formation is complete, the DiRAM4 and processor chips are connected face-to-face through fine micro-bumps using chip-on-chip packaging technology[1][2]. The interconnect to the package is completed via larger solder bumps. This will avoid the usage of through-silicon-via (TSV) resulting in low cost packaging solution.

A. Design and Simulation of RDL for connecting four Processor chips with a DiRAM4 die

The RDL design assumes the four processor chips are placed at the center of the DiRAM4 die close to each other as shown in Fig 2. The wiring layout was implemented in two routing layers in such a way that the skew between signals is minimized. Width, thickness, interlayer dielectric height and minimum spacing of wires were all fixed at 1um to complete the routing within two signal layers.

After completion of the routing, the two dimensional layout of three adjacent wires including the longest wire, that is 3mm long, was imported into HFSS for 3D frequency domain simulation from 10MHz to 10GHz. Wire thickness and inter-layer dielectric height were set to be 1um to complete the 3D HFSS modeling.

Time domain simulation was performed using HSPICE based on the full-wave equivalent circuit exported from the HFSS tool. The conditions for the simulation were set as follows: VDD=1.0V, temperature = 90C, clock frequency = 2GHz and rise and fall time = 50ps. The parasitic capacitance at the input of the receiver pad was assumed to be at 0.5pF.

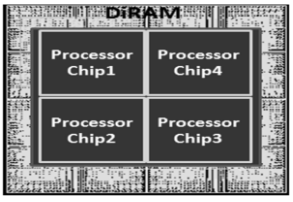


Fig. 2. Four processor chips on top of DiRAM

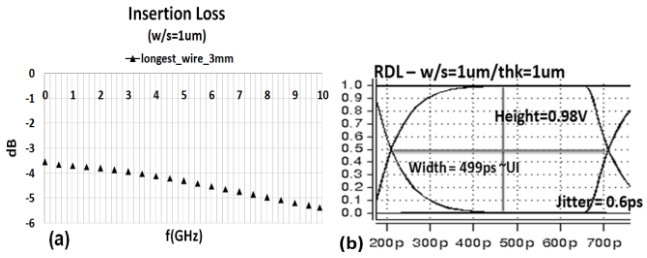


Fig 3. (a) RDL Insertion loss (b) RDL eye diagram

Both ends of the interconnect structure were terminated with 50Ω resistor to minimize reflection. An input signal consisting Pseudo Random Bit Sequence (PRBS) of 128 bits was driven into the interconnect channel to evaluate the channel's response. The delayed and attenuated waveform at the output of the channel was superimposed over a period to form the eye diagram.

B. Results and Analysis for RDL

The charts in Fig 3 summarize the frequency and time domain simulation results. Fig 3(a) indicates that insertion loss at 2GHz is ~4dB, which is only slightly worse than at low frequency suggesting the loss is mainly attributed to the resistance of the wire. As the frequency increases to 10GHz, the insertion loss gets worse due to elevated cross-talk noise and dielectric loss. The eye diagram in Fig. 3(b) demonstrates wide opening with minimal jitter.

III. INTERPOSER FOR LATERAL CONNECTION

The application of interposers for interconnecting processor chips with high bandwidth memory is viewed as a cost effective alternative to the System-on-chip (SOC) approach. In this packaging technology, the processor and memory chips are mounted face-down and side-by-side on the interposer as shown in Fig 4. Interconnect wires are routed in the interposer to link the signal pads of the two chips. Through-silicon-via (TSV) is used to complete the routing to the package [5] [6].

Interposers that are currently in production mainly use organic and silicon substrates. Organic interposers are widely available due to their reduced cost and relative ease of manufacturability. However, the poor dimensional stability and low I/O density will have a limitation on the usage of organic interposers for scaled-down technology nodes [7]. Silicon

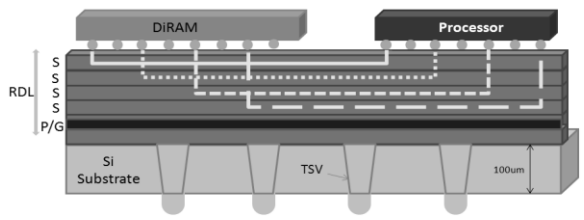


Fig. 4. DiRAM and Processor laterally connected through Interposer

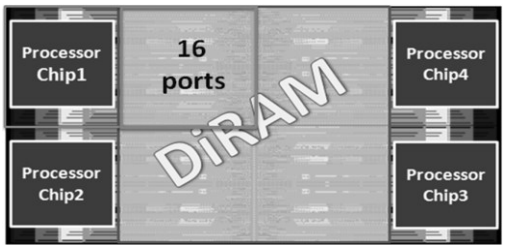


Fig.5. Four processor chips on opposite sides of the DiRAM

interposers on the other hand exhibit exceptional dimensional stability attaining very high IO density.

A. Design and Simulation of Interposer

In this study, a silicon interposer was designed to connect one of the processor chips with a quarter of the DiRAM4 die which contains 16 independent ports. Identical layout was applied to additional three processor chips to complete the interconnection of the entire DiRAM4 die with four processor chips positioned on opposite sides of the DiRAM4 as shown in Fig. 5.

The wires were laid out in a way to minimize skew between the longest and shortest wires as illustrated in Fig 4. As such, the arrangement of the signal pads in the processor and DiRAM4 were designed to be in such a pattern to allow the skew mitigation technique previously implemented by Kariyazaki et al. [6]. Using this approach, it became possible to contain the length of the wires within 8-10mm. Otherwise, the longest wires could reach over 14mm which would worsen the skew and insertion loss.

The design specification stipulates that only four signal layers were to be used for routing the wires with one additional layer for power and ground. Two different layer arrangements were considered during the analysis: GSSSS, where all four signal layers are stacked on top of the reference layer and SSGSS in which the reference layer is inserted between two signal layers above and below it. The thickness of the substrate material was set to be 100um as used in Lee et al's studies [5].

B. Results and Analysis

The charts in Fig 6 summarize the insertion loss for three different cases of width and spacing for the GSSSS layer ordering. The length of the wires for the top and bottom layers are 10mm and 8.5mm respectively. As shown in Fig. 6(a) and (b), increase in width and spacing from 1um to 3um leads to

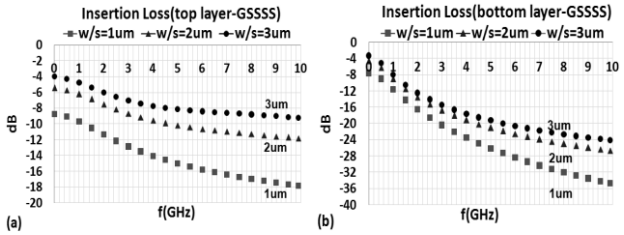
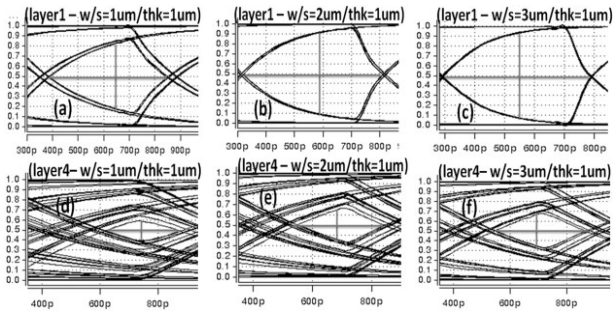


Fig 6. Insertion loss for GSSSS layer arrangement (a) top layer: w/s=1um,2um,3um (b) bottom layer: w/s=1um,2um,3um



Layer	wire width/spacing/thickness	Eye height	Eye width	Jitter
layer1(top)	1um/1um/1um	0.61V	0.91UI	0.08UI
	2um/2um/1um	0.81V	0.98UI	0.02UI
	3um/3um/1um	0.86V	0.99UI	0.01UI
layer4(bottom)	1um/1um/1um	0.2V	0.5UI	0.5UI
	2um/2um/1um	0.32V	0.6UI	0.4UI
	3um/3um/1um	0.33V	0.63UI	0.37UI

Fig 7. Eye diagrams for GSSSS: top layer wire (a) w=s=1um (b) w=s=2um (c) w=s=3um bottom layer wire(d) w=s=1um (e) w=s=2um (f) w=s=3um

Significant reduction in insertion loss. This is attributed to improvement in conductive loss and cross-talk noise as a result of using wider wire and spacing respectively. However, the change from 2um to 3um produced minimal gain compared to change from 1um to 2um suggesting further increment in width of wire also increases the wire capacitance thereby offsetting the benefit of lower resistance. The other observation from the charts is the worsening of the insertion loss for wires routed in the bottom layer, adjacent to the reference plane, versus wires in the top layer. This is due to aggravated cross-talk and dielectric loss. Time domain simulation is performed at identical settings discussed in the RDL section. The best and worst case eye-diagrams for each width and spacing instance are summarized in Fig 7.

The other analysis done for the interposer includes insertion loss comparison for GSSSS and SSGSS layer orderings. The chart in Fig 8 shows slight improvement for SSGSS particularly at high frequencies. This is attributed to reduced cross-talk effect due to the insertion of ground plane between the signal layers.

The interposer design results analyzed so far suggest that further improvement is required. Therefore, additional simulation was conducted by increasing the wire and interlayer dielectric thickness from 1um to 2um. The frequency and time domain simulation results compiled in Fig. 9(a) and (b) indicate significant gain for the thicker layer suggesting tradeoffs can be made to attain the signal integrity goals of a design.

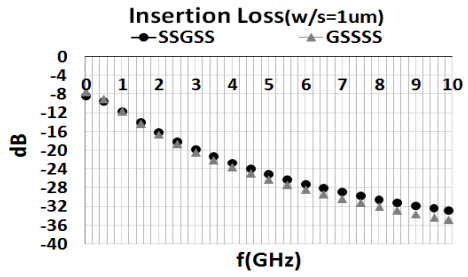
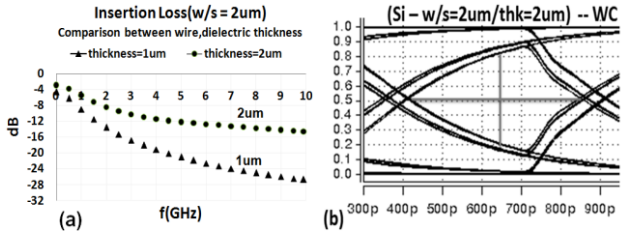


Fig 8. Insertion loss comparison for Si GSSSS, SSGSS



eyeHeight	eyeWidth	Jitter
0.6V	0.87UI	0.13UI

Fig 9. (a) Insertion loss comparison for 1um vs 2um thickness (b) Eye diagram

IV. CONCLUSION

In this study, RDL and interposer designs were considered for interconnecting processor chips with high performance memory. A comparative analysis of signal integrity was conducted in both frequency and time domain. The data indicate the RDL design produced better results than the interposer due to the fact that RDL uses shorter wires. However, it is demonstrated that the Interposer's performance can be improved by increasing the width, thickness and spacing of the wires as well as widening the thickness of the interlayer dielectric material. It was also shown that signal integrity of the interposer can further be enhanced by inserting ground plane between signal layers to minimize cross-talk. In the end, the choice of interconnect design requires careful examination of additional factors beyond signal integrity including reliability, cost, yield, and thermal and power integrity issues which are not discussed in this paper.

V. ACKNOWLEDGEMENT

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