Boosting Off-chip Interconnects through Power Line Communication

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***Abstract*—The number of available pins on SOC is one of the limiting factors to the off-chip bandwidth, for example many-core enabled Internet of Things (IoT) devices, where the package size and PCB floorplan are tightly constrained. A typical SOC package allocates more than half of the pins for power delivery, resulting in the number of IO pins for off-chip communications is greatly reduced. We observe the requirement for the number of power and ground (P/G) pins is driven by the highest performance state and the worst design corners, while SOC is in lower performance state for most of the time for longer battery life. Under observation, we propose to reuse some of the power pins as dynamic power/signal pins for off-chip data transmissions to increase the off-chip bandwidth during SOC low performance state. Our proposed method provides 30Gbps bandwidth per hybrid pair, while managing minimum impact to the original power delivery network (PDN) design.**

I. Introduction

The development of packaging and PCB technology (e.g. BGA/CSP) is slower than the speed of transistor size shrinking, which limits the performance for the off-chip bandwidth. For example, ball-to-ball pitch was 0.4mm in 28nm planar silicon technologies while it is only reduced to 0.35mm in 14nm FinFet [1], causing a competition for precious BGA resources between signal and power balls.

Commercial SoCs integrate CPU, GPU, memory, modem, ISP, and south bridge, including multiple voltage domains and performance modes. The number of power and ground (P/G) pins is designed for the highest performance state. Traditionally, all the system-level PDN designs and analysis are based on the highest performance mode or the worst-case, resulting in more than enough pins allocated for the normal mode. For example, In $Snapdragon^{TM}$ 410 [2], 55% out of 760 BGA balls are used for power delivery.

Researchers have been working on improving the off-chip bandwidth through 3D Package on Package (POP) and power transmission line [3], [4], [5]. Recently, Chen *et al.* proposed to switchable pins [6]. The implementation requires four external switches per switchable pin and greatly increases the PCB layout complexity. Power line communication (PLC) was proposed in [7], which is a hybrid power and signal pin method to serve for power delivery and signal communication depending on the performance state.

In this paper, PLC on an industrial SOC BGA ballmap is studied with on-die parasitics capacitance of the switches included in the model. The contributions of our paper are as follows. 1. The performance of a PLC model using the industrial PDN model is investigated. 2. The parasitic capacitance of the power gating switches is studied in the model. 3. Receiver channel equalization is utilized to improve signal integrity. 4. The noise immunity of PLC is investigated.

II. Design Overview

The proposed PLC reuses some power pins of core voltage rails for data communications in low performance state, leaving only a few dedicated power pins connected to the on-die power grid to meet the PDN requirement. The design target for PLC is to have the least modifications on the existing layout, while minimizing the coupling noise of data communication and power delivery noise, and maximizing the eye diagram and bit rate for data transmission.

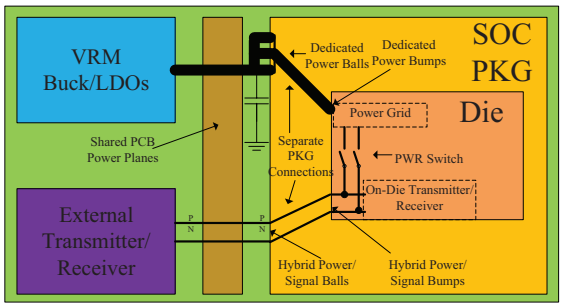


Fig. 1. High-level overview of the proposed PLC on PDN.

Figure 1 illustrates the high-level diagram of proposed PLC. There are four main components, including voltage regulator module (VRM), SOC, off-chip driver/receiver and decoupling capacitors. The VRM provides voltage for the SOC rails. Off-chip drivers/receivers communicate to SOC die through differential hybrid ball/bump pairs. As data communication and power delivery share the same conductor on PCB, we propose to use differential signaling, i.e. two pins for each channel, to minimize the noise to the dedicated power pins. The common mode voltage of the differential pair is set to the corresponding nominal voltage of the power plane. With the design challenge of the data communications of differential pairs and power delivery share the common conductors, some PDN margins are compensated for better eye diagram.

The package design requires a layout modification to support PLC, where separate connections are made for the dedicated power bumps and balls and the hybrid ones. The detailed package implementation for PLC can be found in [7]. With the dedicated traces for each hybrid bump/ball pair, the differential signals can pass through packages with less attenuation. However, the additional void area on the power plane increase the parasitic inductance and resistance of PDN.

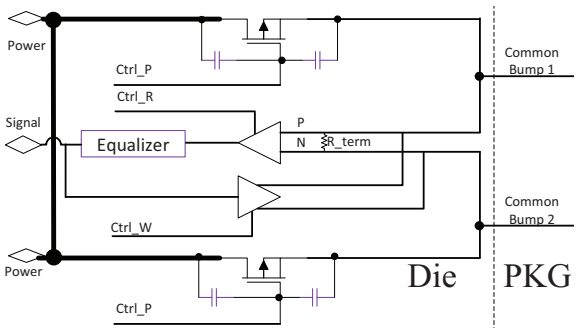


Fig. 2. The circuit diagram of a on-die differential signal-to-power switch

A. On-Die Implementation

Figure 2 depicts the on-die circuitry for a differential hybrid power/signal pair. Two power transistors are needed for each pair to switch between signal mode and power mode. There are two operation modes for the hybrid pins. In signal mode, the on-die switches are turned off and the hybrid pins are used for signaling. In power mode, the switches are turned on and the hybrid pins are connected to the main power grid. The R_{dson} of the switch can be as low as 1.8mΩ [6].

Different from [7], the impact of parasitic capacitance (C_{gs}, C_{gd}, C_{bs} and C_{bd}) of switch is considered as the main limiting factor for the eye height of signal mode as the drain of switches is shorted to power grid. While total parasitic C can be reduced by decreasing the size of transistors, R_{dson} increases which weakens the function of hybrid pins during power mode.

Our studies show that by adding series resistors on gate of the switches can minimize the impact of the gate capacitance. However, the capacitance between source and drain of the switch cannot be compensated by series resistors, which is translated to DC resistance in power mode.

A Continuous-Time Linear Equalizer (CTLE) is added to improve the eye diagram of the receiver. The performance of the CTLE will be discussed in the next session.

B. PCB Implementation

Figure 3 shows a four layer PCB layout for PLC. The top and bottom layers are solid ground planes. The off-chip driver/receiver (P1-P4) with two channels and a 14x14mm SOC are located on Layer 1. In center top left region, there are 7x7 P/G balls in checkerboard pattern allocated for a single power domain to minimize the loop inductance. Among them, four leftmost power pins are for two pairs of hybrid power pins for PLC, which connects to the SOC package balls, while the rest balls are defined as dedicated power pins for noise observations. The port definition for S-parameter model is highlighted on Layer 1. All the following simulations follow this port definition. Layer 3 is allocated for signal transmission and Layer 2 is defined as the power plane.

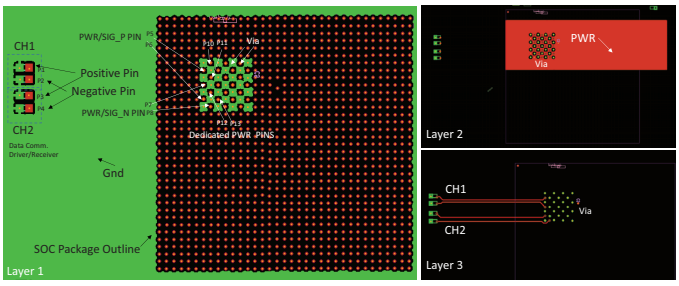


Fig. 3. An overview of the 4-layer PCB test coupon layout for PLC.

When the off-chip driver sends out the differential signal from P1 and P2 for CH1, signal first travels through a Layer 1 to 3 via to the trace on Layer 3. The differential traces are loosely coupled on Layer 3 and the trace width is set to 100ohms of Z_{diff}. The main power plane stays on Layer 3. The differential signal traces and power plane are connected together through micro-vias from Layer 2 to 3. P5, P6, P7, P8 and other dedicated power pins are connected to the power plane through micro-vias from Layer 1 to 2. Therefore, P1 and P2, P5 and P6 are the PCB to package interfaces of the PLC between off-chip driver and SOC for CH1. VRM (P9)is not shown in the figure. To improve SI for data communication, layout modifications are needed to on layer 2 to isolated the current loop for dedicated and hybrid power pins, which will be discussed in the next section.

III. PCB Model Optimization

PCB power plane optimization for PLC is discussed in this section. The goal is to maximize the magnitude and bandwidth of differential forward voltage gain (S_{dd21}) from P1-P2, to P5-P6 for CH1 (from P3-P4, to P7-P8 for CH2) on PCB. Our layout studies are based on Expedition, Siwave and HFSS 2015, Sigrity 16.61 and ADS 2013.12. An Intel Xeon W3550 PC with 20GB DRAM is used for extractions and simulations.

The relation of S_{dd21} and the additional notches between two hybrid pins has been analyzed in [7]. In this paper, we observe that the beauty of checkerboard pattern between P/G balls can naturally create the needed notches for PLC. By decreasing the via connections to the power plane for the hybrid pins, the bandwidth and peak of S_{dd21} can be greatly increased as shown in Figure 4. Eq 1 shows the expressions of the frequency for the peak S_{dd21}. The peak magnitude of S_{dd21} is proportional to $1/C$, where C is parasitic capacitance of the two pins.

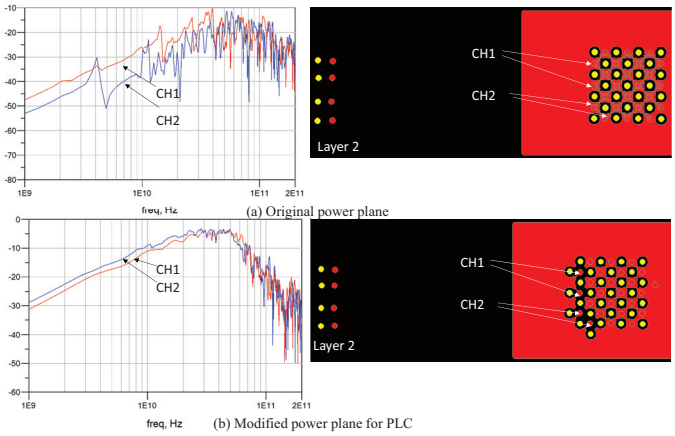


Fig. 4. S_{dd21} of two channels from the original and the modified power plane.

$$f_{peak} = \frac{c}{\sqrt{\epsilon_r}} \frac{1}{D} \tag{1}$$

where c is the speed of light, $\epsilon_r = 4.4$ is PCB dielectric, and D is electrical distance between two hybrid pins.

IV. Case Study: A Complete Power Delivery and Data Communication Path

The effect of the on-die circuit to the performance of hybrid pins in signal mode is discussed in this section. Firstly, we demonstrate PLC on a complete PDN from PCB, package to die by investigating the eye diagram for pseudo-random binary sequence (PRBS) bit streams during the signal mode. The noise immunity of PLC is analyzed. Secondly, the impedance profile of the complete PDN path with PLC in power mode is demonstrated. The PCB model is in Figure 4(b). The package and die models are applied from the previous work [7].

A. Eye Diagram for Signal Mode

Figure 5 illustrates the schematic of the data path for one hybrid pair. PRBS is generated by the off-chip driver and connected to PCB through Port 1 and 2. Manchester code is used for self clock recovery. Port 5 and 6 are defined as PCB

interfaces to hybrid pins to the package model. Port 10 to 13 are the dedicated power pins. Port 9 is connected with a local PCB decap with 2.2uF to represent a typical output capacitor of VRM for CPU/GPU rails. By looking into S_{dd21} (from off-chip driver to SOC) of the combined PCB/PKG/die circuitry model, we determine 30Gbps as the bit rate for PLC.

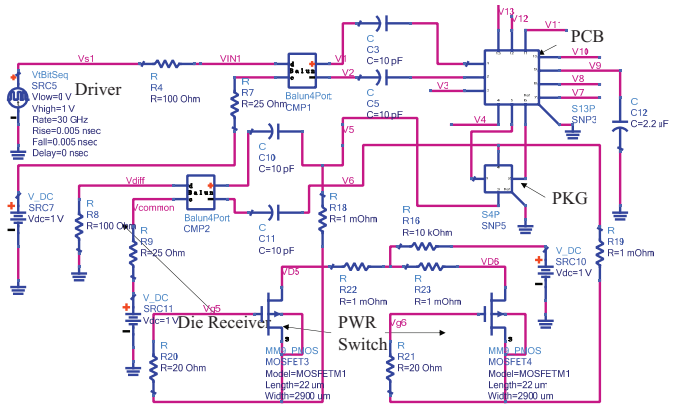


Fig. 5. Schematic for data communication on a PDN

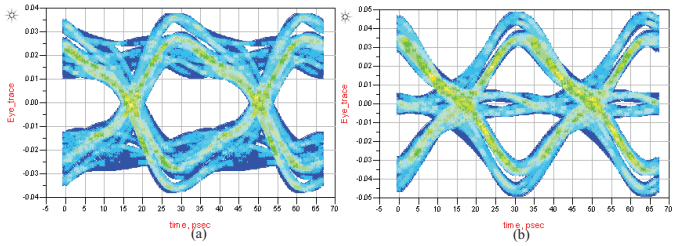


Fig. 6. Eye diagram of a 30GHz PLC (a) without equalizer, (b)with equalizer.

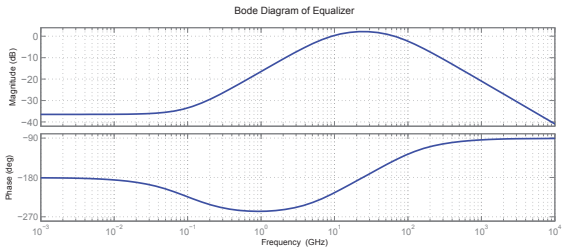
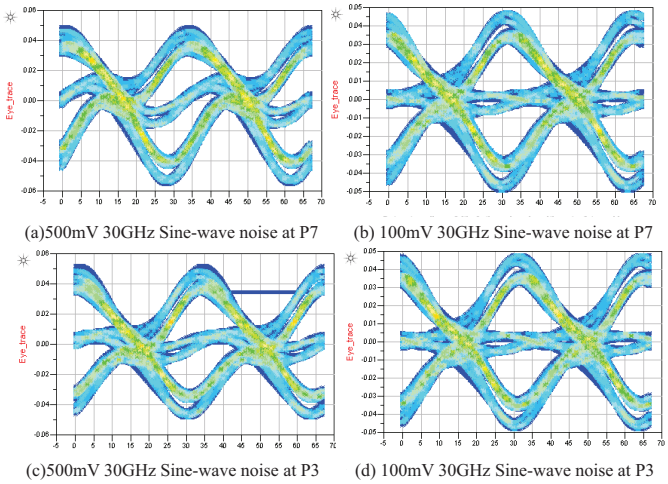


Fig. 7. The transfer function of the receiver equalizer.

Figure 6(a) shows the eye diagram of the signal received at the die level without or with the equalizer. Compared to the previous results in [7], the eye height is only 1/20th of the original results after considering the parasitics capacitance of the power switches from source to drain, because the drain of switches is short to the main power grid on the die level.

After investigating the transfer function of the channel, we designed CTLE as shown in Figure 7 to improve the eye diagram. Figure 6(b) shows that the eye height was recovered three times larger.

The noise immunity of PLC is also investigated by injecting two noise sources at P3 (far-end) and P7 (near-end) individually. The noise source is a sine-wave at 30GHz with an amplitude of 100mV or 500mV. Figure 8 shows that PLC is immune from most of the noise sources on power plane and a near end noise can be barely observed at 500mV amplitude due to P/N phase skew.



(a)500mV 30GHz Sine-wave noise at P7 (b) 100mV 30GHz Sine-wave noise at P7

(c)500mV 30GHz Sine-wave noise at P3 (d) 100mV 30GHz Sine-wave noise at P3

Fig. 8. Receiver eye diagram after equalization with near-end and far-end noise source from power plane.

B. PDN Analysis for Power Mode

The PDN during high performance mode is studied when all the hybrid pins turn on the power switches to connect with the dedicated power pins. The PDN simulation setup can be referred from [7]. Figure 9 shows the impedance profile of the original and modified PDN for PLC. The PDN degradation is contributed by PCB and package, as a $5m\Omega$ higher impedance peak at the lowest frequency resonance is observed.

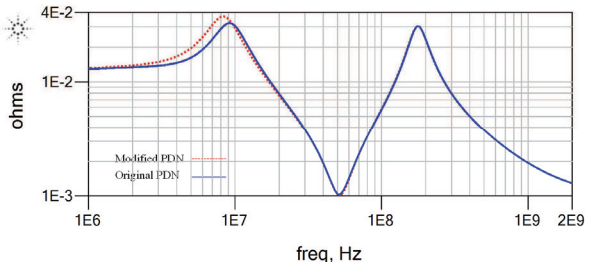


Fig. 9. Impedance profile for the original and the modified PDN with one pair of PLC

V. Conclusion

A 30Gbps bandwidth PLC on a SOC PDN design with on-die equalization is proposed. The proposed architecture can greatly improve the off-chip bandwidth, while preserving the PDN performance. Our future work will focus on the further optimization of the on-die circuitry to minimize the impact from the parasitic capacitance of the power switches.

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