Electrical Modeling and Analysis of 3D Neuromorphic IC with Monolithic Inter-tier Vias

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***Abstract*—Neuromorphic computing is an emerging computing technology which utilizes very-large-scale integration (VLSI) technology to mimic neuro-biological architectures present in the nervous system. It promises the realization of parallel computing with extremely low power consumption. To fully take advantage of this computing technology, its scalability and complexity need to be extended beyond its current two dimensional (2D) CMOS fabrication and package technology. In this paper, a three dimensional integrated circuit (3D-IC) technology, which employs Monolithic Inter-tier Via (MIV) and memristor, is proposed to further miniaturize the system and reduce the power consumption. In this work, the building block of the 3D-IC is modeled. In addition, the impact of the crosstalk between the memristor and the MIV is discussed**

Keywords—Neuromorphic Computing; 3D-IC; Crossbar Structure; Memristor; Signal Integrity; Monolithic 3D-IC

I. INTRODUCTION

Since the proposition of the von Neumann architecture in 1945, the computer based upon this architecture has advanced enormously to serve the computational needs. Because of its separation of the center process unit (CPU) from the memory, the data must travel between CPU and memory during the computing. When more computational horsepower is in demand and the data rate increases, this architecture becomes less efficient, particularly the data transfer between the CPU and the memory inevitably becomes a bottleneck. To overcome the difficulties and limitations inherited from the von Neumann architecture, a new computer architecture needs to be developed.

On contrast to the von Neumann architecture, the super computer such as a human brain integrates the CPU with the memory seamlessly, which significantly eliminates the data travel overhead imposed.

Neuromorphic computing, proposed by Mead[1], mimics human brain's architecture by using VLSI technology. In recent years, several successful researches have been conducted. Their hardware implementations are listed in Table 1. Although they were very impressive, their hardware implementations are not comparable to the human brain in term of neuron density, power density, network connection complexity, and so on.

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In Table 1, each neuron in human brain connects to more than 10,000 other neurons. The same parameter is 244 in TrueNorth chip, and 222 in HICANN chip. Moreover, to achieve same neuron number level, we need approximate 10,000 TrueNorth chips, which would be 4.3 m^2.

Table 1: Comparison of Power Density, Neuron Density, Synapse Density, and Neuron Connection Degree

	TrueNorth [2]	Neurogrid[3]	HICANN chip/ BrainScaleS[4]	Human Brain[5]
Neuron number	1,048,576	65,535	511	20Billions
Synapse number	256 millions	N/A	113,636	200 Trillions
Area/volume	430 mm^2	168 mm^2	50 mm^2	1130 cm^3
Neuron Density	2438.55 per mm^2	390 per mm^2	10 per mm^2	17,699 per mm^3
Synapses Density	0.595 million per mm^2	N/A	2272 per mm^2	177 million per mm^3
Ratio of synapses to neurons	244	N/A	222	10,000
Power density	0.15 mW/ mm^2	18 mW/ mm^2	57 mW/ mm^2	0.0177 mW/ mm^3

Two major preordained drawbacks in 2D IC implementation of the Neuromorphic IC such as long transfer distance between the neurons and a large area for synapse make it incompetent comparing to the human brain pertinent to neuron density, synapse density, power efficiency and neuron network complexity. In order to overcome the limitations imposed by 2D IC technology, [6] proposed the application of 3D-IC technology and Nano-scale memristor. 3D-IC offers the third dimension interconnections between neurons. The total connections length can be reduced by 3x [7]. Also, 3D-IC technology reduces the chip area by 35%, and lowers power consumption by 50% [8]. Memristor is a new two terminal nonvolatile device [9]. Its conductance can be gradually modified by controlling charge or flux through it, which is similar to the biological function of synapse. Memristor can reduce the size of synapse to Nano scale. Moreover, as a nonvolatile device, it does not need power to maintain the weight value.

II. 3D NEUROMORPHIC IC WITH MIVS

In order to design a 3-D neuromorphic IC, stacking a crossbar is a viable strategy to achieve larger array size and shorter RC delay comparing to vertical RRAM structure [10]. But the pitch dictated by the formation of nanowire crossbar is as small as 400 nm for TSVs with radius of 1um to directly connect or go through [6]-[11]. On the contrast, a new 3D-IC

integration technology such as "Monolithic 3D-IC" can stack two or more tiers sequentially, rather than bonding two independently fabricated dies together using bumps and/or TSVs. Due to the benefit offered by the small size of the Monolithic Intertiers Vias (MIVs), which can be 100 nm or smaller in diameter [12] , we propose a 3D memristor-based crossbar stacking structure using MIVs, as illustrated in Figure 1. In this implementation, the synapse crossbar in different CMOS neuron layers can be feasibly interconnected through MIVs.

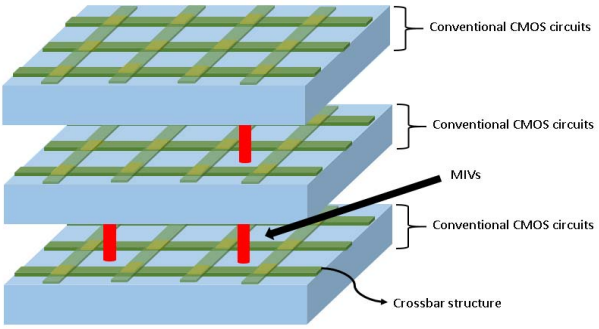

Figure 1:3D-IC Neuromorphic Structure using MIVs

In order to achieve large scale neuromorphic system and highly parallel computing ability, the number of MIVs between two neuron layers can be thousands in parallel. At a relative high operating frequency (2GHz [2]), the signal integrity of the building block consisting of MIVs and a crossbar need to be accurately modeled and analyzed.

III. Q3D Extracter and Spice Hybrid Model

For the purpose of analyzing the signal integrity of this new structure, a SPICE hybrid model with the assistance of Q3D extractor is built. A neuron spiking model [13] shown in Figure 6 is used as a voltage stimulus source in SPICE simulations. An equivalent circuit model for two MIVs with the presence of the crossbar is proposed and is illustrated in Figure 4 while the equivalent circuit considered for two MIVs adjacent to a crossbar is presented in

Figure *5*. Two MIVs are placed in the middle of 60 nm adjacent pitch crossbar [14]. The frequency band considered in the simulation is from DC to 2GHz. The memristor crossbar is designated as a floating net in Q3D model. The material of MIVs is copper while the Nano wire connecting memristor is modeled as platinum. Identical to [9], TiO2 is used for memristor material and an oxygen reduced state (TiO1.5) is used as a switching "on" state. The electrical properties of TiO1.5 are presented in Table 2. The resistance, inductance, and capacitance matrixes are extracted and imported to SPICE [15] [16] for building hybrid models as shown in Figure 4 and 5.

Table 2: Electrical Properties of TiO1.5

Memristor Material	TE-BE	Relative Permittivity	Relative Permeability	Bulk Conductivity	Dielectric Loss Tangent
TiO1.5	Pt-Pt	4.85[17]	1	35 (Ωcm)[18]	0[17]

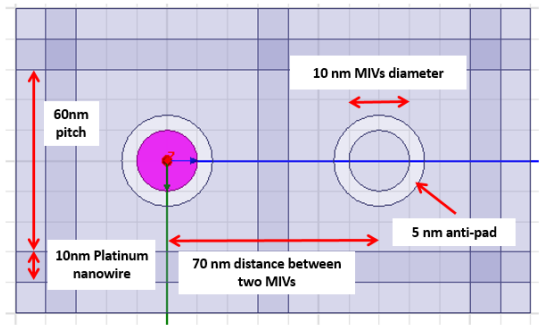

Figure 2: Top View of Q3D Extractor Model of Integration between MIVs and Memristor-based Crossbar Structure

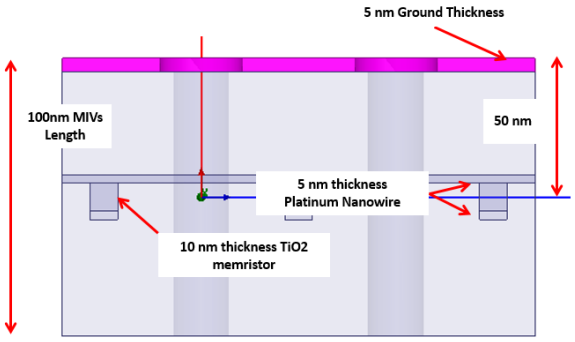

Figure 3: Side View of Q3D Extractor Model of Integration between MIVs and Memristor-based Crossbar Structure

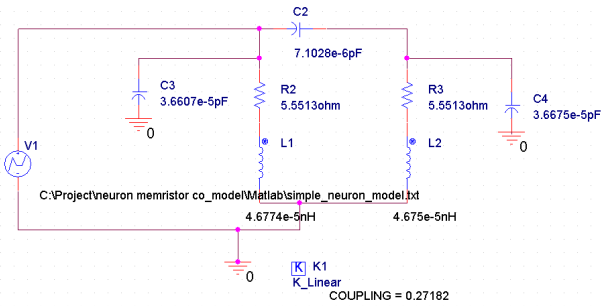

Figure 4: Two Simple MIVs SPICE Model

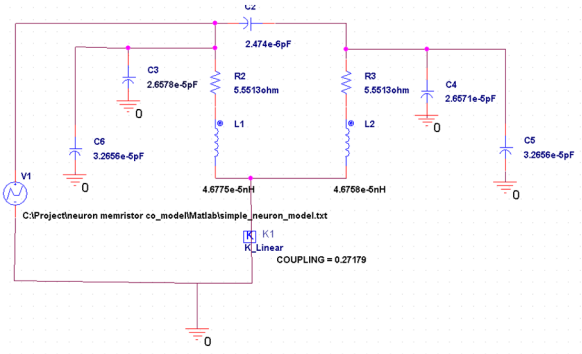

Figure 5: Two MIVs SPICE Model with One Layer Memristor

IV. Result and Discussion

The simulation results show the memristor crossbar capacitance with respect to the ground plane is 3.26E-6 pF. The crossbar structure acting as a bridge between two MIVs offer a new coupling path between two MIVs and it consequently changes the mutual capacitance between two MIVs. More peculiarly, the presence of the crossbar reduces the mutual capacitance of two MIVs from 7.10E-6 pF to 2.74E-6 pF, which potentially could reduce the direct coupling between MIVs.

A time domain SPICE simulation is performed. The result with no crossbar influence is shown in Figure 6. A coupling current noise signal in a victim MIV is induced by spiking stimulus rising and falling edge. After adding a memristor crossbar structure between two MIVs as shown in Figure 3. The coupling current is reduced as expected, which is shown in Figure 7.

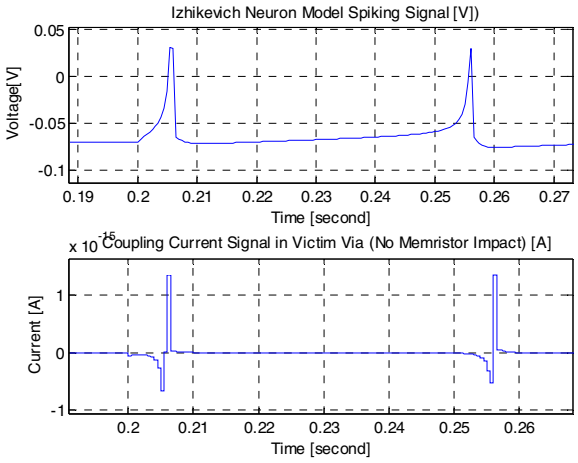

Figure 6: Spiking Stimulus Signal Waveform and its Current Coupling Signal Waveform on Victim MIV

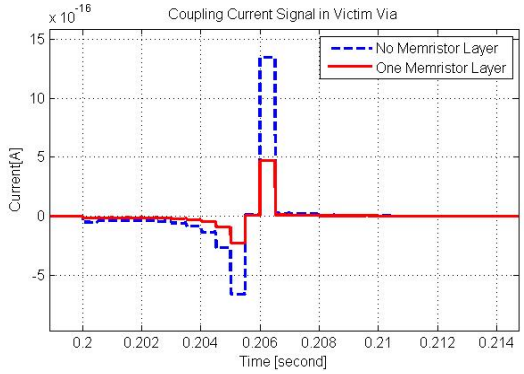

Figure 7: Comparison of Current Coupling Signal Waveform Victim MIV between No Memristor and One Memristor Case

The application of 3D-IC and memristor crossbar structure in a neuromorphic IC design has a high potential for achieving large scale neuron system and reducing computing power consumption at the same time. However embedding crossbar structures provides a new coupling path between MIVs, which need carefully modeled and analyzed.

V. References

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