Guard Band Reduction Via Dynamic Voltage Sensing and Reference Setting Schemes in Power Gated Applications

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***Abstract*—Use of power gates for leakage power reduction comes at the expense of higher DC and AC load lines due to location of voltage regulator sense point before the power gate and choice reference voltage to guarantee minimum voltage across all power gate and load conditions. This paper proposes schemes to dynamically change both the sense voltage and the reference voltage to reduce AC & DC load lines and consequently voltage guard bands. The simultaneous choice in sense and reference centers the load voltage variation between different gated domains providing an optimal solution without increase in maximum voltages. Application to client microprocessors show a benefit of a few tens of milli-Volts.**

Keywords—voltage sensing; voltage regulator; load line; voltage guard band; power integrity

I. Introduction

Due proliferation of circuits and shrinking CMOS process nodes [1] leakage current is now a significant part of the total current consumption. To limit power loss due to leakage, power gates (PGs) are therefore ubiquitous in digital and analog systems. Commonly, several circuits are powered from a single voltage regulator (VR) and PGs are used to power individual circuits on a need basis. In these applications the VR feedback sense point is chosen at a location before the PGs and adequate decoupling [2] is added before the power gates to de-sensitize the control loop dynamics to the different power gating scenarios. This choice has the following drawbacks: larger DC voltage variation (DC load line) at the load point and therefore larger voltage guard bands to ensure a required minimum voltage; larger droops due to transients on gated domains; and higher capacitor cost and more conservative loop design.

This paper proposes schemes that dynamically change both sense voltage feedback & the VR reference voltage to overcome the above shortcomings and result in reduced DC load line & transient droops. The schemes cover: change in sense location and reference voltage based on PG states in a single gated load case; sense voltage determination as a simple or weighted average between domains and reference voltage choice to ensure required minimum voltage; and transition sequence between power states changes. Clear benefits of DC voltage guard band (GB) reduction due to effective compensation of resistive drop, and lower AC GB reduction due to compensation of gated domain parasitics and more optimal loop design for different power states are shown. Importantly, the benefits come without addition of passive components or increase in the maximum load voltages. Application examples for client CPU cores show benefit of several tens of mV reduction. The concepts presented here are part of a patent application made by the authors.

The rest of the paper is organized as follows. The standard scheme and its drawbacks are described in Section II. Section III and IV describe the proposed schemes for single and multiple gated domains, respectively. Section V includes transient results, Section VI transition schemes followed by conclusions in Section VII.

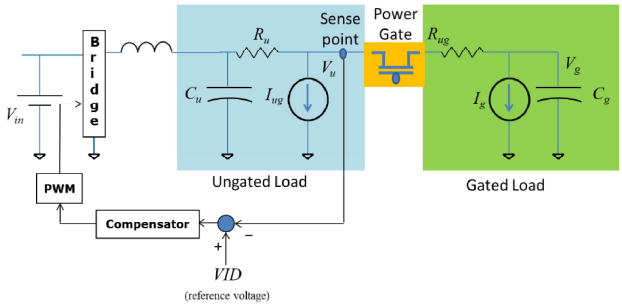

Fig. 1. Standard sense scheme.

II. Standard Scheme and Drawbacks

Fig. 1 shows the schematic of an application with ungated (always powered) circuits and gated circuits. The gated load is infrequently powered and the scheme saves power by reducing leakage in the gated circuits for the time that it is not powered. The VR sense point location is chosen before the PGs. The VR voltage reference or *VID* is set to the minimum voltage required for the gated circuits plus the DC voltage drop expected across the PG at maximum current. The gated side sees a larger DC voltage variation since the DC load line is increased by resistance R_{ug}, which represents sum of PG and parasitic resistance to the gated load. Furthermore, transients on the gated domain are not accurately reflected in the sensed voltage due to filtering leading to larger voltage droops.

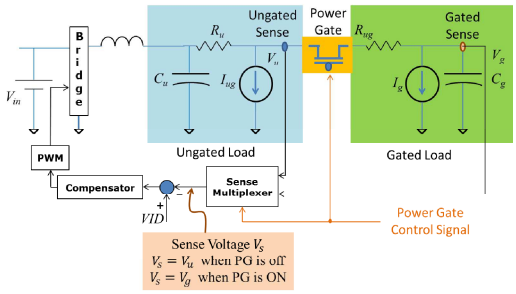

Fig. 2. Sense & reference scheme for one gated domain.

III. Single Gated Domain Scheme

We start with the scheme shown in Fig. 2 for a single gated domain. It entails a change in sense location and VID based on PG state. The power gate signal is utilized to multiplex the sense voltage fed back to the VR. While a buck type regulator is shown the same principles apply for any other type of voltage regulator—switched capacitor or linear regulator.

The scheme mitigates the DC load line (DCLL) [2] for the gated load by effectively mitigating the DCLL contribution from resistance R_{ug} by a factor ($1+GH_{DC}$), where GH_{DC} is the DC loop gain of the VR.

$$DCLL = \frac{R_u}{1+GH_{DC}} + R_{ug} \rightarrow \frac{R_u+R_{ug}}{1+GH_{DC}} \quad (1)$$

$$\Delta_{DCLL} = R_{ug}\left(1-\frac{1}{1+GH_{DC}}\right) \cong R_{ug} \text{ for } |\mathrm{GH_{DC}}| \gg 1 \quad (2)$$

In an example CPU core this scheme provides a DCLL reduction of a few mΩ. For illustration, a 2 mΩ DCLL reduction with a current of 20A reduces the DC GB by 40 mV, which can be utilized for some combination of power and performance benefit. In addition, if the VR has fast loop response it can partially compensate for voltage droop due to impedance between the gated and ungated domains. Transient performance is addressed in Section V.

The sense voltage multiplexing can be achieved in several ways. For an integrated circuit (IC) supplied by a motherboard voltage regulator a sense point output from the IC can be introduced. The output would provide feedback to VR after multiplexing sense signals coming from the gated and ungated loads using knowledge of power gate state. Alternatively, two sense signals could be fed back to the VR along with power gating information to accomplish the multiplexing in the VR.

IV. Multiple Gated Domains

A. Scheme for Two Gated Domains

Fig. 3 shows the two gated domain application with the proposed scheme. The sense voltage is determined as the average of all the gated domains drawing current. In addition the reference voltage is changed as described below.

The case of one gated domain ON is similar to that described in the last Section. With both gated domains power gated ON the sense voltage is determined as $V_s=(V_{g1}+V_{g2})/2$. Assuming the VR dc loop gain is high enough we have:

$$V_u = V_{g1} + \Delta_1 = V_{g2} + \Delta_2; \text{ and } V_s = \frac{V_{g1}+V_{g2}}{2} = VID \quad (3)$$

$$V_{g1} = VID + \frac{\Delta_2-\Delta_1}{2} \begin{cases} \min: VID - \frac{\Delta}{2} \\ \max: VID + \frac{\Delta}{2} \end{cases} \quad (4)$$

$$V_{g2} = VID + \frac{\Delta_1-\Delta_2}{2} \quad (5)$$

$$V_u = VID + \frac{\Delta_1+\Delta_2}{2} \quad (6)$$

where,

$$\Delta_1 = I_{g1}R_{ug1}, \Delta_2 = I_{g2}R_{ug2}, \Delta = \max(\Delta_1,\Delta_2) \quad (7)$$

Now, to guarantee a minimum voltage V^*, we can set $VID = V^* + \Delta/2$. In scheme of Fig. 1 where the sense voltage is fixed to V_u, to guarantee V_{g1}, $V_{g2} > V^*$ we had to set $VID = V^* + \Delta$. Thus, the proposed scheme reduces the DC voltage guard band by $\Delta/2$. Detailed comparison of nominal, minimum & maximum DC voltages are included in Table 1.

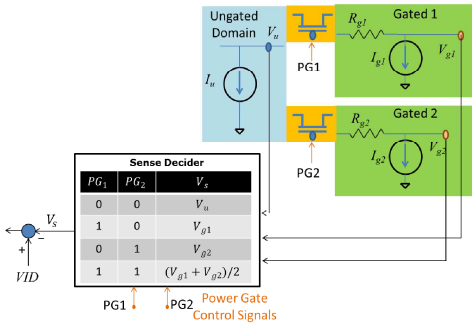

Fig. 3. Scheme for two gated domains.

Existing Solution					Proposed Solution				
PG1	0	1	0	1	PG1	0	1	0	1
PG2	0	0	1	1	PG2	0	0	1	1
Vs	Vu	Vu	Vu	Vu	Vs	Vu	Vg1	Vg2	(Vg1+Vg2)/2
Vu	Vu*	V*+Δ	V*+Δ	V*+Δ	Vu	Vu*	V*+Δ1	V*+Δ2	V*+Δ/2+(Δ1+Δ2)/2
Vu(Min)	Vu*	V*+Δ	V*+Δ	V*+Δ	Vu(Min)	Vu*	V*	V*	V*+Δ/2
Vu(Max)	Vu*	V*+Δ	V*+Δ	V*+Δ	Vu(Max)	Vu*	V*+Δ	V*+Δ	V*+3Δ/2
Vg1	NA	V*+Δ-Δ1	NA	V*+Δ-Δ1	Vg1	NA	V*	NA	V*+Δ/2-(Δ1-Δ2)/2
Vg1(Min)	NA	V*	NA	V*	Vg1(Min)	NA	V*	NA	V*
Vg1(Max)	NA	V*+Δ	NA	V*+Δ	Vg1(Max)	NA	V*	NA	V*+Δ
Vg2	NA	NA	V*+Δ-Δ2	V*+Δ-Δ2	Vg2	NA	NA	V*	V*+Δ/2-(Δ2-Δ1)/2
Vg2(Min)	NA	NA	V*	V*	Vg2(Min)	NA	NA	V*	V*
Vg2(Max)	NA	NA	V*+Δ	V*+Δ	Vg2(Max)	NA	NA	V*	V*+Δ
VID	Vu*	V*+Δ	V*+Δ	V*+Δ	VID	Vu*	max(V*,Vu*)	max(V*,Vu*)	max(V*+Δ/2,Vu*)

TABLE I. DC VOLTAGE COMPARISON BETWEEN PROPOSED AND STANDARD UNGATED SENSING.

B. Generalization to Arbitrary Number of Domains

The idea is generalized to multiple gated domains along with current weighted averaging to set the sense voltage as:

$$V_s = \sum_{k=0}^{n} \frac{PG_k I_k V_{g,k}}{PG_k I_k} \quad (8)$$

where, PG_k is the power gate state (1 for on and 0 for off), I_k is the current of the k^{th} gated domain, and $k = 0$ refers to the ungated domain. Weighting by domain current provides further improvement by factoring in domain activity. The scheme reduces to the two gated domains scenario above by equating I_1 & I_2 and ignoring the current draw on the ungated domain. The reference voltage choice for the generalized case is omitted here due to space constraints.

V. Transient Performance

Changing the sense point to the gated domain captures the dynamics of the parasitics, decoupling, and the load in the gated domain. Fig. 4 shows a representative transient droop [3] benefit simulated for a client CPU with two gated domains, which can be power gated independently. Several benefits are evident from Fig. 4.

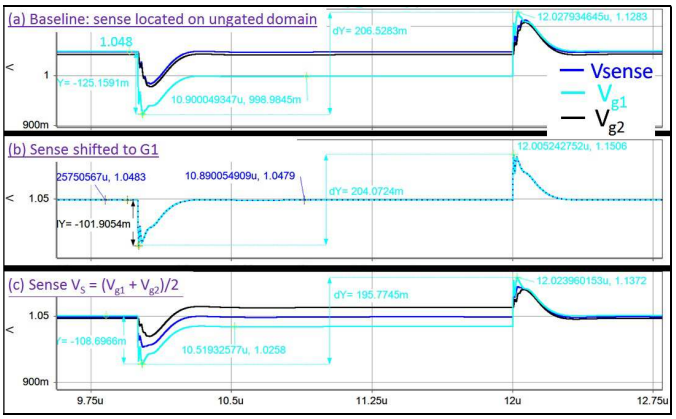

Fig. 4. Transient performance comparison for the two gated domain case with G1 experiencing a load increase at 10µs and decrease at 12µs. G2 is ON for (a) & (c) but OFF for (b).

Comparing Fig. 4(b) with Fig. 4(a) the G1 DC voltage is regulated to 1.05V (50mV improvement), its droop is reduced by 23mV, the maximum voltage with overshoot upon load release is almost the same, and (V_{max} - V_{min}) is the same for G1. Comparing Fig. 4(c) & 4(a) the G1 DC voltage is regulated to 1.026V (28mV DC improvement), droop is reduced by 16mV, the maximum voltage upon load release is almost the same, and (V_{max} - V_{min}) is lower by 10mV.

In the single gated load ON scenario the combined benefit for DC and AC provides a total guard band reduction of 73mV without increase in V_{max} on any domain. In the two gated load ON scenario cumulative AC & DC guard band reduction is 42mV. Furthermore, changing the VR loop compensator element values with the power gate states to account for extra parasitics along with a change in the sense location will yield even better transient performance for the gated domains resulting in further guard band reduction.

VI. Transition Scheme

Fig. 5 shows the proposed sense voltage transition schemes for two power gated domains. The concept can be extended to higher number of gated domains. Signals PG1 & PG2 indicate which domains are gated ON. The changes in sense voltage V_s with transitions in PG1 and PG2 are indicated along with delays, as required. The basic idea is as follows.

When the number of domains being supplied increases, (e.g., {PG1, PG2}: {OFF, OFF} → {ON, OFF} or {OFF, ON} → {ON, ON}) the PG transition is allowed to complete (intervals t_1 & t_4) and only after that V_s is changed to reflect the new power gate states. This introduces latency (intervals t_2 & t_5) for the voltages to settle before the domains can reach their full activity level. However, these intervals are much smaller than latencies in typical power gate transitions.

When the number of domains being supplied decreases, (e.g., {PG1, PG2}: {ON, ON} → {ON, OFF}, etc.) the PG & V_s transitions are carried out simultaneously.

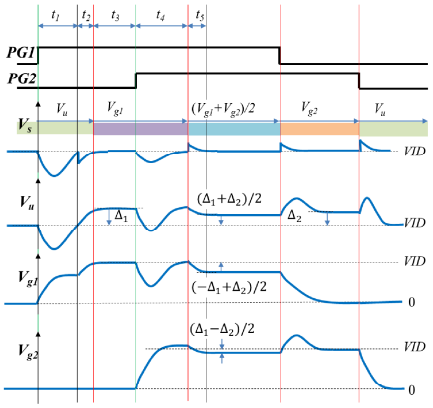

Fig. 5. Sense voltage transition scheme for two gated domains.

VII. Conclusion

The paper has presented schemes that change the sensed voltage and reference setting for voltage domains with several power gated loads. Single and two power gated domain cases have been analyzed in detail. Examples show benefit in voltage guard band reduction by several tens of mV due to DC voltage drop and transient voltage droops. Generalization of the approach to arbitrary number of domains along with current weighting for further benefit and transition schemes for power gate transitions have also been presented. Due to the resulting logic performance increase the proposed schemes enable the cheaper and simpler alternative of single voltage regulator gated power delivery as compared with more expensive fine grain distributed voltage regulator solutions.

References

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