Impact of Wafer-Bonding Defects on Monolithic 3D Integrated Circuits

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Abstract—**Monolithic three-dimensional (M3D) integration has the potential to achieve significantly higher device density compared to 3D integration based on through-silicon vias. We analyze defects that arise due to voids created during the wafer-bonding step in M3D integration. We quantify the impact of these defects on the threshold voltage of a top-layer transistor in an M3D integrated circuit. We also show that wafer-bonding defects can lead to a change in the resistance of inter-layer vias (ILVs), and in some cases, lead to an open in an ILV or a short between two ILVs. We then analyze the impact of these defects on path delays. Our results show that the timing characteristics of an M3D IC can be significantly altered due to the presence of wafer-bonding defects.**

Keywords*—*Monolithic 3D Integration, 3D Vias, Wafer Bonding.

I. Introduction

Monolithic 3D (M3D) integration is receiving considerable interest as it has the potential to achieve higher device density compared to TSV-based 3D stacking [1]. In this technology, transistors are processed layer-by-layer on the same wafer. Sequential integration of transistor layers enables high-density vertical interconnects, known as inter-layer vias (ILVs). Such high-density vertical interconnects can be achieved by fabricating the top-layer transistors on an extremely thin silicon substrate with thickness in the range of 10 nm [2]. In order to realize a thin silicon layer over the bottom layer without damaging the underlying interconnects and degrading the bottom-layer transistors, several layer-transfer techniques are being explored [2]. Low-temperature wafer bonding is a key processing step in these techniques.

In this paper, we analyze the impact of wafer-bonding defects on path delays in an M3D IC. We first understand the impact of bond defects on the threshold voltage of a top-layer transistor and on the ILVs. Our results show that the impact of wafer-bonding defects on the threshold voltage of a top-layer transistor is significant, and cannot be ignored, especially for M3D ICs integrated at the gate-level. We also show that the presence of defects at the bond interface can lead to a change in resistance of an ILV, and in some cases, lead to an open in the ILV or a short between two ILVs. These defects can significantly impact the slacks for paths through the top layer in a gate-level-integrated M3D IC.

II. Impact on Device Threshold Voltage

Defects during wafer bonding tend to occur at the bond interface. They can be attributed to air voids, delaminations (unbonded areas or voids), and foreign particles [3]. The size of these defects can be in the mm to nm range. Although the occurence of bond defects can be reduced by tightly controlling the above factors, it is not possible to completely prevent them due to increasing process variations at nanoscale technology nodes. It is especially difficult to control the occurence of nm size voids; they can easily form with a small variation in the surface roughness.

The presence of a void at the bond interface impacts the threshold voltage of top-layer transistors. The oxide layers, which act as the bond interface, form the inter-layer dielectric (ILD). For an M3D IC partitioned at the transistor level [2], the front-gate of a bottom-layer transistor acts as the back-gate for a top-layer transistor, and the ILD acts as the back-gate dielectric. Moreover, the front- and back-gates of a top-layer transistor will be connected to each other if all the standard cells are designed using static CMOS logic. Therefore, a top-layer transistor in an M3D IC partitioned at the transistor level can be regarded as a double-gate SOI transistor.

For an M3D IC partitioned at the gate level [2], a metal line (typically, the uppermost metal line) from the BEOL of the bottom layer acts as the back-gate for a top-layer transistor, and the ILD acts as the back-gate dielectric. Therefore, in this case, a top-layer transistor can be regarded as a double-gate SOI transistor in which the front- and back-gates are independent of each other.

If a void is present in the back-gate dielectric of a double-gate transistor, the back-gate capacitance will be lower compared to the defect-free case, since the dielectric constant of air is lower than that of a dielectric material such as SiO_2 or Al_2O_3. Let us consider a void that is perfectly aligned with the channel of a top-layer transistor as shown in Fig. 1. We assume a void in the shape of a ellipsoid of revolution (oblate spheroid) in accordance with the voids reported in the literature [4]. We also assume the diameter of the void to be greater than the channel length of the transistor under consideration but not large enough to affect transistors in other gates. This is a valid assumption since voids that impact transistors in multiple gates lead to catastrophic faults, and they can be easily detected. We are interested in analyzing the impact of voids that cause parametric faults.

With these assumptions, the effective back-gate dielectric capacitance can be expressed as the capacitance of the void in series with the capacitances of the di-

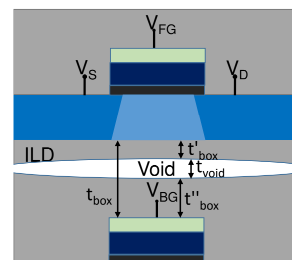

Fig. 1: Illustration of a defect in the back-gate dielectric of a top-layer transistor.

TABLE I: Threshold-voltage values of a double-gated device for transistor-level M3D integration

Channel Type	Defect-Free Case	Void Thickness				
		2.5 nm	5 nm	7.5 nm	10 nm	12.5 nm
P	-0.057 V	-0.052 V	-0.048 V	-0.039 V	-0.034 V	-0.030 V
N	0.090 V	0.063 V	0.054 V	0.040 V	0.027 V	0.020 V

electric layers above and below the void: $1/C_{effective} = t'_{box}/\epsilon_{ox} + t_{void}/\epsilon_{void} + t''_{box}/\epsilon_{ox}$, where t_{box} is the thickness of the back-gate dielectric in the absence of a void, t'_{box} and t''_{box} are the thicknesses of the dielectric layers above and below the void, respectively, t'_{void} is the thickness of the void, and ϵ_{ox} and ϵ_{air} are the dielectric constants of the ILD and void, respectively.

We carried out HSpice simulations using the LETI-UTSOI2.1 model to evaluate the impact of a void on the threshold voltage of a top-layer transistor [5]. The values of various parameters for the devices were obtained from [2]. We calibrated the model parameters using experimental values of on- and off-currents [2].

We obtained plots of the drain current (I_D) as a function of the front-gate voltage (V_{FG}) for double-gate transistors used to analyze transistor- and gate-level M3D for: (i) defect-free case, and (ii) a void in the back-gate dielectric. Here, we directly present the threshold-voltage values that we extracted from those curves. The threshold-voltage values are calculated using the constant-current threshold voltage extraction method for a drain-source bias of 100 mV.

Table I shows the threshold-voltage values of a double-gate transistor used to study the impact of a void on the threshold voltage of a top-layer transistor in transistor-level M3D integration. For the defect-free P-channel double-gate transistor, the threshold voltage was obtained to be -0.057 V. We observe a 5 mV increase from the threshold voltage of a defect-free double-gate transistor when the back-gate dielectric capacitance was modified to account for a 2.5 nm thick void. The change in threshold voltage increases to 27 mV when the simulation was carried out for a 12.5 nm thick void.

For the defect-free N-channel double-gate transistor, the threshold voltage was obtained to be 0.090 V. We observe a 27 mV decrease from the threshold voltage of a defect-free double-gate transistor when the back-gate dielectric capacitance was modified to account for a 2.5 nm thick void. The change in threshold voltage increases to 70 mV for a 12.5 nm thick void. Therefore, our results show that the presence of a void in the back-gate dielectric can have a notable impact on the threshold voltage of a top-layer transistor in an M3D IC partitioned at the transistor-level.

Table II shows the threshold-voltage values of a double-gate transistor used to study the impact of a void on the threshold voltage of a top-layer transistor in gate-level M3D integration. The threshold voltage of a conventional P-channel SOI transistor was obtained to be -0.062 V. For the defect-free P-channel double-gate transistor, the threshold voltage was obtained to be -0.139 V and -0.001 V for a back-gate voltage of 0 V and 1 V, respectively. We observe a 29 mV change from the threshold voltage of a defect-free double-gate transistor when the simulation was carried out for a back-gate voltage of 1 V and when the back-gate dielectric capacitance was modified to account for a 2.5 nm thick void. The change in threshold voltage increases to 85 mV for a 12.5 nm thick void. On the other hand, no change in the threshold voltage was observed due to a void in the back-gate dielectric for a back-gate voltage of 0 V.

The threshold voltage of a conventional N-channel SOI transistor was obtained to be 0.104 V. For the defect-free N-channel double-gate transistor, the threshold voltage was obtained to be 0.153 V and 0.051 V for a back-gate voltage of 0 V and 1 V, respectively. We observe a 25 mV change from the threshold voltage of a defect-free double-gate transistor when the simulation was carried out for a back-gate voltage of 0 V and when the back-gate dielectric capacitance was modified to account for a 2.5 nm thick void. The change in threshold voltage increases to 52 mV when the simulation was carried out for a 12.5 nm thick void. On the other hand, a very small change (3 mV) in the threshold voltage values was observed due to the presence of a void in the back-gate dielectric for a back-gate voltage of 1 V.

III. Impact on Inter-Layer Vias

We now analyze the impact of wafer-bonding defects on ILVs. In the M3D fabrication flow, ILVs are etched after the top-layer transistors have been processed. The ILVs are therefore processed along with the first metal layer of the top layer. The presence of a void in the dielectric at the position where an ILV is being etched impacts the electroplating process. To fill trenches and vias completely, without any voids or seams, a superconformal deposition of the barrier and seed layers is required [6]. However, if a void is present in the dielectric, superconformal deposition may or may not happen depending on the size of the void; thus, leading to the formation of voids or seams, and resulting in an increase in the resistance of the ILV. In some cases, the void can be large enough to cause an open defect in the ILV. On the other hand, if the size of the void is large enough to impact two neighboring ILVs, then it leads to a resistive short between the two ILVs. The resistance of the defect depends on the thickness of the void.

IV. Impact on Path Delays

We carry out HSpice simulations to analyze the impact of wafer-bonding defects on path delays. Fig. 2 shows the design on which we performed our analysis. We partition this design into two layers as shown in Fig. 2 in order to simulate gate-level design partitioning. For transistor-level design partitioning, all N-channel transistors are placed on the top layer and all the P-channel transistors are placed on the bottom layer. As shown in Fig. 2, constant DC voltages were applied to all the inputs, except on one input, on which a rising transition with a rise time of 5 ps was applied. The delay

TABLE II: Threshold-voltage values of a double-gated device for gate-level M3D integration

Channel Type	Conventional SOI	Back-Gate Voltage	Defect-Free Case	Void Thickness				
				2.5 nm	5 nm	7.5 nm	10 nm	12.5 nm
P	-0.062	0 V	-0.139 V	-0.139 V	-0.139 V	-0.139 V	-0.139 V	-0.139 V
N	0.104	0 V	0.153 V	0.128 V	0.115 V	0.108 V	0.104 V	0.101 V
P	-0.062	1 V	-0.001 V	-0.030 V	-0.055 V	-0.065 V	-0.075 V	-0.086 V
N	0.104	1 V	0.051 V	0.052 V	0.053 V	0.053 V	0.054 V	0.054 V

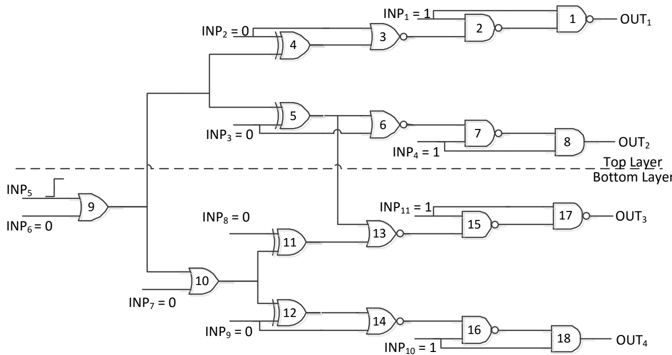

Fig. 2: Design used in Section IV.

in propagating this transition to the output nodes was calculated. We carry out simulations on 100 instances of the above design, created by randomly injecting defects on the gates in that design. In the case of transistor-level design partitioning, we inject four defects that include voids, which impact top-layer transistors (N-channel), and at the most one ILV defect. We only consider resistive opens and intra-cell shorts for the ILV defects. We do not consider inter-cell shorts as they are less likely to occur. The defect sizes considered for resistive opens (4 K-Ohm and 40 K-Ohm) and shorts (80 K-Ohm and 400 K-Ohm) were obtained from [7]. For gate-level partitioning, there are only two ILVs (highlighted in the figure), if we neglect the ILVs for routing the inputs and the power supplies from the top layer to the bottom layer. We inject four defects even in this case that include voids, which impact top-layer transistors, and at most one ILV defect (resistive open in one of the two ILVs or a resistive short between the two ILVs). We also assume that a void impacts a complete gate in gate-level design partitioning, i.e., we consider the same defect size for both N- and P-channel transistors in a gate.

Fig. 3(a) shows the propagation delay to the output nodes for transistor-level design partitioning. For each output, the delay in propagating the input transition to that node for the case in which no wafer-bonding defects were considered, and the case in which defects were considered, are shown in this figure. We observe that the path delays do not change significantly when ILV defects are not considered, i.e., only voids in the back-gate dielectric of a top-layer transistor are considered. This is expected as the impact of voids on the threshold-voltage of a top-layer transistor is not very significant. In addition, all the defects are not necessarily injected on the same path. However, for the instances in which all the defects were injected on the same path, or the instances in which ILV defects were considered, the impact on the path delays is notable. For a few instances, the ranking of the path delays is different from the case in which no wafer-bonding defects were considered. Nonetheless, the impact of wafer-bonding defects on the timing characteristics of a design partitioned at the transistor-level is not expected to be significant since paths in such designs contain large number of gates, and a small number of defects may not change the path profiles.

Fig. 3(b) shows the propagation delay to the output nodes for gate-level partitioning. For each output, the delay in propagating the input transition to that node for the case in which wafer-bonding defects were considered, and the conventional SOI case, are shown in this figure. For gate-level partitioning, we use the conventional SOI technology as the baseline as path delays can vary even in the defect-free gate-level design partitioning case due to variations in the back-gate voltage [8]. We observe that the change in path delays is notable even when ILV defects are not considered. This is expected as the impact of voids, in combination with variations in the back-gate voltage, on the threshold-voltage of a top-layer transistor is significant. Moreover, for the instances in which all the defects were injected on the same path, or the instances in which ILV defects were considered, the impact on path delays is significant. For these circuit instances, the ranking of the path delays can be different from the conventional SOI case. Therefore, wafer-bonding defects can cause a significant change in path delays.

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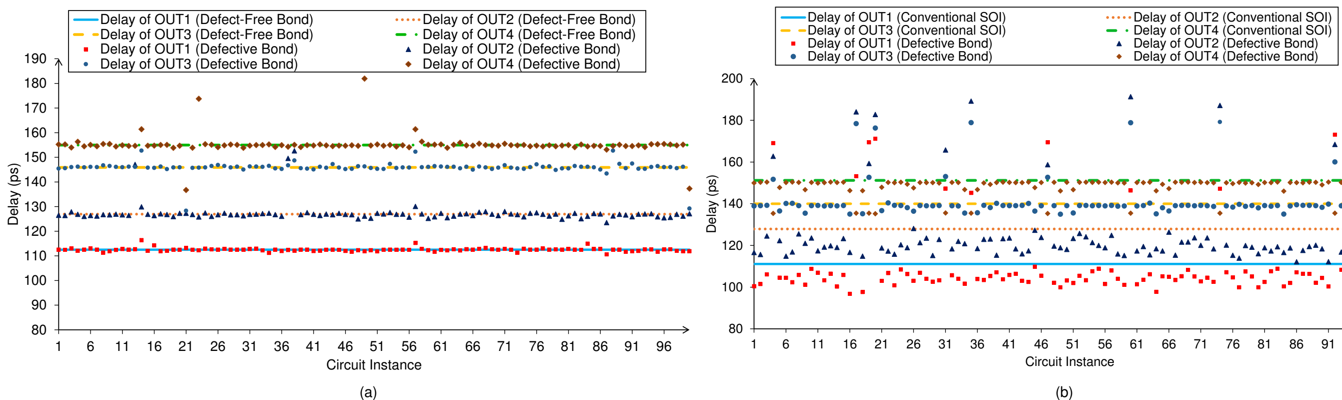

Fig. 3: Propagation delay of the transition to the output nodes for: (a) transistor-level M3D, and (b) gate-level M3D.