Techniques for detection of package issues in chip power integrity closure

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***Abstract*— Ever increasing need for better performance, die size reduction to aid cost saving and achieving schedule targets has challenged chip designers in multiple spaces. One such very important area is delivering required voltage to on die circuits through robust power grid. Designers have to make some tradeoffs to meet design requirements amid different constraints. Some of these tradeoffs if not well assessed can cause design failures. Through this write-up, we present assessment scheme which can bring out package power plane weaknesses by doing chip-package power delivery network (PDN) analysis.**

Keywords—power integrity;PDN; chip-package co-design

I. INTRODUCTION

Shrinking process geometries have allowed designers to add more functionality on the SoCs (System-On-Chips). Increasing device densities have resulted in higher power densities and thereby increase in current demands. Smaller geometries have also allowed supply voltage reduction. Supplying higher demand currents at stringent noise requirements, due to lower supply voltages, makes power network design challenging.

The goal of power delivery network is to provide good power supply to all the active devices on the die. Power delivery network must be assessed accurately considering all the different components of IR drop within the system. Traditional analysis techniques mainly focused on on-chip analysis while assuming fixed package parasitics (RLCG) for all the bumps on the die.

With the power supply voltage drop margins shrinking for each of the components in system, it is important to do a detailed analysis of each part of the system. This paper discusses traditional approach of PDN analysis and the gaps with that approach. We also discuss proposed method to identify package weaknesses and make the power delivery network robust.

II. TRADITIONAL APPROACH TO PDN ANALYSIS

Traditional PDN analysis was divided in two parts –

A. Chip level power integrity analysis

Chip level power integrity analysis focuses on on-die static/dynamic IR analysis, where a voltage source is defined at the chip bumps and current sinks are applied at different nodes based on power computed for each standard cell, to find out the voltage drop at each of the standard cell instance in the design.

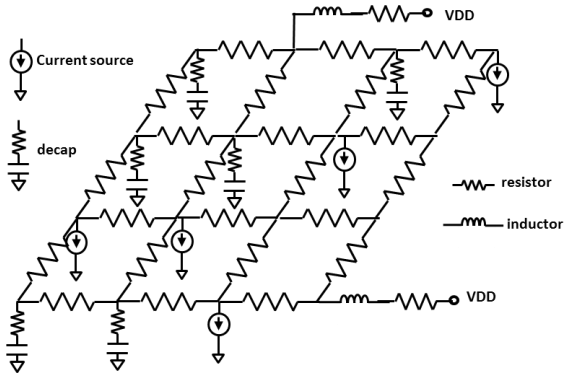

Fig. 1. Chip level power integrity analysis

Few technology nodes back, IR drop analysis was performed only at chip level ignoring package level IR drop. But with the voltages reducing and drop margins for each component shrinking, chip designers had been doing IR drop analysis including a lumped package model. Main objective of this analysis is to check if the power grid is able to supply required voltage to all the instances in the design.

Lumped package model could be either a two port RLCG or two port S parameters model. One port represented all the bumps on die side and the other port represented the BGA connections on the printed circuit board side.

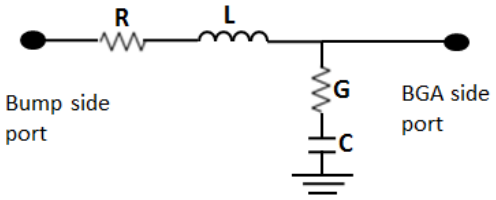

Fig. 2. Example 2 port RLCG model

B. System level Impedance analysis

This analysis simulates the complete system which includes the Voltage Regulator module (VRM), Printed Circuit Board

(PCB) model, IC package model and Rdie/Cdie model. Main objective of this analysis is to find out the impedance of the path from VRM to the die. This is often referred to as Impedance analysis. The magnitude of power noise or voltage ripples is proportional to the Impedance and transient current drawn from the chip. Efficient power delivery network has Z_{PDN} lower the system target impedance Z_{TARGET}. This analysis is used to estimate die, package and/or board level decap estimation.The Impedance analysis explained above is based on a lumped S parameter model of the package and PCB.

Lumped package model has same parasitics for all the bumps. Use of this model is perfectly alright where all the power bumps are very well connected to BGAs through package power planes.

III. LIMITATIONS OF TRADITIONAL APPROACH

Here we present a design challenge faced in one of the designs. Nearly half of the design perimeter was occupied by high speed serdes, DDR and analog IPs and rest of the half was available for other general purpose IOs as depicted in Fig. 3.

Right side of the die edge, the GPIO region, was filled with signal bumps associated with the GPIOs and their corresponding IO power and ground supply bumps. Due to bump placement strategy driven by chip level RDL routing and package level escape routing, there were no core power (VDD) bumps placement possible in this region, let's call it shadow region. This shadow region almost extended up to 1500uicro-meters into the core region from the die edge. Through co-design efforts, with bonding and packaging team designers were able to create some space in the IR drop hotspot regions to add few rows of VDD bumps (orange colored) as shown in Fig. 4.

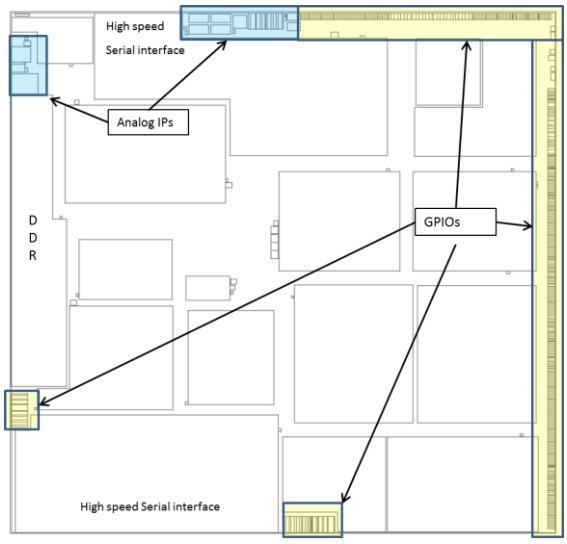

Fig. 3. Design floorplan

As mentioned earlier, initial IR drop analysis was performed with a lumped package model as represented by Fig. 2. Sign-off power analysis with lumped package model showed worst IR drop 0.5% less than the target voltage drop, meaning no IR drop violations. Worst IR drop reported was in the shadow region where number of core power bumps was less. Fig. 5 shows IR drop map using lumped package model.

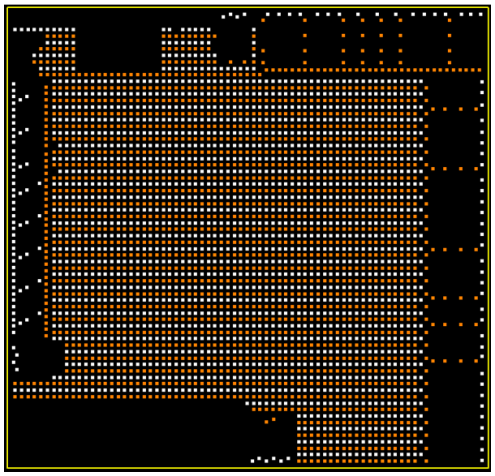

Fig. 4. Core power/Ground bump map

Package layout visual assessment revealed that connectivity of shadow region core power bumps was not very good due to their placement surrounded by signal bumps. These bumps were connected on top layer to the core region power plane with just a thin connection as highlighted in Fig. 6. It was clear that these bumps are certainly going to have higher parasitics compared with core region PG bumps.

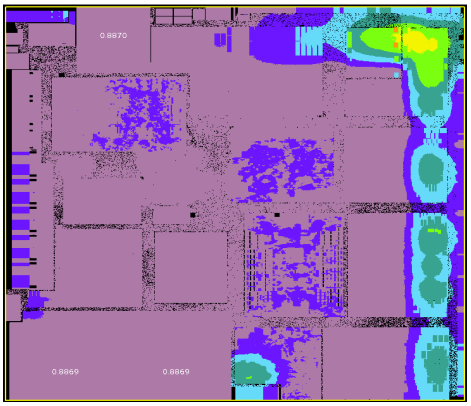

Fig. 5. IR drop map with lumped package model

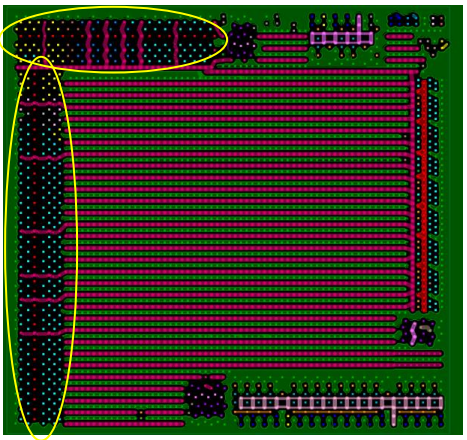

Fig. 6. Package Layout view : shadow region bumps connection

Lumped package models although are good for overall voltage drop analysis and system level impedance analysis of a particular design they are unable to bring out any package weaknesses. To bring out any package power plane connectivity issues, we need models with parasitics for every bump. We present this in the next section.

IV. Proposed Solution to Use Per Bump Parasitics

In the recent years, few full-wave package extraction solutions became available which claim to accurately extract package parasitics with per bump resolution [1][2]. These tools have ability to report package RLC values at bump level graphically as well as through detailed reports, allowing designers to quickly identify any package performance issues.

Fig. 7 shows inductance distribution for each bump in the device package. From the three dimensional graphical contours it was obvious that shadow region bumps had higher inductance relative to core region bumps.

In most designs, depending on the location of power/ground bumps and their connectivity to respective package planes, there would be few bumps which may have higher inductance relative to average. In this case it was due to shadow region bumps isolated from rest of the power plane. In some cases it may be acceptable to have higher inductance for few bumps if the current density is lower.

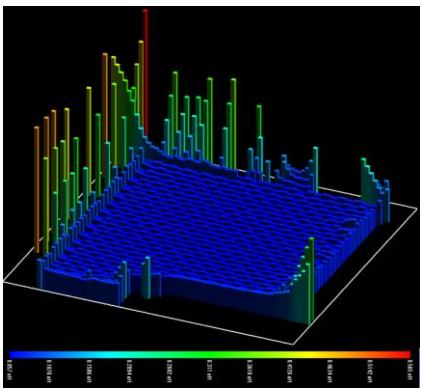

Fig. 7. Core VDD : per-bump package inductance distribution

It was important to assess IR drop with per-bump package model. Fig. 8 shows IR drop map using per-bump package model. It is evident from per-bump model based analysis, that lumped package model based analysis was optimistic and masked possible violations by shorting all bumps together.

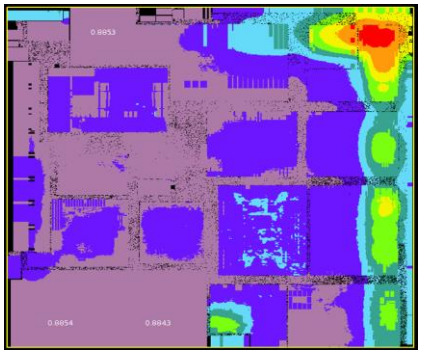

Fig. 8. IR drop map with per-bump package model

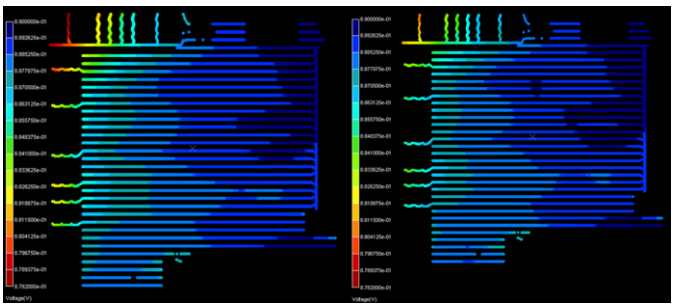

Fig. 9. Package layer1 IR drop contours, before and after improvements

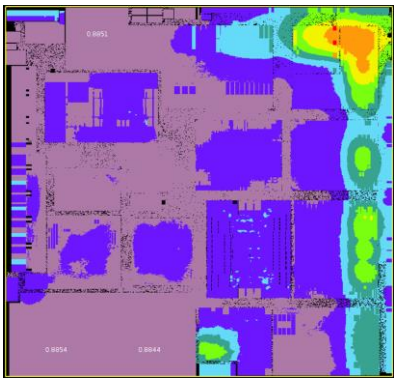

Fig. 10. IR drop map with per-bump model for improved package

Per bump package inductance distribution helps identify weak connections but few tools provide designers to do package level IR drop analysis by using bump currents taken from IR drop analysis [2]. This helps in discovering which weak connections to be fixed. Fig. 9 shows package level IR drop contours on layer1 of package, before and after shadow region package connection improvements.

IR drop analysis with per-bump model for improved package showed only 11 violations, worst being 0.04% above the IR drop target. Fig. 10 shows the IR drop map with per-bump model for improved package. In summary, lumped model based IR drop analysis doesn't uncover package weakness and per-bump model helps designers uncover those weaknesses.

V. Conclusion

Traditional lumped model based analysis represents optimistic results. As supply voltage values are going down, voltage drop margins are shrinking at each stage. Use of detailed per-bump package models help designers close the gaps in design level IR drop analysis and evaluate voltage drop targets accurately. Advancements in package extraction tools is allowing designers to quickly detect design flaws and make corrections in timely manner. Designers need to take advantage of these tool capabilities and carefully evaluate all components of the system through co-design efforts.

References

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