Flip-Chip Package for 28G SerDes Interface

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***Abstract*—This paper describes successful flip-chip package design for 28G-capable SerDes interfaces. Design optimization of the multi-layer 3D vertical BGA area is accomplished using an EM solver to obtain the best possible insertion and return losses given manufacturing capabilities. Several different stripline and microstrip pair-to-pair spacings bearing different amounts of coupling were evaluated in terms of eye opening and crosstalk-induced jitter. After full die-to-package-to-board assembly, the performance is measured up to 28G data rate. Both stripline and microstrip pairs were found to exhibit adequate performance.**

Keywords—Package design; flip-chip; SERDES; differential pair; broadband model; 3D electromagnetic simulation

I. INTRODUCTION

Packaging strategies for high-speed SerDes designs up to 28G demand that the differential lanes maintain a high quality low loss, low reflection signaling environment. Maintaining a low amount of crosstalk *between* the lanes is also paramount. Due to these concerns, an all-stripline package may be sought. While added layers can always be used to form stripline for all layers, confirmation that microstrip has adequate performance allows the outer layer to be used for signals. This in turn allows reduction of package layer count and potential cost-savings.

The key to successful use of microstrip is minimizing DRL at the BGA. The match on the die-side is controlled using a well-matched SerDes IO design. The far-end crosstalk (FEXT) is most important for parallel transmit (TX) channel crosstalk while the near-end crosstalk (NEXT) is less crucial especially since DRL is optimized. To limit TX-to-receive (RX) crosstalk the RX and TX are already separated on different layers, and RX pins are isolated from TX pins with ground pins. It is seen that for both microstrip and stripline cases, the total FEXT is not so different and stays better than <-40dB to out past the fundamental. The total crosstalk is often dominated by the BGA area pattern crosstalk, further reducing the difference between microstrip and stripline. Typically, the distance between the microstrip pairs is kept to 3x the in-pair spacing or more, and usually a ground stripe with vias to ground plane is possible between all pairs. It is shown that even in the case of long coupled microstrip pairs with spacing hardly greater than in-pair spacing, and no ground stripes, the overall performance, including crosstalk, was found adequate.

II. TEST VEHICLE PACKAGE DESIGN

The test vehicle package is of a ten layer 4-2-4 construction with a 1.0mm BGA pitch. An 800um core is used for reliability reasons. Modern low-loss build-up material is used to limit the insertion loss. The package was used in the characterization of a 28G SerDes interface.

As shown in Fig. 1, various main-line configurations were studied including stripline and microstrip. As shown on the left of Fig.1, normally-coupled microstrip pairs (left white circle), intentionally closely-spaced highly-coupled microstrip pairs (middle white circle), and normally-coupled stripline pairs (right white circle) were studied and characterized. Although the impact of the tighter coupling for the highly-coupled microstrip pairs on crosstalk was found obvious in the NEXT, the resulting effect on the measured performance under simultaneous switching conditions was less obvious. As will be shown, acceptable performance was found even for the highly-intentionally-coupled microstrip.

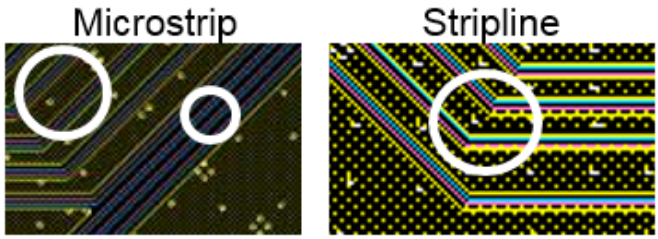

Fig. 1. Microstrip (USTR, left) and stripline (SLIN, right) layouts. Coupled lines examined as indicated. Right hand microstrip circle on xtra-XT USTR.

While losses are limited by using the low-loss material, the discontinuity at the board-to-package interface, in this case a ball-grid-array (BGA), gets minimized through careful design practice. Design parameters such as pad size, antipad size, void hole size and via pitch are adjusted and an optimized set of parameters is selected [2].

Please refer to Fig. 2 for the sequence of modeling results. Typically, a differential insertion loss (DIL) of better than > -3dB out to past 20GHz, and differential return loss (DRL) of better than <-20dB to 10GHz, are obtained in the frequency-domain. An in-pair coupling which is not too tight is used to help limit the common mode return loss to better than <-10dB to 10 GHz. Time-domain reflectometry (TDR) is also used to study and find local ways of reducing the impedance discontinuity through the BGA and vertical package structure.

As shown in the third chart of Fig 2, the differential NEXT of the normally-coupled microstrip is hardly different than that of the normally-coupled stripline. This is because the vertical

BGA-area is responsible for one-half or more of the typical crosstalk, both NEXT and FEXT. Whereas, for highly-coupled pairs, there are high NEXT peaks reaching up to worse than -40dB across the whole band. However, as indicated in the fourth chart of Fig 2., the FEXT among both microstrip types and the stripline are all more similar to each other, and below -40dB out to about 20GHz for all three lines types.

Full-wave modeling of the designs has been carried out in Ansys HFSS [3], including main line and BGA area. Modeling structures are directly converted from the physical design layout file. Frequency-dependent material properties are used in the modeling. A wideband set of passive, causal S-parameters with DC point and adequate low-frequency content, using small-enough frequency-spacing, is generated. The channel simulations are carried out in ADS [4] as shown in the final chart of Fig. 2. Standard driver, board models and pseudo-random data patterns are used for simplicity. Measurements on the simulated eyes indicate that even for the intentionally-coupled microstrip, the jitter is low enough and the eye height and width at-BER are large enough and compare favorably to the stripline. We also checked the noise induced at the receiver of a victim lane while all of its top aggressors switch simultaneously. In both measurements and simulation, the microstrip was found to have adequate performance compared to the normal stripline.

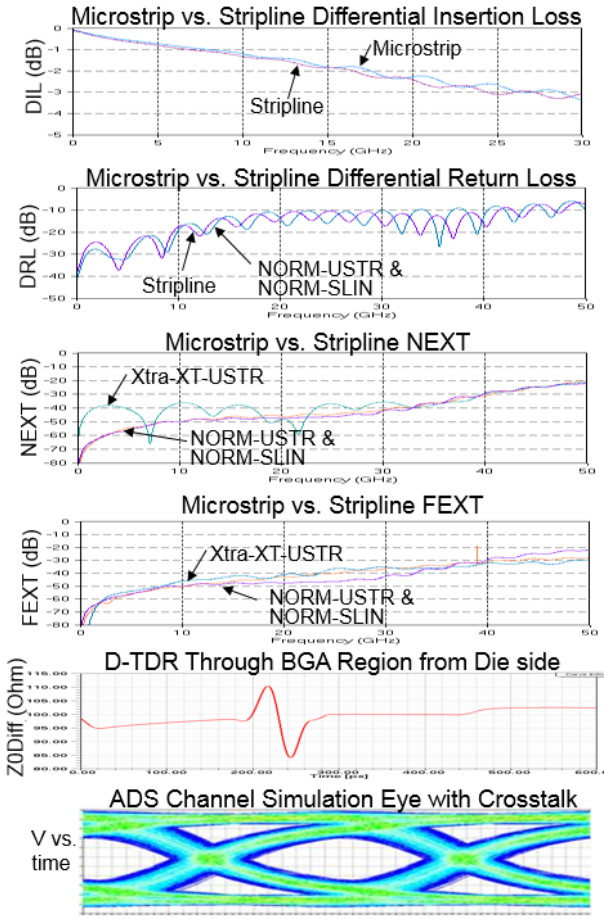

Fig. 2. HFSS and ADS Modeling and Simulation Data.

III. Benchtop Validation with 28G SerDes Silicon

In order to understand the impact of different microstrip and stripline routing schemes on 28G SerDes performance, the fully assembled active die in package on board is extensively tested on the benchtop. A BERTscope is used and the DUT is mounted on a high-speed test board. We measured output eye height and jitter of the modules under various noise modes, using the soldered-on probes for the best accuracy. Both full- (HFTP) and one-quarter-frequency (LFTP) alternating 1-0 patterns, and full-speed CJTPAT patterns were applied at 5G, 16G and 28G. The 28G protocol used was CEI-28G-VSR. Results showed adequate height and jitter for all types and cases. All eyes were measured under three modes: quiet, synchronous noisy, and asynchronous noisy. Asynchronous noisy pattern was achieved by running PCIe at a data rate other than that the victim lane being tested, on all aggressor lanes.

A compilation of the eye measurements is shown in Fig. 3. Note that the measured eyes include some additional effect of the printed-circuit board through-vias due to escaping to backside, and a small amount of board crosstalk adding in. Many additional eyes (not shown) were measured over different data rates, switching conditions, and protocols. These large amounts of lab data are summarized on subsequent bar charts as shown in Figs. 5-7.

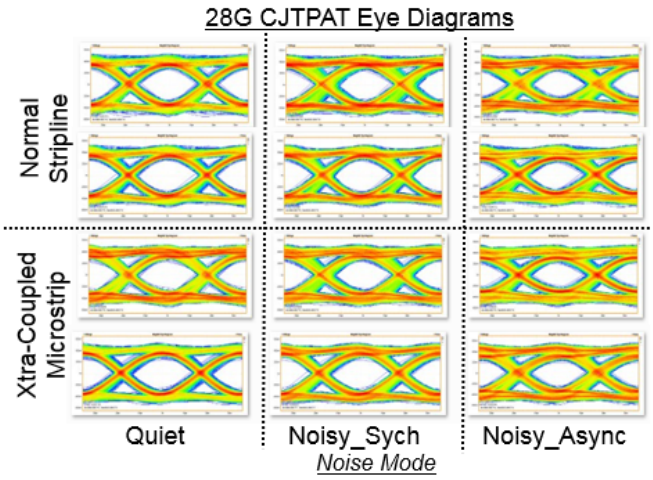

Fig. 3. Compilation of Eye measurements.

A compilation of the quiet-lane victim noise measurements is shown in Fig. 4, across 5G, 16G and 28G aggression data rates, for each line type indicated. As will also be summarized in the bar charts, neither the normal microstrip, nor the extra-intentionally-coupled microstrip, exhibit significantly larger quiet-lane noise than does the stripline.

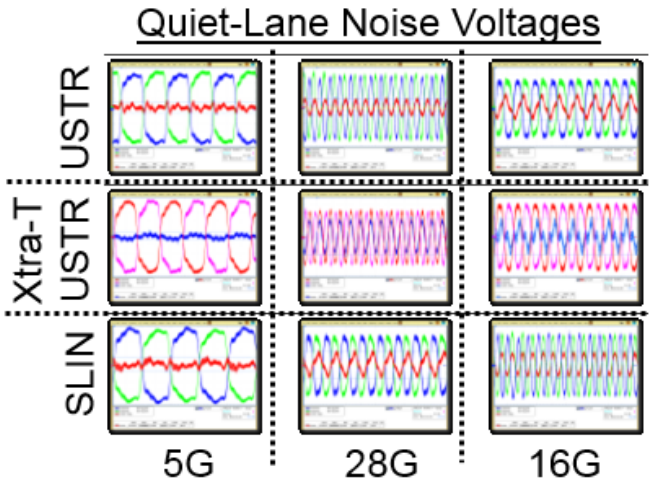

Fig. 4. Compilation of quiet-lane XT waveforms on various types of victim lines measured at 5G (left), 28G (middle) and 16G (right) data rate.

The results of jitter measurement for 5G, 16G and 28G are shown in Fig. 5. In all cases the quiet-mode (left set of four bars under protocol) is best, then the synchronous noise mode (middle four bars), and then the asynchronous noisy mode (right four bars) being the worst. The result is that the overall differences between the microstrip and stripline are small. The highly-coupled microstrip results, across several data rates, protocols and modes of crosstalk, were not measurably worse than the normal stripline.

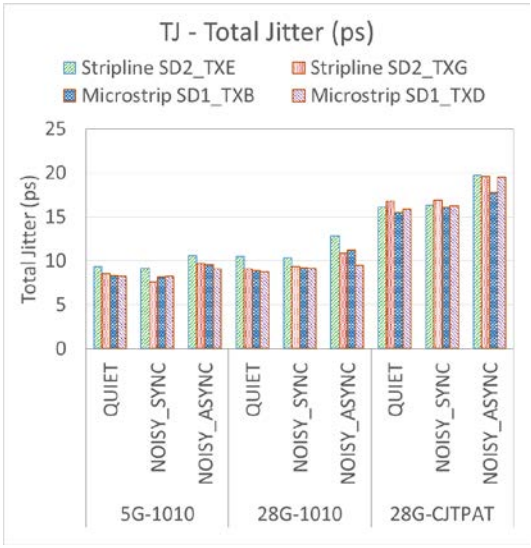

Fig. 5. Deterministic, random and total jitter for microstrip vs. stripline against pattern and noise mode.

The stripline vs. microstrip eye height measurement results are given in Fig. 6, by data rate and mode of crosstalk. It can be seen that plus or minus a few mV, all of the microstrip results compare favorably to the stripline results. The effect on risetime is also not too severe.

A summary of the quiet lane crosstalk results for each line type, is given in Fig. 7. These results indicate that the normal microstrip performs at least as good as the stripline.

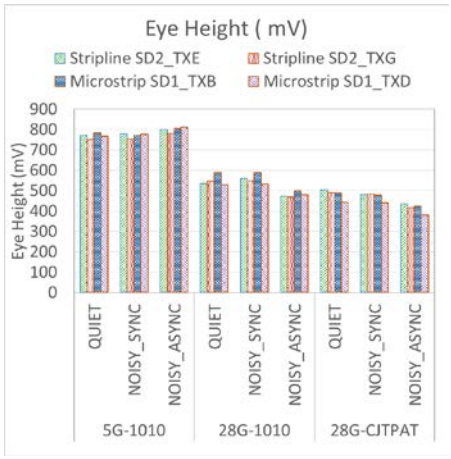

Fig. 6. Eye height and rise time for stripline vs. microstrip measurement against pattern and noise mode.

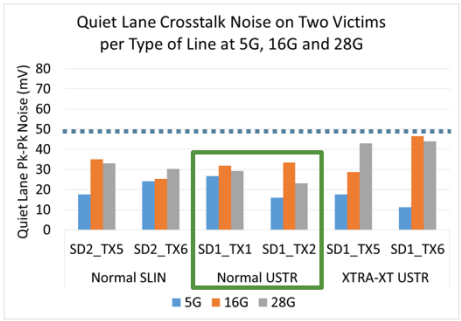

Fig. 7. Quiet Lane Crosstalk Noise per line type.

IV. Conclusion

Eye diagram and quiet-lane crosstalk noise measurements using various data patterns (including CJTPAT) are carried-out on a 28G-capable test vehicle. In comparing jitter, eye height, and quiet lane crosstalk data, it is found that the microstrip has a performance that is adequate. This is especially true when designed in the normal way with adequate spacing and ground-strip shielding as soon as possible after die fanout escape. Hence the package cost can be saved by using outer layers for signals, rather than need overlying ground.

Acknowledgment

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References

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