Modeling and Design of System-in-Package Integrated Voltage Regulator with Thermal Effects

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***Abstract*—This paper demonstrates a new approach to model the impact of thermal effects on the efficiency of integrated voltage regulators (IVRs) by combining analytical efficiency evaluations with coupled electrical and thermal simulations. An application of the approach shows that a system-in-package solution avoids thermal problems typically observed in other IVR designs. While the evaluation in this paper focuses on the thermal impact on loss in the inductor wiring and the PDN, the developed approach is general enough to also model thermal impacts on the power dissipation in the inductor cores and the buck converter chip.**

Keywords—integrated voltage regulator, buck converter, system-in-package, embedded passives, magnetic core inductor, thermal analysis, Joule heating

I. Introduction

Integrated voltage regulators (IVRs) have recently become a key research area in power delivery for electronic systems [1]–[4]. IVRs can increase the number of independent high-current voltage domains and improve the transient response [4], allowing a fine-grained spatio-temporal dynamic voltage-frequency scaling (DVFS). They can contribute to power savings and reduce the motherboard area occupied by discrete voltage regulators. IVRs of buck converter type are often used due to their ability to provide a wide range of output voltages. The passive elements required in the buck converter output filter can be embedded in package [4], on a silicon interposer [1], or on-chip [5]. Increasing levels of integration allow further system miniaturization, but at the same time makes the thermal design challenging. Higher power dissipation in the passive elements due to higher parasitic resistances as well as thermal coupling due to small separations can lead to high component temperatures [6], which in turn may considerably decrease the IVR efficiency. For this reason, the design of integrated voltage regulators should include a thermal evaluation approach that does not only evaluate component temperatures but also models the impact of component heating on efficiency to make sure that efficiency goals are achieved. Towards this end, this paper proposes an evaluation approach that combines an analytical efficiency evaluation with coupled electrical and thermal simulations. The approach is applied to evaluate the impact of inductor heating on the efficiency of a system-in-package (SIP) IVR, demonstrating that a suitable design can minimize the thermal impact on efficiency.

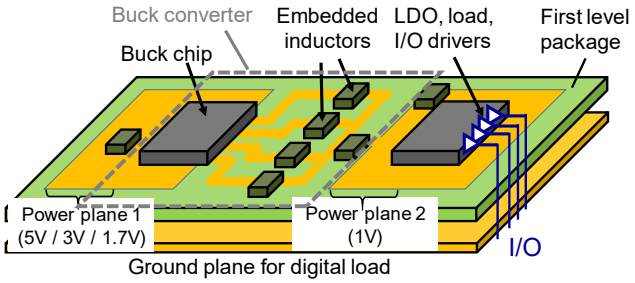

Fig. 1. SIP design as proposed in [7]. The buck converter part inside the dashed line is the focus of this paper, while a simplified model is used for the LDO / load chip. The output power of the buck converter is 10W. (Figure adapted from [7].)

II. IVR Design Modelled in this Paper

This section briefly introduces the IVR design that will be evaluated in this paper, as knowledge of the design is useful for the description of the thermal modeling approach in the following section. The targeted design is a two-chip solution as shown in Fig. 1, consisting of a buck converter for downconversion of the input voltage and multiple LDOs to provide clean input power for multi-gigabit I/O drivers and a fine-grained DVFS for the load chip. In this paper, the focus is on the analysis and optimization of the buck converter with the required embedded inductors, using a simplified model for the load. The buck converter designed in [7] has four phases with one master and three slave phases. The power stages use a stacked topology, which increases the acceptable operating input voltage to twice the breakdown voltage of a single device. Through this design, a single-stage 5V:1V conversion is enabled which can be used to eliminate an off-package conversion stage. Each of the four inductors has 25nH of inductance and uses a magnetic core to reduce size and DC resistance of the inductor. The design is the result of an optimization described in [7].

III. Thermal Modeling Approach

This section describes the approach to model the impact of component heating on efficiency by combining analytical evaluations with coupled electrical and thermal simulations as shown in Fig. 2.

A. Analytical IVR Efficiency Evaluation

This approach is based on analytical equations that model the major loss contributions – namely resistive and switching loss in the FETs, AC and DC loss in the inductors, loss due to the equivalent series resistance (ESR) of the capacitor and loss in the power distribution network (PDN) – as described in detail in [7]. The analytical approach allows to accurately track the impact of switching frequency, load condition and component design on overall IVR efficiency and loss breakdown. In this paper, the evaluation of AC and DC loss in the inductor is different from [7]. The inductor AC power loss, $P_{L,AC}$, is again calculated from an analytical equation as:

$$P_{L,AC} = \sum_{n=1}^{N} \left\| \hat{I}_L(f_n)/\sqrt{2} \right\|^2 \cdot ESR_L(f_n) \qquad (1)$$

based on the first N harmonics of the one-sided spectrum of the inductor ripple current, with current amplitude $\hat{I}_L$ and equivalent series resistance of the inductor ESR_L. An example of the inductor current and the corresponding one-sided spectrum is shown in Fig. 3 for the IVR design described in Section II with a switching frequency of 100 MHz. The AC inductor loss is dominated by the magnetic material and can be assumed to be localized in the inductor core for the thermal simulation. The DC loss, in contrast, is distributed, and therefore simulated using the approach described below.

B. Simulation of DC loss

To obtain the DC inductor loss, a commercial simulation tool [8] is used that can accurately capture the distribution of the DC loss in the inductor wiring and provide a power map that can be imported into the thermal simulation tool [9]. At the same time, the overall power dissipation from the simulation can be fed into the analytical efficiency evaluation. Due to the simulation approach, DC losses in the inductor and the PDN are combined into a single value.

C. Inputs to the Thermal Simulation

The dissipated power in the buck converter chip and in the inductor cores, which is needed as an input to the thermal simulation, is a direct result of the analytical efficiency evaluation described in Subsection A. The power map corresponding to the DC loss in the inductor windings and in the PDN is imported into the thermal simulation from the electrical simulation described in Subsection C.

D. Feedback from the Thermal Simulation

The results of the thermal simulation are fed back in two ways, as illustrated in Fig. 2. A list of component temperatures is fed back to the analytical evaluation. At the same time, a detailed heat map is provided to the DC loss simulation. While the evaluation in Section IV of this paper focuses on the latter aspect – the impact of the increased copper temperature on the

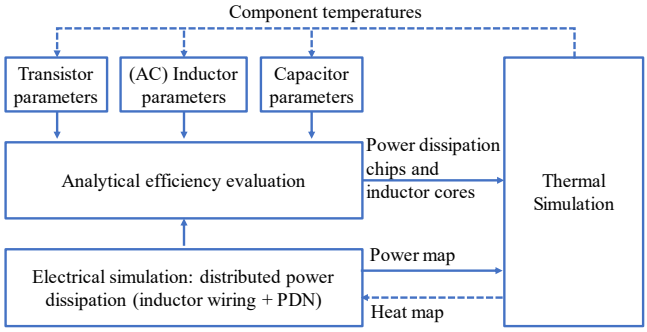

Fig. 2. Suggested simulation approach. Dashed lines indicate feedback from the thermal simulation. Simulations are carried out iteratively until the thermal simulation has converged.

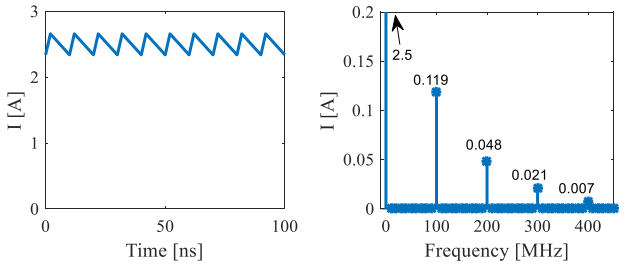

Fig. 3. Left: Current through one of the 4 inductors. A 2.5A DC current is superposed with a 320mA peak-peak AC ripple current with 20% duty cycle. Right: Corresponding one-sided spectrum of the inductor current.

DC loss in the inductor wiring and the PDN – it should be noted that the proposed approach is general enough to take into account the impact of component heating on the power dissipation in the chips and the inductor cores as well. As the changed power dissipation will in turn change the thermal result, loss evaluation and thermal simulation are carried out iteratively until the thermal simulation result converges.

IV. Results of the Thermal Simulation

Two scenarios are evaluated in this section. The first one studies the self-heating of the inductors, while the second one is a simulation of the full SIP that takes into account thermal coupling between inductors and chips. Both scenarios assume an ambient temperature of 21°C and the maximum load condition (10W power provided to and dissipated in the load).

A. Self-heating of the Inductors

For the analysis of self-heating, the SIP described in Section II is simulated without the two chips. The analytical efficiency evaluation provides 27mW of power dissipated in each inductor core, while the DC simulation provides an overall DC loss of 613mW. The thermal simulation result shows that without additional heat-sources in the system, the inductor temperature resulting from power dissipation in the magnetic core and the metal traces is limited to about 28°C, as listed in Table I. The thermal simulation converges – in good approximation – with the second iteration.

B. Thermal Simulation of the Complete SIP

The complete SIP was simulated including power dissipation in the two chips (4.2W in the buck chip obtained

from the analytical evaluation and 10W in the load chip) and cooling by a fan with 30cfm volumetric air flow placed above the load chip. It should be noted that the focus of this paper is not the optimization of the cooling scenario, but rather the thermal analysis of the SIP for fixed conditions. The thermal simulation result for the top metal layer, which contains power planes, routing traces and the bottom windings of the inductors, is shown in Fig. 5. While some heat spreading from the chips into the inductors can be observed, the inductor temperature is still limited to about 43°C., as shown in Table I. The observed heating increases the metal resistance, increasing the power dissipation in the traces by 11.3% compared to ambient temperature. However, the resulting change in the loss breakdown and the overall power dissipation is very small as shown in Fig. 4, reducing the overall system efficiency only by 0.3%. A second thermal simulation shows that again, the thermal simulation converges with the second iteration.

TABLE I. COMPONENT TEMPERATURES IN °C

	Inductor only 1st it.	**Inductor only 2nd it.**	**Complete system 1st it.**	**Complete system 2nd it.**
Inductor 1	28.19	28.42	41.64	42.36
Inductor 2	28.36	28.59	43.02	43.77
Inductor 3	28.24	28.47	42.87	43.61
Inductor 4	28.23	28.46	41.61	42.28
Buck chip	-	-	72.49	73.04
Load chip	-	-	92.48	93.65

C. *Comparison to an Alternative IVR Design*

In [6], a thermal analysis is carried out for an IVR with embedded inductors on a silicon interposer, which provides a 1.8V:1V conversion for 5W output power. The solution in [6] provides strong integration and system miniaturization, but leads to a high inductor temperature of 96°C even after thermal optimization. While the thermal impact on efficiency is not evaluated in [6], a simple estimation based on the temperature coefficient of copper and the loss breakdown provided in [6] indicates that overall efficiency can decrease by about 5% due to the thermal impact on the DC loss in inductor wiring and PDN. This illustrates the importance of combining modeling with design that takes into account the impact of component heating on efficiency. It furthermore illustrates the advantages of the SIP IVR design evaluated in this paper, which – in return for a larger system size – avoids thermal problems by using passive elements with low loss and limiting thermal coupling through sufficient spacing between inductors and chips.

V. CONCLUSION

Using a newly developed evaluation approach, this paper has shown that a system-in-package realization of an integrated voltage regulator with magnetic core inductors is advantageous from a thermal point of view. The heating of the inductor wiring and the PDN changes the overall IVR efficiency by less than 1%. The evaluations in this paper do not take into account the effect of heating on the magnetic material. It is expected that this impact will be negligible as long as the inductor temperature remains in the predicted range below 60°C.

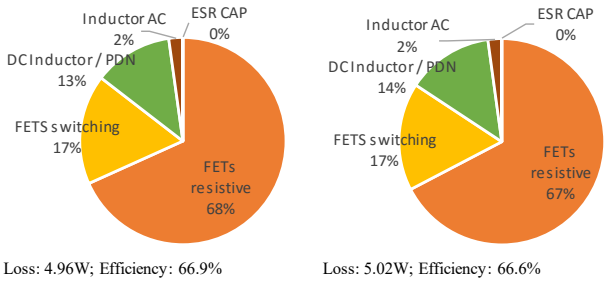

Fig. 4. Left: Loss breakdown and overall efficiency for the 5V:1V conversion at 100 MHz switching frequency. Left: without thermal impact. Right: with thermal impact.

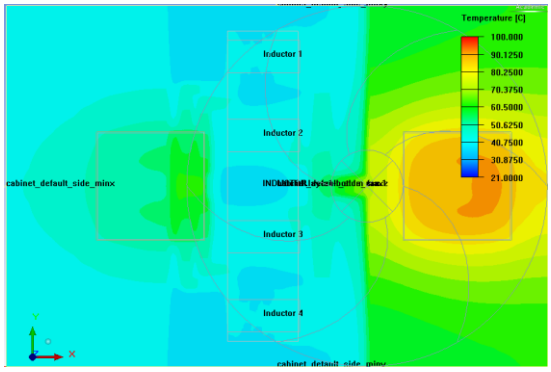

Fig. 5. Temperature distribution in the top metal layer of the SIP (power planes, routing and inductor bottom windings) simulated with [9].The highest temperature is reached in the load chip (see Table I). Heat spreading from the chips into the inductors exists but is limited.

ACKNOWLEDGMENT

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