Time domain PDN noise modeling for high performance system

Han-Biao Jin[1], Er-Ping Li[2], Albert E. Ruehli[3], James L. Drewniak[4], and Bruce Archambeault[5]

[1,2]Zhejiang University jinhb@zju.edu.cn liep@zju.edu.cn
[3,4,5]Missouri University of Science and Technology albert.ruehli@gmail.com drewniak@mst.edu Brucearch@aol.com

***Abstract*—In this paper, we investigate the impact of the PDN inductance/impedance as well as the decoupling capacitors location on the initial IC noise voltage drop for a high performance system. To consider a worst case situation for the noise voltage at the integrated circuit (IC) we set the on-chip capacitance to zero. The impact of the delay due to remote location of the decoupling capacitors for fast rise-time current waveforms is also studied.**

***Index Terms*—power distribution modeling, power integrity analysis, PPP solver**

I. Introduction

An essential function of the decoupling capacitor in high performance systems is to keep the noise voltage directly at the integrated circuit chip (IC) sufficiently small. However, the initial voltage at the IC is difficult to control due to the impedance of the plane pair and the arrangement of decoupling capacitors. To clearly determine the worst case impact, we assume that the integrated circuit (IC) on-chip decoupling capacitor are zero and that the package decoupling capacitors are lossless.

We use a usual triangular waveform for the current drawn by the IC in our model, which is shown in a simplified form in Fig. 1. Since the system is linear we need to compute the response only for a single pulse $i(t)$. Any combination of pulses can be constructed by superposition of the solution due to $i(t-\tau)$ where τ is the appropriate delay time of the pulse portions. We assumed than the peak current for the single IC pin model is 150 mA.

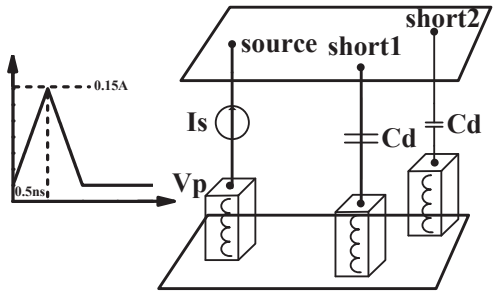

Fig. 1. Current waveform and simplified illustration of PCB model

We based our solver on the Parallel Plane PEEC (PPP) method for the solution [1]. We show that for the frequency range of interest, an equivalent full-wave solution can be obtained without introducing delay or retardation for the partial elements due to the cancellation of the distant couplings. This is confirmed by a comparison of the solution with the CST Microwave Studio [2]. To compare the time domain solutions between the solvers we applied a step response to the structure. The response and the good agreement is shown in Fig. 2.

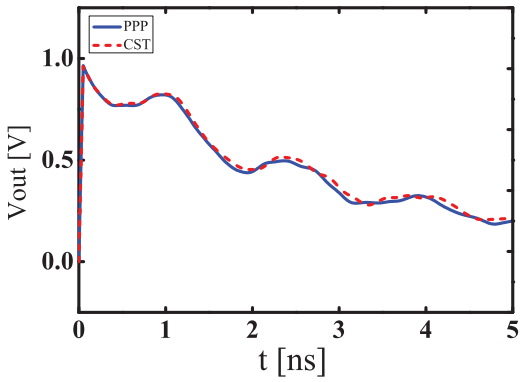

Fig. 2. PPP and CST time domain results comparison

A large number of experiments have been performed to understand the sensitivity of the noise voltage reduction based on the details of the connection, the printed circuit board and the location of the capacitors. We found some rather surprising results from the experiments performed. One aspect of interest was the delay which results due to the physical distance between the IC and the decoupling capacitors. The plane inductance or impedance is an important aspect of the problem.

II. Time domain solver formulation

In this short paper we point out the important features of the solver formulation. It is required that the solver provides a good high frequency response since we are investigating the short time - high frequency solution aspects. The solution approach is based on the Parallel Plate PEEC (PPP) method developed recently [3], [4], [1]. However, it at first seems that the conventional PPP solution does not fulfill the requirements since the partial inductances in the PPP method are evaluated in a quasi-static form without retardation. However, the opposite current it the planes leads to the so called difference inductance [5] for the plane pairs mutual coupling shown in Fig. 3. The difference inductance for the plane-pair cells to plane-pair cells coupling is given by

$$Ld_{km} = \frac{V_a - V_b}{I_m} = \frac{Vd_k}{sI_m} = 2(Lp_{km} - Lp_{km'}). \quad (1)$$

Importantly, the difference coupling inductance Ld decays rapidly and that the impact of the retardation between the distant partial inductances can be neglected. This leads to a sparse MNA circuit matrix such that the retardation also leads to a speed-up in the solution [1].

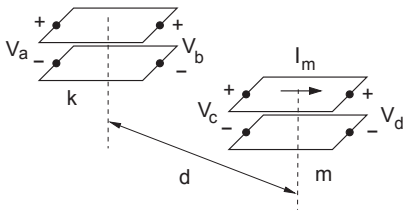

Fig. 3. Coupling between two pairs of overlapping cell pairs.

The modeling of PDN systems has been performed at different levels, e.g., [6]. This work specifically aims to answer several important questions regarding the design of the decoupling capacitor arrangement which is difficult for high performance systems. Mainly, the initial noise voltage is excessive. As we show in the next section, it is difficult to find an arrangement for which the delay and impedance is sufficiently small. With this work, we aim at pointing out the sensitivities of different arrangements.

III. Numerical Experimental Noise Investigation

In all our experiments we uses a plain-pair which was 50 mm wide. The majority of our experiments were done with plane pairs which were 150 mm long. However, in our first experiment in the next section the length was also 50 mm. We note that we are mostly concerned about the amplitude of the response up to 1 ns which relates directly to the switching currents. All our responses are measured directly at the IC. Also, all our experiments are conducted with decoupling capacitors with a total value of 1 μF. To be able to separate the impact of the different parts of the path, we are assuming that the decoupling capacitors are perfect by setting the inductance and the ESR series resistance to zero.

A. Inductance/Impedance

In this section, we compute the obvious case where we connect the decoupling capacitor directly at the IC connections. The response of this case is the dotted waveform in Fig. 4. This result is as expected. In the same figure we place a 1 μF decoupling capacitor 10 mm from the IC. We see that the noise voltage increases to about 70 mV for an assumed size of the plane connection pin to have a diameter of 0.25 mm. In this subsection, the plane size is $50mm \times 50mm$, where the IC is located at the center (25 mm, 25 mm) and the decoupling capacitor is located at (15 mm, 25 mm) and the plane-to-plane spacing is 0.125 mm. The distance is small enough such that the delay time form the IC to the capacitor is less than 100 ps and that it does not impact the result.

1) Size of the IC connection: Another interesting aspect in view of the ever decreasing miniaturization is the size of the pin or connection to the PC board. Fig. 5 shows the frequency and time domain results for different difference IC pin sizes from 0.25 mm to 1 mm. From the impedance curve, we can easily compute that the inductance is 0.22nH, 0.19nH and 0.15nH for 0.25mm, 0.5mm and 1mm pin size. A smaller pin sizes results in a larger inductance.

We see that the pin contact size has an appreciable impact on the noise waveform.

2) Plane-to-plane distance: Figures. 6 shows the frequency as well as the time domain results for difference plane-to-plane spacing. The larger plane-to-plane separation strongly increases the plane inductance and impedance. From this it is clear that for high performance structures it is required that the planes are placed very closely to keep the plane impedance as low as possible.

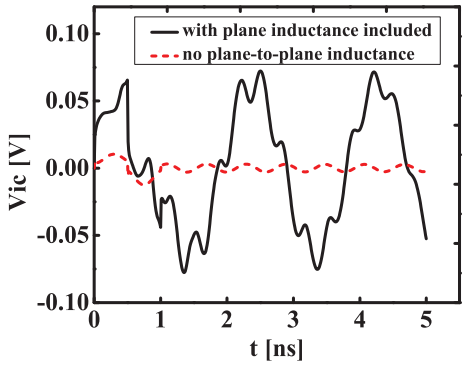

Fig. 4. V_{ic} of a normal case and ideal case when plane inductance is 0

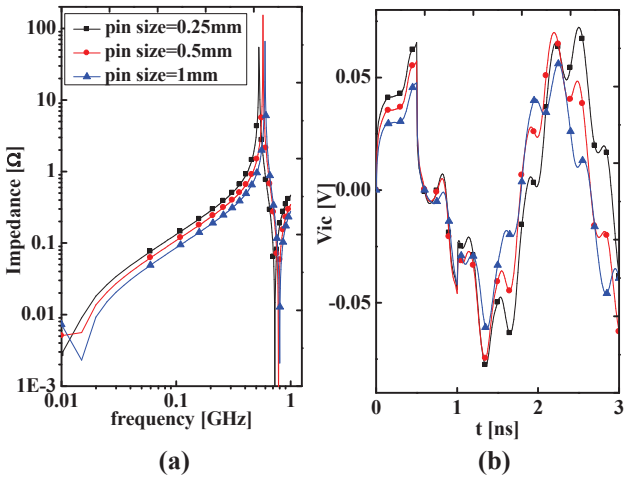

Fig. 5. IC pin size study (a) Results frequency domain solution: Impedance (b) Results time domain solution: V_{ic}

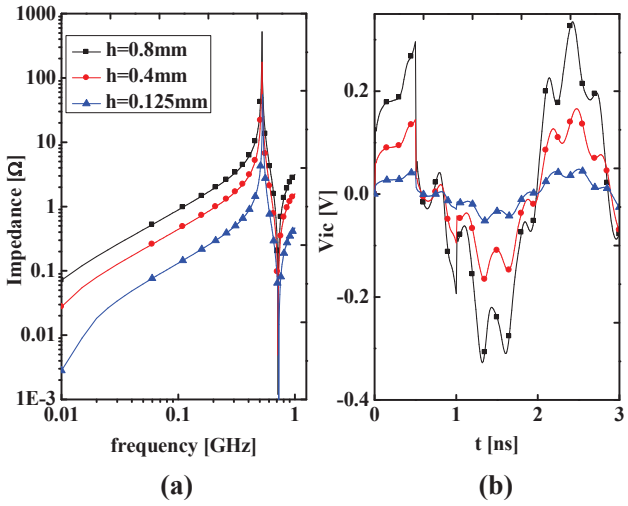

Fig. 6. Impact of different spacings h for parallel planes (a) Frequency domain result: Impedance (b) Time domain result: V_{ic}

B. Decoupling capacitors placement

It is well known that the plane inductance plays a very important role in the noise performance at the IC. In these part of the study, the IC pin size is 0.25mm and the plane-to-plane spacing was 0.125mm.

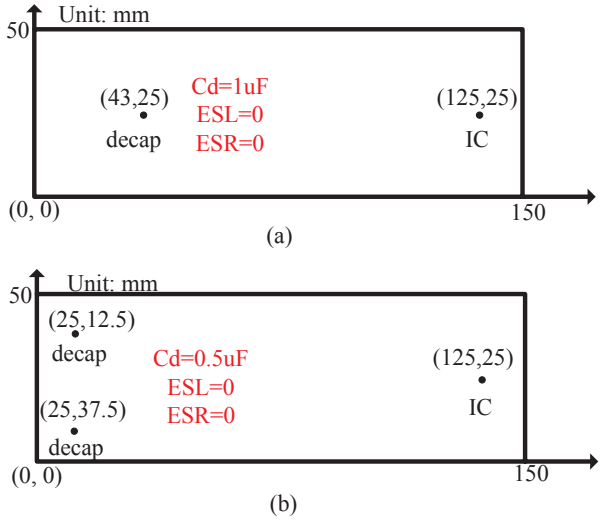

Fig. 7. Decoupling capacitors arrangement (a)case A (b)case B

Here, as shown in Fig. 7, we look at two situations , case A and case B, with the same loop inductance but different decoupling capacitors arrangement mainly the distance(delay) part different. In case A, a $1\mu F$ decoupling capacitor is 82mm away form the IC and in case B, two $0.5\mu F$ decoupling capacitors are 100mm away from the IC. There is a 18mm distance difference between case A and case B.

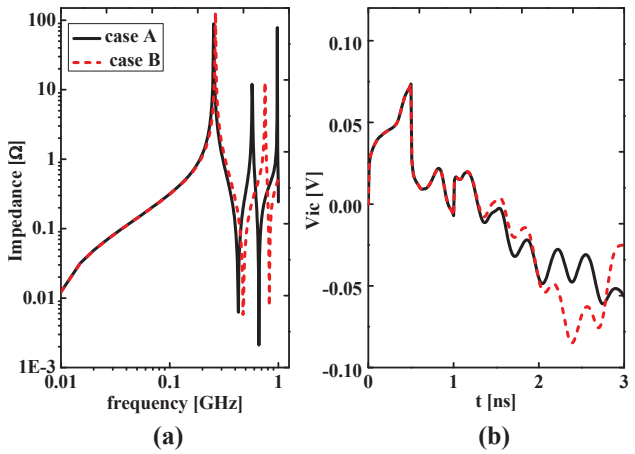

Fig. 8. Frequency and time domain result of case A and case B

From Fig. 8(a), we can see that the inductance between case A and case B is the equivalent. Fig. 8(b) is the time domain V_{ic} result of case A and case B. In the initial waveform, i.e. first 1ns, is the practically the same for case A and case B. When the inductance is large enough and if it dominates the output, the distance(delay) part has no impact on ΔV.

1) Impact of delay time on solution: In this section we finally consider the impact of the delay due to the physical spacing between the IC and the decoupling capacitor. The goal for both cases is to set up the capacitors such that inductance from the capacitors to IC is the same. Meanwhile, in order to weaken the inductance's influence so that we can see the impact of delay, this inductance should be much smaller compared to that in case A and case B This was accomplished by placing one capacitor at a distance of 17 mm. The second case had two decoupling capacitors a distance of 37 mm from the source. Hence the two capacitors are 20 mm further away from the IC in the second case. Fig. 9 shows that the noise voltage is about 10 mV larger for the more distant capacitors with additional delay in comparison to the single capacitor placed 20 mm closer. We conclude from this study that the impact of the delay time is relatively small in comparison to the impact or the plane pair impedance even for high performance designs.

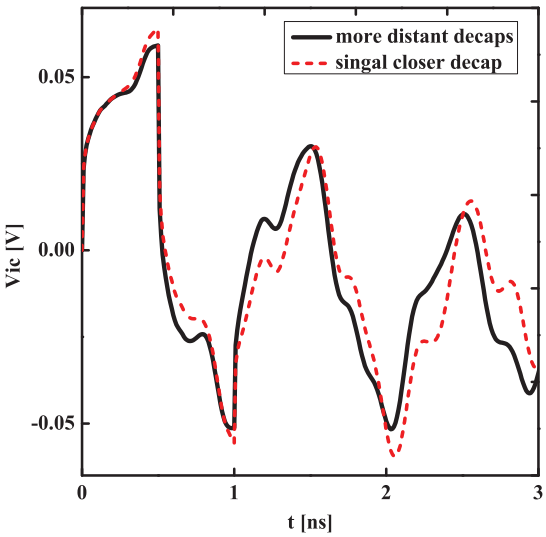

Fig. 9. Time domain V_{ic} result of case C and case D

IV. Conclusions

In this short paper we studied different design aspects of the PDN system. We show that the impedance of the connection from the IC to the decoupling capacitors must be designed carefully for high performance systems.

References

[1] L. Wei, K. Shringarpure, A. E. Ruehli, E. Wheeler, and J. Drewniak, "Plane-pair PEEC models for PDN using sub-meshing," in *EPEPS*, vol. 22, Portland, OR, Oct. 2013, pp. 159–162.

[2] *CST Studio Suite, 2006B*, Computer Simulation Technology, www.cst.com, 2007.

[3] F. Zhou, A. E. Ruehli, and J. Fan, "Efficient mid-frequency plane inductance computations," in *Proc. of the IEEE Int. Symp. on Electromagnetic Compatibility*, Fort Lauderdale, FL, Aug. 2010, pp. 831–836.

[4] L. Li, A. E. Ruehli, and J. Fan, "Accurate and efficient computation of power plane pair inductance," in *Proc. of the IEEE Int. Symp. on Electromagnetic Compatibility*, Philadelphia,PA, Aug. 2012.

[5] A. E. Ruehli, G. Antonini, and L. Jiang, *The partial element equivalent circuit method for electromagnetic and circuit problems*. John Wiley and Sons, New York, 2016.

[6] K. Jingook, K. Shringarpure, F. Jun, K. Joungho, and J. L. Drewniak, "Equivalent circuit models for power bus design in multi-layer PCBs with via arrays," *IEEE Microwave and Wireless Components Letters*, vol. 21, pp. 62–64, 2011.