Enlarged Cell Technique for Conformal Equivalent Circuit Model of Power Delivery Network

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***Abstract*—This paper describes a technique to improve a conformal equivalent circuit model for efficient transient analysis of a power delivery network (PDN). The conformal equivalent circuit of the PDN may include small capacitance due to an irregular cell, which has a small conductor area. The small value of the capacitance makes the time step size of an explicit leapfrog scheme be small to ensure its numerical stability condition. The proposed enlarged cell technique is based on enlargement of the conductor area in the irregular cell to derive a larger capacitance and avoid the time step size reduction.**

***Index Terms*—conformal equivalent circuit model, enlarged cell technique (ECT), fast transient analysis, power delivery network**

I. Introduction

Verification of a power delivery network (PDN) is one of the common and important issues in signal/power integrity (SI/PI) design because power-supply noises seriously affect the PI of an electronic circuit and thereby the SI of high-speed interconnects. Therefore, it is necessary to develop proper modeling and efficient simulation techniques for the PDN.

For circuit modeling of the PDN, both rectangular mesh and triangular mesh approaches have been studied [1], [2]. However, the number of the meshes tends to be large to represent the exact shape of a complex and fine structure even if unstructured triangular meshes are used.

Recently, we have proposed a conformal equivalent circuit model to reduce the number of the meshes without losing the accuracy [3]. In addition, it has been demonstrated that an explicit leapfrog scheme is suitable for the conformal equivalent circuit to achieve the fast simulation of the PDN [3]. However, due to a limitation of a time step size, the efficiency of the leapfrog scheme degrades in the simulation including an irregular cell, which has a small conductor area. More recently, we have provided one of the remedies to the time step size limitation by adopting an implicit difference scheme [4]. In this paper, we propose a circuit-oriented enlarged cell technique (ECT) for the conformal equivalent circuit model to avoid reducing the time step size of the leapfrog scheme.

II. Existing Methods and Their Limitations

A. Conformal Equivalent Circuit Model

The structure focused on in this paper is a pair of parallel conductor planes on both sides of a dielectric substrate, which is a typical PDN structure of a board and a package. We assume that the bottom conductor is a ground plane, and the upper plane is divided by orthogonal meshes into a number of cells on the x-y coordinate system. In the conformal modeling technique, the meshes themselves are not required to represent an exact shape of the plane, and some cells may contain both conductor and air as shown in Fig. 1(a). We call such a cell with mixed materials a subcell and define conformal meshes as orthogonal meshes including subcells. As illustrated in Fig. 1(a), the conformal equivalent circuit model uses the main and dual conformal meshes [3]. The main mesh is used to derive resistance and inductance, and the dual mesh is used for conductance and capacitance of the equivalent circuit. Fig. 1(b) shows a cell-based circuit around the grid point (a, b), where a and b are the nonnegative integers, and the entire parallel plane structure can be constructed by interconnecting a number of cell-based circuits.

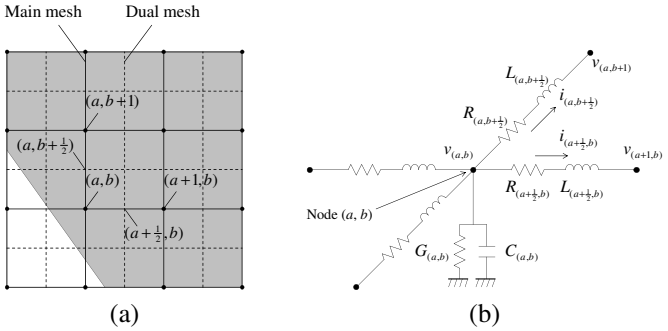
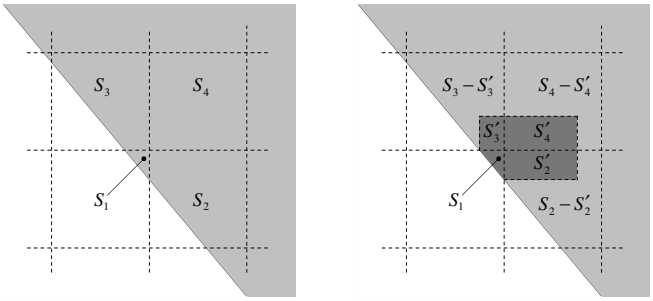


Fig. 1. An conformal equivalent circuit model. (a) The top view of the conductor plane with a non-orthogonal contour. The gray part is the conductor, the white part is air, and the solid and the dashed line represent the main and the dual mesh. (b) The conformal equivalent circuit model around (a, b).

For example, the capacitance $C_{(a,b)}$ at the node (a, b) in Fig. 1(b) can be calculated by [3]

$$C_{(a,b)} = \varepsilon \frac{S_{(a,b)}}{h} \tag{1}$$

where ε is the permittivity of the dielectric between the conductor planes, h is the distance between the planes, and $S_{(a,b)}$ is the conductor area of the subcell. If $S_{(a,b)}$ is calculated accurately, we can compensate the inaccuracy of the shape



(a) (b)

Fig. 2. The cell enlargement procedure. The light gray part is the conductor, and the dark gray parts are the intruded areas. (a) The irregular cell of S_1 and the adjacent cells of S_k, $k = 2, 3, 4$. (b) S_1 is enlarged and becomes $S_{\text{eng}} = S_1 + S'_2 + S'_3 + S'_4$.

representation of the conformal meshes, and the accurate element value is obtained. The other element values can be derived in a similar manner. As depicted in Fig. 1, an edge of the main mesh corresponds to a series RL branch, and a parallel GC path is connected between the node of the grid point (a, b) and the ground. For simplicity, we consider a lossless case below, namely, $R = G = 0$ in Fig. 1(b).

B. Time Step Size Limitation of the Explicit Leapfrog Scheme

The time step size of the explicit leapfrog scheme is limited by the numerical stability condition [5]

$$\Delta t \leq \min_{a,b} \left(\sqrt{\frac{2C_{(a,b)}}{N_{(a,b)}}} L_{\min,(a,b)} \right) \tag{2}$$

where $N_{(a,b)}$ is the number of inductors connected to the node (a, b), and $L_{\min,(a,b)}$ is the minimum inductance among them. The condition (2) indicates that low reactances force the time step size to be small. From (1), it is obvious that the capacitance is proportional to the conductor area $S_{(a,b)}$ in the subcell and inversely proportional to the dielectric thickness h. Since h is generally constant throughout the PDN and sufficiently small, it does not decrease the time step size. On the other hand, the small conductor area induces the time step size reduction. As for the inductance, it depends on the aspect ratio of the conductor area [3]. In general, the aspect ratio is not changed in both small and large cells to ensure the accuracy, and therefore, the inductance is uniform in the conformal equivalent circuit. Because of this, we assume that the inductance does not affect the time step size reduction. Consequently, one of the ideas to avoid reducing the time step size is enlarging the small conductor area to achieve a large value of $C_{(a,b)}$.

III. Enlarged Cell Technique (ECT) for the Conformal Equivalent Circuit Model

Kirchhoff's current law (KCL) applied to the node (a, b) in the conformal equivalent circuit leads to

$$C_{(a,b)} \frac{dv_{(a,b)}}{dt} = -\tilde{i}_{(a,b)} \tag{3}$$

where $\tilde{i}_{(a,b)}$ is the net current flowing from the node (a, b). The explicit leapfrog scheme discretizes (3) by staggering the time points of the voltage and the current and provides the difference equation

$$\varepsilon \frac{S_{(a,b)}}{h} \frac{1}{\Delta t} \left(v^{n+\frac{1}{2}}_{(a,b)} - v^{n-\frac{1}{2}}_{(a,b)} \right) = -\tilde{i}^{n}_{(a,b)} \tag{4}$$

where n is the index of the time step, Δt is the time step size, and we intentionally rewrite the capacitance by using the physical dimensions and parameter in (1). The updating formula of the voltage can be derived by transforming (4):

$$v^{n+\frac{1}{2}}_{(a,b)} = v^{n-\frac{1}{2}}_{(a,b)} - \frac{h\Delta t}{\varepsilon} \frac{\tilde{i}^{n}_{(a,b)}}{S_{(a,b)}}. \tag{5}$$

If the conductor area $S_{(a,b)}$ in (5) is small, the capacitance value is also calculated to be small, and we have to reduce the time step size.

To avoid the time step size reduction, we propose the circuit-oriented ECT, which enlarges such an irregular conductor area to acquire a large value of $C_{(a,b)}$ in a similar manner in [6]. First, by assuming the total charge $q_{(a,b)}$ related to the net current $\tilde{i}_{(a,b)}$ flowing from the cell (a, b) and taking into account its time rate, we define the time rate of the charge density, $\hat{\rho}_{(a,b)}$, as

$$\hat{\rho}_{(a,b)} \equiv \frac{d\rho_{(a,b)}}{dt} = \frac{1}{S_{(a,b)}} \frac{dq_{(a,b)}}{dt} = \frac{\tilde{i}_{(a,b)}}{S_{(a,b)}} \tag{6}$$

where $\rho_{(a,b)} = q_{(a,b)}/S_{(a,b)}$ is the charge density. Note that $\hat{\rho}_{(a,b)}$ appears in the last term of (5).

Next, assume that the irregular cell with the small conductor area S_1 as shown in Fig. 2(a). Hereafter, we refer to the cell (a, b) as the cell 1, and the same goes for the related values, e.g., $S_{(a,b)}$ as S_1. Additionally, we assume the three numbered cells adjacent to the cell 1 as illustrated in Fig. 2(a). In this case, S_1 is enlarged to S_{eng} with which the numerical stability condition is satisfied without reducing the time step size. This is achieved by enlarging S_1 into its adjacent cells of S_k ($k = 2, 3, 4$) so that

$$S_{\text{eng}} = S_1 + S'_2 + S'_3 + S'_4 \tag{7}$$

where S'_k are the intruded areas of the adjacent cells shown in Fig. 2(b). The net current $\tilde{i}_{\text{eng}}$ flowing from the enlarged cell can be written as

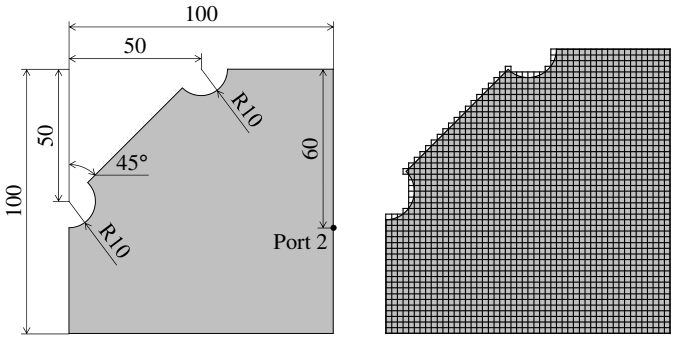
$$\tilde{i}_{\text{eng}} = \hat{\rho}_1 S_1 + \hat{\rho}_2 S'_2 + \hat{\rho}_3 S'_3 + \hat{\rho}_4 S'_4 \tag{8}$$

where $\hat{\rho}_k$ is the time rate of the charge density in an adjacent cell. Therefore, the time rate of the charge density $\hat{\rho}_{\text{eng}}$ in the enlarged cell is

$$\hat{\rho}_{\text{eng}} = \frac{\tilde{i}_{\text{eng}}}{S_{\text{eng}}} = \frac{1}{S_{\text{eng}}} \left(\hat{\rho}_1 S_1 + \hat{\rho}_2 S'_2 + \hat{\rho}_3 S'_3 + \hat{\rho}_4 S'_4 \right). \tag{9}$$

Finally, for the cell 1, since the total area S_1 of the conductor is inside the enlarged cell with $\hat{\rho}_{\text{eng}}$, its new net current $\tilde{i}_{1\text{new}}$ is

$$\tilde{i}_{1\text{new}} = \hat{\rho}_{\text{eng}} S_1 \tag{10}$$



(a) (b)

Fig. 3. The example PDN (unit: mm). (a) The shape and dimensions. (b) The conformal meshes including a number of irregular cells.

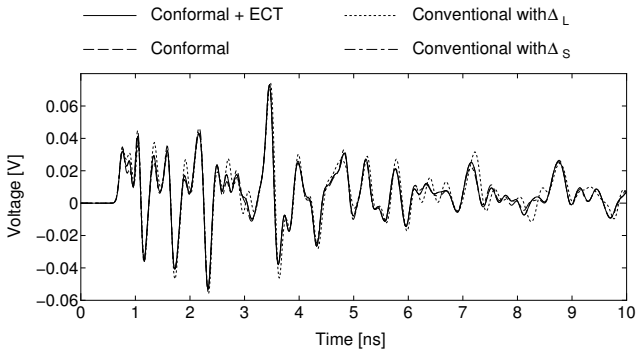


Fig. 4. The waveform results.

and then (5) is rewritten as

$$v_1^{n+\frac{1}{2}} = v_1^{n-\frac{1}{2}} - \frac{h\Delta t}{\varepsilon}\hat{\rho}_{\text{eng}} \tag{11}$$

where $v_1 = v_{(a,b)}$. In (11), the enlarged cell area S_{eng} is used instead of the irregular area S_1. For the adjacent cell k, its new current $\tilde{i}_{k\text{new}}$ is obtained as

$$\tilde{i}_{k\text{new}} = \hat{\rho}_{\text{eng}} S'_k + \hat{\rho}_k \left(S_k - S'_k\right) \tag{12}$$

and the associated updating formula of the voltage becomes

$$v_k^{n+\frac{1}{2}} = v_k^{n-\frac{1}{2}} - \frac{h\Delta t}{\varepsilon}\frac{1}{S_k}\left(\hat{\rho}_{\text{eng}} S'_k + \hat{\rho}_k \left(S_k - S'_k\right)\right). \tag{13}$$

As a result, there is no need to reduce the time step size by using the new updating formulas (11) and (13) of the voltages.

It is worth mentioning that during the enlargement process, the summation of the new currents $\tilde{i}_{k\text{new}}$ is equal to that of $\tilde{i}_k$: The net current is conservative throughout the cell enlargement, and the continuity equation, i.e., charge conservation, holds during the formulation. Therefore, the proposed circuit-oriented ECT is physically consistent similar to ECT for the conformal FDTD method, in which the total electromotive force is conservative [6].

IV. Numerical Results

The shapes and dimensions of the upper plane of the example PDN are shown in Fig. 3(a). The plane has the non-orthogonal contour which includes circular arc. The conformal meshes of the plane is also illustrated in Fig. 3(b). In this case, each cell is 2 mm $\times$ 2 mm, and the irregular cells exist around the circular arc. We use $\varepsilon = 4.0\varepsilon_0$, where ε_0 is the vacuum permittivity. A current source is appended at the bottom-left corner of the plane, and we observe the voltage waveform at the top-right corner.

TABLE I
CPU time and speed-up ratio in the transient analysis

Method	Δt(ps)	CPU time (s)	Speed-up
Conformal + ECT	29.75	0.29	917
Conformal	4.34	1.88	141
Conventional with Δ_{L}	29.75	0.27	985
Conventional with Δ_{S}	2.98	266	1

The waveform results obtained by the conformal equivalent circuit model with ECT, existing conformal equivalent circuit model, conventional equivalent circuit model with the cell sizes of $\Delta_{\text{L}} = 2$ mm and $\Delta_{\text{S}} = 0.2$ mm are plotted in Fig. 4. The conventional model with Δ_{L} uses the orthogonal meshes shown in Fig. 3(b) without subcells: the subcells are filled with the conductor. All circuit models are solved by the explicit leapfrog scheme with the time step size shown in Table I. From Fig. 4, it is confirmed that all results except for the conventional one with Δ_{L} agree well with each other. The CPU times are listed in Table I. From Table I, we can see that the proposed ECT can improve the efficiency of the existing conformal method with the same accuracy.

V. Conclusion

In this paper, the circuit-oriented ECT for the conformal equivalent circuit model has been proposed to avoid reducing the time step size used in the explicit leapfrog scheme. The proposed ECT was physically consistent because the total current is conservative throughout the cell enlargement procedure. The numerical results showed that ECT worked well in terms of the accuracy and efficiency compared with the existing modeling methods.

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