DIRECT DIGITAL SYNTHESIS AND SPUR REDUCTION USING METHOD OF DITHERING

By

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December 2012

ABSTRACT

Many application, including communication, test and measurements, and radar require the generation of sinusoidal signal with high degree of spectral purity. One method for producing source signal with high purity is by using technique of Direct Digital Synthesis. The method of Direct Digital Synthesis for generation sinusoidal signal uses a very simple circuit, it is easy to control, has stable performance, high frequency conversion speed and fine accuracy. The standard approach to implement a Direct Digital Synthesizer is to truncate the output of phase accumulator to reduce the size of lookup table and truncate the output of lookup table to match number of input bits of Digital to Analog Converter. This process generates spurs and degrades the quality of signal at the output of Direct Digital Synthesizer. One way of reducing the spurs in Direct Digital Synthesizer without increasing the size of look-up table is by quantizing the summed output of a dither generator and phase accumulator before sending the resultant multi-bit signal to the lookup table or by quantizing the summed output of a dither generator and lookup table before sending multi-bit signal to the Digital to Analog Converter. By adding the output of dither generator i.e. by adding a pseudo-random sequence to the Direct Digital Synthesizer the truncation spur can be can be randomized and converted to noise throughout the available bandwidth, thereby increasing the floor noise and improving the signal resolution.

ACKNOWLEDGMENTS

I would like to thank Professor Jose Schutt-Aine and Karan Bhagat for their support during my research project

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Motivation

Direct Digital Synthesis is a commonly used technique for sinusoidal signal generation in modern radio frequency applications and test equipment. The ability to quickly and directly modify the frequency tuning word (FTW), enables the Direct Digital Synthesizer (DDS) topology to offer the fastest frequency jumping and the finest frequency tuning resolution of any technology available today in a completely digital environment. As a result, DDS has found wide application in the fields of communications and test and measurement equipment. However, the performance of a DDS is limited by errors in the signal generation, most notably phase noise and periodic signal generation errors which manifest as spurs in the frequency domain. As has been the tendency in other technology industries, we look to improve the performance of a DDS by adding a pseudo-random sequence to DDS and take advantage of the fact that pseudo-random sequencing will randomize the spurs and improve the signal quality.

The purpose of the thesis is to examine the benefits of method of dithering to improve the quality of the output signal. In doing so, the thesis first goes over the details of the normal DDS and common types of error that occurs in DDS. It then goes into the mechanism of implementing DDS on the FPGA (Field-Programmable Gate Array) and discusses the results obtained by implementing DDS on FPGA. It also covers the method

of dithering to reduce the spurs in DDS to improve the signal quality, where it discusses implementation of DDS with the dithering source on FPGA and limitations of using technique dithering. It is our hope that this thesis will serve both as a guide to the advantages and limitations of using a DDS in a real system and as a survey of the potential benefits of using the technique of dithering to improve performance in signal generation system.

1.2 Outline

The thesis is organized as follows: Chapter 2 provides an introduction to the basic structure of a DDS, discusses spurs produced by the DDS and advantages of the DDS. Chapter 3 includes the implementation of basic DDS on an FPGA and results obtained by simulating DDS with virtex 6 FPGA. Chapter 4 discusses technique of dithering, it includes discussion about two ways of adding pseudo-random sequence to the DDS. It also includes discussions about generation of pseudo-random sequence and comparison of DDS with dithering and basic DDS. Chapter 5 concludes with a general discussion about the DDS and the effectiveness of using dithering in DDS for improving the system performance and provides some commentary on the possibilities of future work.

CHAPTER 2

BACKGROUND

2.1 Structure of the DDS

With the widespread use of digital techniques in instruments and communication systems, a digitally controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis [1]. The basic structure of DDS shown on Figure 2.1 was first introduced in 1971 by Tierney, Radar and Gold [2]. The basic structure of DDS consists of five essential components: a source clock, phase accumulator (PA), a look-up table (LUT), a digital-to-analog converter (DAC) and a reconstruction filter [1, 3]. At every clock cycle, the PA which is effectively a counter increments itself by the amount of the frequency tuning word (FTW). The phase value stored in the PA is read by the LUT and converted to a corresponding sine value through use of sine LUT. The discrete sine amplitude generated by LUT is passed to DAC, which converts it to analog output. At every clock cycle, as phase value is incremented by FTW, the amplitude output steps through the sine LUT generating the desired analog sinusoidal signal. The amplitude of the generated sine wave can be set by digitally scaling the input of the DAC or by a physical attenuator at the output and the signal frequency can be varied by chancing the value of FTW. A larger value of FTW results in the PA moving through the period of the LUT more quickly, yielding higher frequency of output sine wave, while a smaller value of FTW results in the PA to move

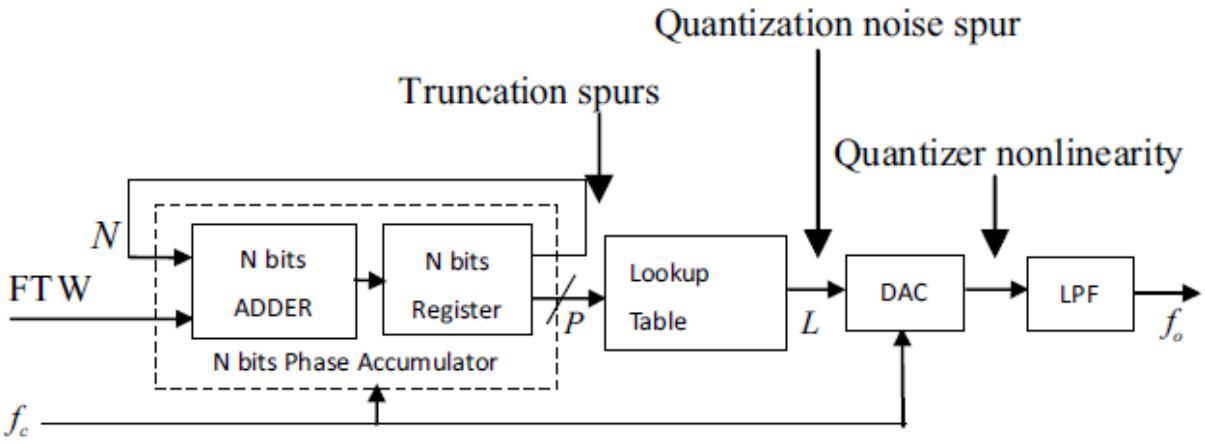

Figure 2.1: Basic Structure of Direct Digital Synthesizer [3]

through the period of the LUT slowly, yielding a lower frequency of the output sine wave. The maximum frequency of output sine wave is determined by its source clock frequency and limited by the Nyquist constraint to one half the clock frequency and by cutoff frequency of the lowpass reconstruction filter at the output [3].

The following subsections of section 2.1 discuss each component of basic DDS structure shown in Figure 2.1

2.1.1 Source Clock

The source clock is very important part of a DDS system. It is generally a clock with high spectral purity, similar in quality to that which would be used as the local oscillator of a receiver [3]. The source clock drives the PA and the DAC, so that the phase and the output of the DAC are synchronized.

2.1.2 Phase Accumulator (PA)

A phase accumulator is the heart of the DDS system. The phase accumulator is basically an N-bit overflowing counter that stores the digital phase of the output signal. PA as shown in Figure 2.2 consists of an N-bit adder and a register. At every clock cycle its value is added to FTW and fed back to itself. The 2^N possible values of the PA map to the phase of sinusoid uniformly distributed from 0 to 2π [3]. As shown in Figure 2.3, as the value of the FTW is added at every clock cycle the register overflows and new period of output sinusoid begins. This gives rise to a sawtooth waveform for the output of the PA. The output frequency of the output sinusoid for a given value of FTW is given by

$$f_{out} = \frac{f_{clk} \times FTW}{2^N} \tag{2.1}$$

which holds as long as the Nyquist criterion

$$f_{out} \leq \frac{f_{clk}}{2} \tag{2.2}$$

is satisfied [3].

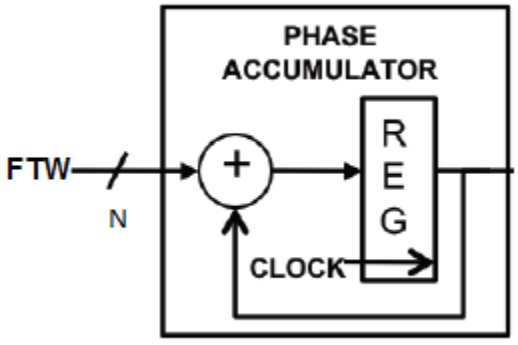

Figure 2.2: Phase Accumulator [3]

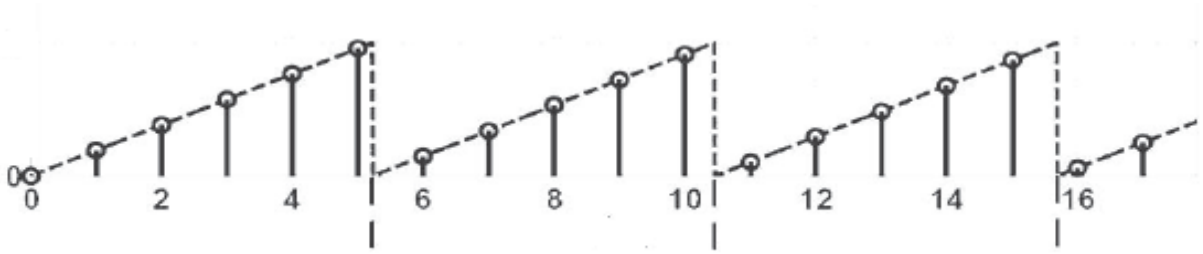

Figure 2.3: Output of Phase Accumulator

As we can observe from equation (2.1), the output frequency of the DDS depends on the FTW. So by finely adjusting the value of FTW at one input clock cycle we can observe the phase continuous output sinusoid at the next clock cycle, enabling nearly instantaneous frequency tuning [3].

2.1.3 Look-Up table (LUT)

The LUT converts the phase output of the PA to the corresponding amplitude on a sinusoid given by

$$f(n) = \sin(2\pi \frac{FTW}{2^N} n) \tag{2.3}$$

where n is a sample number incremented at every clock period ($t = nT_{clk}$). A LUT can be explained using a "phase wheel." As shown in Figure 2.4, visualize the sinusoid wave oscillation as a vector rotating around a phase circle. Each point on the phase circle corresponds to the amplitude of a sinusoid wave. As the vector rotates on the wheel a corresponding sinusoid is generated. One revolution around the phase wheel represents a complete period of a phase wheel. Since the output of the PA is defined by a sawtooth

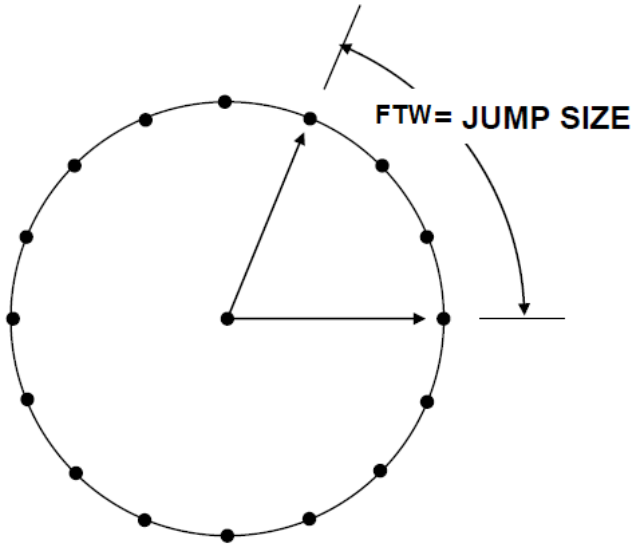

Figure 2.4: Phase wheel [1]

wave, as the value of the phase increases linearly the vector rotates around the phase wheel at a constant speed until the overflow occurs where the sine wave completes one period. The speed of rotation of the vector around the phase wheel is determined the value of the FTW. If the value of the FTW is smaller the vectors rotates around the phase wheel slowly and the output frequency is small, while if the value of the FTW is large the vector rotates around the phase wheel faster and the output frequency is large. The number of discrete phase points contained in “phase wheel” is determined by the resolution, N of the PA [1]. In, practice, the LUT is a read-only memory (ROM) that performs the function in Equation 2.3 to a precision determined by the designer [3]. In practice, the value of N is 32 which require the depth of the ROM to 4294967296. This would require very large size of the ROM, which is a very impractical for a system like

DDS. Therefore, the input phase to the LUT is truncated to a smaller number of bits which leads to spurs in the DDS. In addition, to decrease the size of the ROM, the DDS architecture exploits the symmetrical nature of a sine wave and utilizes mapping logic to synthesize a complete cycle for ¼ cycle of data stored in the ROM [1]. The details regarding this technique for reducing the size of ROM will be discussed in Chapter 3. The output of a LUT will be a discrete sinusoidal wave.

2.1.4 Digital-to-Analog Converter (DAC)

The output of a LUT is connected to the D-bit DAC, which generates an analog value corresponding to the D MSBs of the LUT output amplitude [3]. Since, the output of a LUT is truncated to D-bits it contributes to the spurs in the DDS. In addition, spurs also arise in the DDS due to non-linearities in the DAC. Spurs in the DDS will be discussed in the section 2.2.

2.1.5 Reconstruction Filter

A lowpass reconstruction filter is added at the end of the DDS to smooth the output of the DAC and to limit the output frequency to under half of the frequency of the source clock in order to satisfy the Nyquist criterion. Typically, the cutoff frequency of the filter is set to 40 percent of the source clock frequency to allow for the transition band to be below the Nyquist frequency [1, 3].

2.2 Spurs in the DDS

Due to inherent architecture of the DDS, the sinusoidal signal produced by the DDS in not a perfect sinusoid. Therefore, there is always a difference between the output signal and the ideal signal. There are three different kinds of spurs associated with the DDS:

- Phase Quantization Spurs
- Quantization Spurs
- Quantizer Non-Linearity Spurs

The following subsections provide detailed descriptions of the different spurs associated with the DDS.

2.2.1 Phase Truncation Spurs

The phase truncation spur is a primary source of spectral impurity inherent to the DDS. In order to obtain a high-frequency resolution at the output, the output width of the PA will be so wide that the size of the ROM will become unmanageable. The phase truncation spur is caused due to truncation of LSBs of the output of the PA to reduce the size the ROM to a manageable size. For example, if the DDS architecture has a PA of 32 bits and if output of the PA is connected to a equally sized ROM, it would require 5 gigabytes of the ROM which would be very enormous and power consuming for most of the systems. Now, truncating the 18 LSBs of the output of the PA will require the size of the ROM to be 8 kilobytes, thereby reducing size of the ROM by a factor of approximately one half megabytes. A ROM of 8 kilobytes consumes lower power and it is very small size compared to a 5 gigabytes ROM. Although phase truncation is

practical, it creates periodic error that manifests itself as spurs in the frequency domain [3]. In addition, limited precision of the input of a LUT contributes a quantization spur [3].

2.2.2 Quantization Spurs

The input of a DAC is always limited to a certain number of bits and the bit width for the output of a LUT is not always equal to the bit width of input of a DAC. Therefore, the output of a LUT is truncated to match the number of bits of input to the DAC, thereby losing important information from the discrete sine wave. Therefore, by quantizing the output of the LUT to match the number of bits to input of the DAC introduces quantization spurs to the DDS.

2.2.3 Quantizer Non-Linearity Spur

The DAC in a DSS structure is a non-linear device and it introduces the new inter-modulation spurs and degenerates the truncation and quantization spurs [2]. Although, it is possible to predict the spurs due to phase truncation and quantization by using different mathematical methods, it is hard to predict inter-modulation spurs and degenerated spurs which depend on the non-linearity property of the DAC. Therefore, to reduce the quantizer non-linearity spurs, resolution of the DAC has to be improved.

Therefore, the truncation spurs and quantization spurs discussed already are inherent to a DDS structure and they can be easily determined. Many methods have been proposed to suppress the truncation and quantization spurs, such as compromise between the size of the LUT and the width of the accumulator, to add the additional random

dithering signal to the output of LUT or the output of the PA and many more. Quantizer non-linearity spur is not related to the structure of the DDS but it is related to the non-linearity property of the DAC. The quantizer non-linearity spur can only be suppressed if the resolution of the DAC is improved.

2.2.4 Advantages of the DDS

A Direct Digital Synthesizer also known as numerically controlled oscillator (NCO) has many advantages over traditional analog oscillators. Advantages of the DDS are as follows:

- Micro-hertz tuning resolution of the output frequency and sub-degree phase tuning capability using complete digital control [1].
- Extremely fast “hopping speed” in tuning the output frequency, phase-continuous frequency hops with no over/undershoot or analog-related loop settling time anomalies [1].
- The DDS digital architecture eliminates the need for the manual system tuning and tweaking associated with component aging and temperature drift in analog synthesizer solutions [1].
- The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled, and minutely optimized under processor control [1].

Therefore, these described advantages of the DDS make it attractive to systems that are controlled remotely and the systems that require high-precision frequency tuning.

In addition, due to the digital nature of the DDS, DDS is a perfect choice for the systems that are mostly digital.

CHAPTER 3

IMPLEMENTATION AND RESULTS

The basic DDS described in Chapter 2 was implemented with Xilinx Vertex 6 Field Programmable Gate Array (FPGA). The following sections describe how the DDS was implemented on an FPGA and results obtained by performing simulation with Xilinx Virtex 6 FPGA.

3.1 Implementation on a FPGA

The design of a DDS implemented on the FPGA only consists of an Accumulator and the look-up table because virtex 6 FPGA does not have an inbuilt digital-to-analog converter and low pass filter. The following subsections describe how the accumulator and look-up table were implemented on an FPGA.

3.1.1 Accumulator

The accumulator consists of an adder and a register. Xilinx Design Suite 13.1 has inbuilt intellectual property (IP) for an accumulator consisting of an adder and a register. The accumulator was implemented using accumulator IP with inputs such as a clock and 32-bit FTW and output as 32-bit number.

3.1.2 Look-Up Table

The look-up table is very a important part of a DDS, functions to convert the phase values to the sine amplitudes. To reduce the size of a look-up table, output of the PA is truncated to 14 bits by truncating 17 least significant bits (LSBs) of output of the PA. By truncating 17 LSBs of the output of the accumulator, the size of the look-up table is reduced by a factor of $\frac{1}{32768}$, which reduces the memory from approximately 4 gigabytes to 16 kilobytes. The size of the look-up table was further reduced by storing only a quarter of the sine wave, which reduces the size of the ROM to 4 kilobytes. The look-up table was implemented using block memory IP of Xilinx ISE Suite 13.1 by setting the clock, memory enable and 12-bit truncated output of the PA as input and 12-bit output representing sine amplitude.

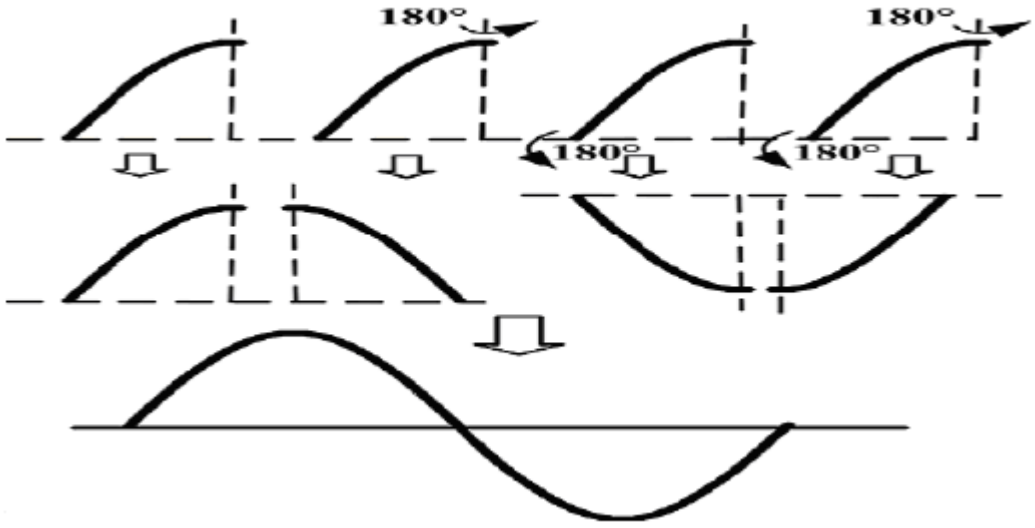

Figure 3.1: Logic behind forming Sine Wave

Since only a quarter of a sine wave was stored in the look-up table, logic has to be implemented to convert the quarter sine wave to a complete sinusoidal signal. Figure 3.1 shows the complete logic behind retrieving the complete sine wave from a quarter of a sine wave stored in look-up table. Since the 17 LSBs were truncated, 14 most significant bits (MSBs) 31 down to 28 were used to form a complete sinusoidal signal. As described previously, 12 bits are sent as input to the ROM to read the right sine value. Therefore, bits 29 down to 18 were used to read the value of the quarter sine stored in the look-up table. The remaining two bits, 31 and 30, were used to decide the direction and sign of a sine wave. For the sine wave, 00 represents first quadrant, 01 represents the second quadrant, 10 represents the third quadrant and 11 represents the fourth quadrant.

Therefore, at every clock period FTW gets added to itself in the PA and output of the PA is truncated to 14 bits and 12 LSBs are sent to look-up table. Twelve LSBs are used to read data from the look-up table and 2 MSBs determine the direction and sign of the quadrant of a sine wave obtained from the LUT, which is thereby used to form complete sine wave.

3.2 Results

DDS described in Section 3.1.1 was implemented on Xilinx virtex 6 FPGA using Verilog and then it was simulated using modelsim. This section describes the results that were obtained by simulating the DDS with virtex 6 FPGA.

Figures 3.2 and 3.3 show the simulation results of the PA and the LUT for FTWs of 1048576 and 1400000 respectively.

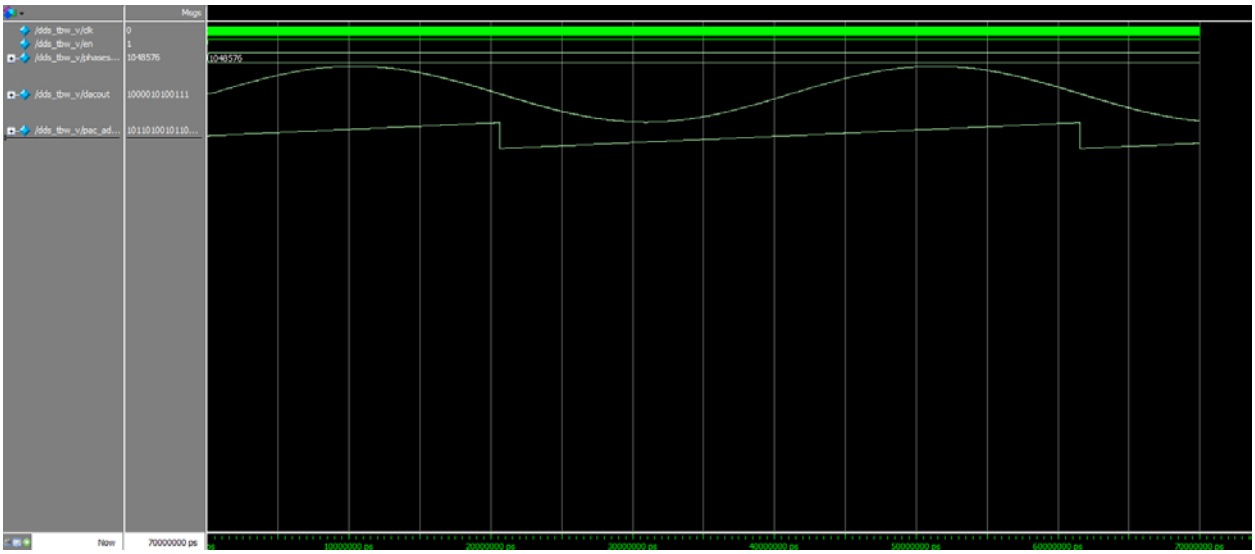

Figure 3.2: Simulation for FTW = 1048576

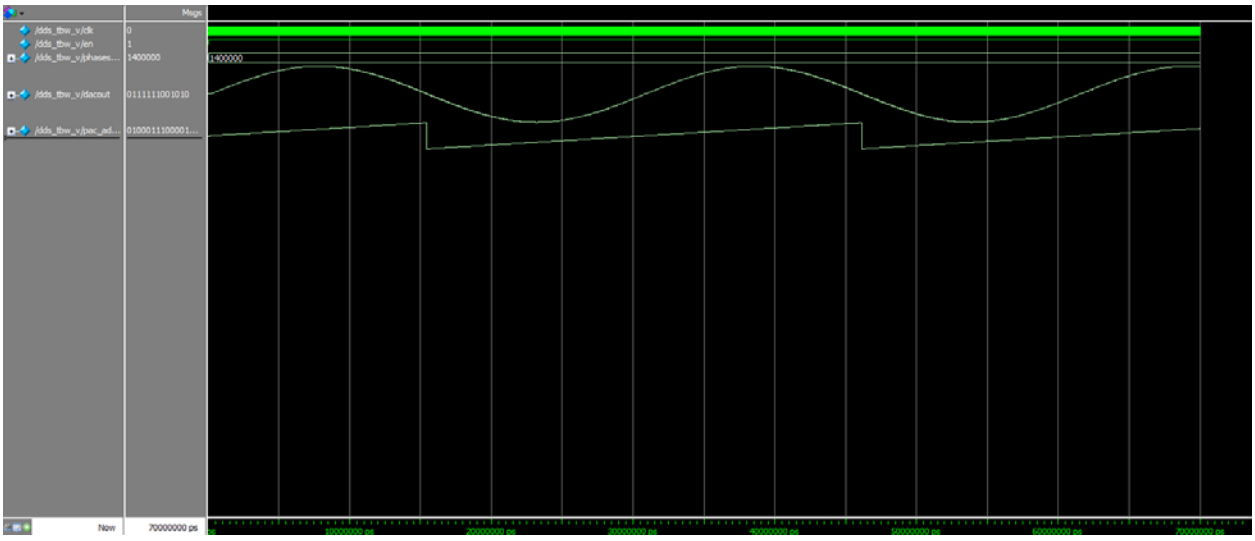

Figure 3.3: Simulation for FTW = 1400000

The topmost plot in the figures 3.2 and 3.3 is the source clock. The FTW, LUT output and PA output are shown as the second, third and fourth plots respectively in figures 3.2 and 3.3.

The simulations were performed at a clock frequency of 100MHz with simulation time of 700000000 ps. As shown in figures 3.2 and 3.3, the simulations are performed for constant value of FTW. The fourth plot on these figures is the plots for the output of PA. As it was described in Chapter 2, a PA is a 32-bit overflowing adder connected to a 32-bit register. The sawtooth waveform of the output PA describes the overflowing property of the adder in the PA. As the value of the FTW gets added to itself, the adder increments itself until it reaches its maximum values and then it resets to zero. In addition, we can also observe that the output of the PA resets itself at every period of output sine wave. This can be explained by using the “phase wheel” that was discussed in Chapter 2. Visualize a phase wheel, and as the phase increases the vector rotates around the phase wheel forming the sine wave. One complete rotation around the phase wheel produces a complete period of a sine wave, therefore at the end of a period of sine wave, the phase should also reset to zero. This explains the sawtooth waveform of output of a PA.

In addition, as we can observe from figurse 3.2 and 3.3, the frequency of the sine wave with FTW equal to 1400000 is higher than that of sine wave with an FTW of 1048576. At clock frequency of 100 MHz with FTW of 1048576, a sine wave of frequency 24.41 KHz can be achieved and with FTW of 1400000 a sine wave of frequency 32.59KHz can be achieved.

Furthermore, figure 3.4 shows very important advantage of a DDS. In this case, the value of FTW is linearly increased for complete runtime of the simulations. We can observe that the phase of the sine wave does not change when the value of FTW is changed.

Therefore, the DDS was implemented on an FPGA by using the inbuilt IP of Xilinx ISE suite 13.1, and the LUT was implemented by only storing a quarter of the sine wave and using some logic to form the complete sine wave from the quarter sine wave stored in the LUT. Then simulations were performed by using different values of FTW and for linearly varying FTW. Three different plots, two for different values of FTW and one for linearly varying FTW were analyzed to show that the frequency of the output sine wave can be changed by changing the value of FTW and to show that the phase of the output sine wave does not change when the value of FTW is changed linearly, which is one of the major advantages of using a DDS.

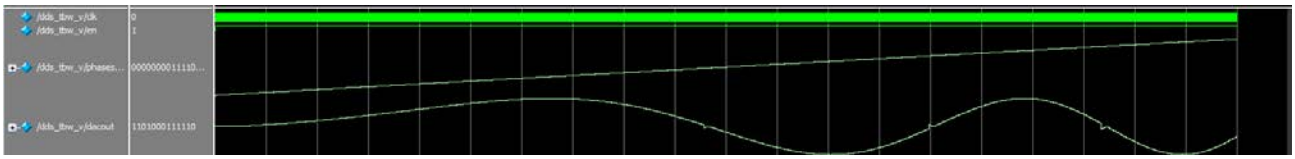

Figure 3.4: Simulation for linearly varying FTW

CHAPTER 4

DITHERING IN THE DDS

Many systems in communications and in test and measurements require a sinusoidal wave with high spectral purity. But the basic DDS discussed in Chapter 2 does not output a sinusoid with high spectral purity. As discussed in Chapter 2, there are many different kinds of spurs that are associated with a DDS system, namely

- Truncation Spur
- Quantization Spur
- Quantizer non-linearity spur

There are many ways of reducing the spurs in the system; one of the very effective ways of reducing spurs in the system is by using the method of dithering. Dithering is a technique of adding a pseudo-random sequence in a DDS to reduce deterministic spurs (i.e. truncation spurs and quantization spurs) in the system. By adding a pseudo-random sequence in a DDS, the spurs related to truncation and quantization are randomized based on where in the system the sequence is added, thereby reducing the spurs and increasing the floor noise in the system. The following sections in this chapter discusses two different ways of adding a pseudo-random sequence in the system, design of a pseudo-random sequence generator, and comparison between the basic DDS and the DDS with pseudo-random sequence generator.

4.1 Ways of Dithering

There are two ways of adding pseudo-random sequence to a DDS. One is adding a pseudo-random sequence before the LUT and other is adding pseudo-random sequence after the LUT. Following two sections discusses the two ways of adding pseudo-random sequence to the DDS.

4.1.1 Adding Pseudo-random sequence before the LUT

As shown in figure 4.1, a pseudo-random sequence of M-bits is added before the LUT. According to the principle by adding the random uniform density M-bit dither signal in the least significant M-bit to the N-bit number generated by the PA before the LUT, the size of LUT can be reduced without changing the resolution of the output signal [4]. The output of the adder is truncated to P-bit before passing it to the LUT. Since P < N, the size of the LUT is reduced by a factor of 2^{N-P}. Truncation and quantization spurs are produced in the DDS due to truncation of the output of the PA or the LUT before sending it to the next block. Since the output of the PA and the LUT are periodic, spurs produced these blocks are also periodic unless it is Randomized somehow [4]. By adding

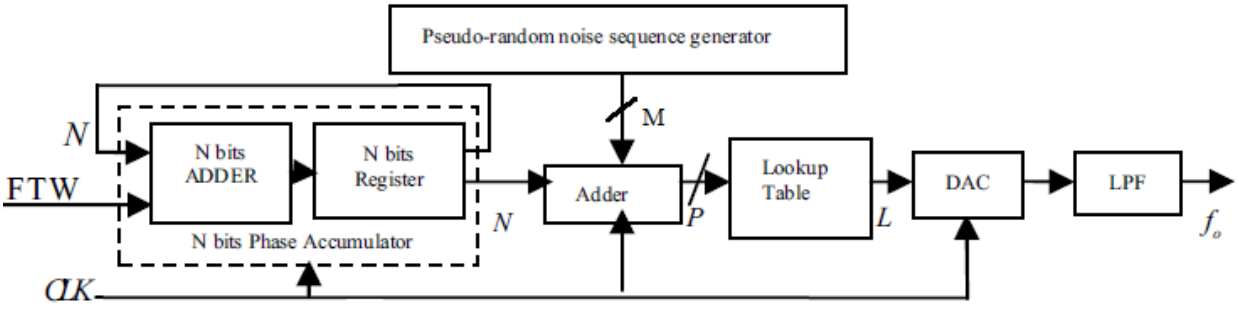

Figure 4.1: Adding Pseudo-random sequence before Look-Up Table [2]

a random sequence prior to the phase truncation randomizes the phase noise resulting in a more desirable white noise spectrum at the output, thereby improving spectral purity of the output sinusoidal signal. Therefore, adding a pseudo-random sequence before the phase truncation randomizes the spurs without increasing the size of the LUT.

4.1.2 Adding Pseudo-random sequence after the look-Up table

When the digital amplitude of the sine wave is converted to analog form, spurious noise is created due to a quantization effect. It is known that for any digital-to-analog conversion there is an error of $\pm\frac{1}{2}$ the smallest quantization step or Least Significant Bit (LSB) for base digital data, for the DAC input data as it is translated to discrete analog amplitude levels [5]. For typical digital conversions, the spurious peaks are found at certain predictable frequencies. These peaks are found to have an energy level that falls roughly 6 dB per DAC input bit, down in energy level from a fundamental output frequency [6]. Therefore, to decrease the spurious noise peaks the resolution of the DAC has to be improved. However, increasing the DAC resolution will increase the complexity of the DAC which leads to slower speed, increased power consumption and higher cost, which are not desirable in any communication systems.

As shown in figure 4.2, the pseudo-random number generator is connected in series with scalar element for receiving the pseudo-random number and for scaling the pseudo-random number to a predetermined amount. The output of the scalar element and the LUT are connected to the adder, the output of which is sent to the DAC after truncation.

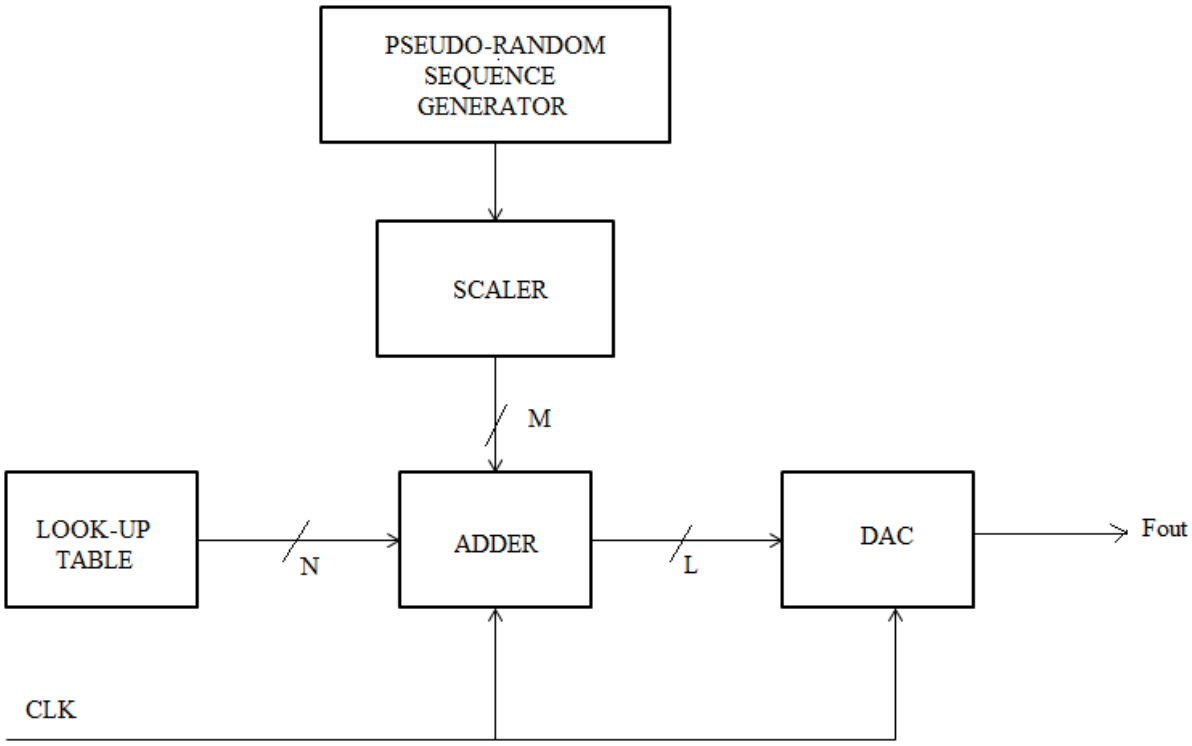

Figure 4.2: Adding Pseudo-Random Sequence after Look-Up Table

For this method of dithering, pseudo-randomly varying numbers are scaled to a predetermined magnitude and added to each of the sine amplitude number during transfer to the DAC. The resultant addend is then truncated before it is sent to the DAC. By adding a pseudo-randomly varying number before the LUT, the quantization error caused due to truncation of sine amplitude during its transfer to DAC is randomized, thereby improving spectral purity of the output sinusoidal signal.

Therefore, pseudo-randomly varying the number can either be added before the LUT or after the LUT. By adding it before the LUT the size to LUT can be decreased without detoriating the resolution of the output, while on the other hand if it is added after

the LUT the quantization effect due to truncation of sine amplitude is reduced. Therefore, by pseudo-randomly adding number to the DDS the spurs produced due to phase truncation and quantization can be reduced and resolution of the output can be improved at the cost to added floor noise in the system.

4.2 Pseudo-random sequence generator

Figure 4.3 shows schematic diagram of a 3-bit feedback shift register pseudo-random generator. The pseudo-random sequence generator consists of a 10-bit shift register which may be formed of a plurality of flip-flops 64 to 82, which are connected in cascaded fashion. The 3-bit dither signal is tapped from output of flip-flops 68, 74 and 82. The input of XOR gate 62 is coupled to output of flip-flop 76 and 82 and output is coupled to input of flip-flop 64. The pseudo-random sequence is operated at clock frequency $f_{s,}$ thereby producing a 3-bit pseudo-random sequence at sampling rate f_s. A very important note about any pseudo-random generator is, a dither generaor provides a pseudo-random sequence of L-bits whose period is at least 2^L samples and whose probability density is uniform, in order for the phase noise produced by truncation to be "whitened" [4].

4.3 Comparision to the basic DDS

It is very important for the communication systems to produce a sinusoidal signal with high spectral purity. Since the basic DDS does not produce a sinusiodal signal with high spectral purity due to truncation and quantization spurs, it is required that other method be used to improve the specral purity of DDS. For the present thesis the dithering technique is discussed which is used to reduce the spurs in the DDS. Present section

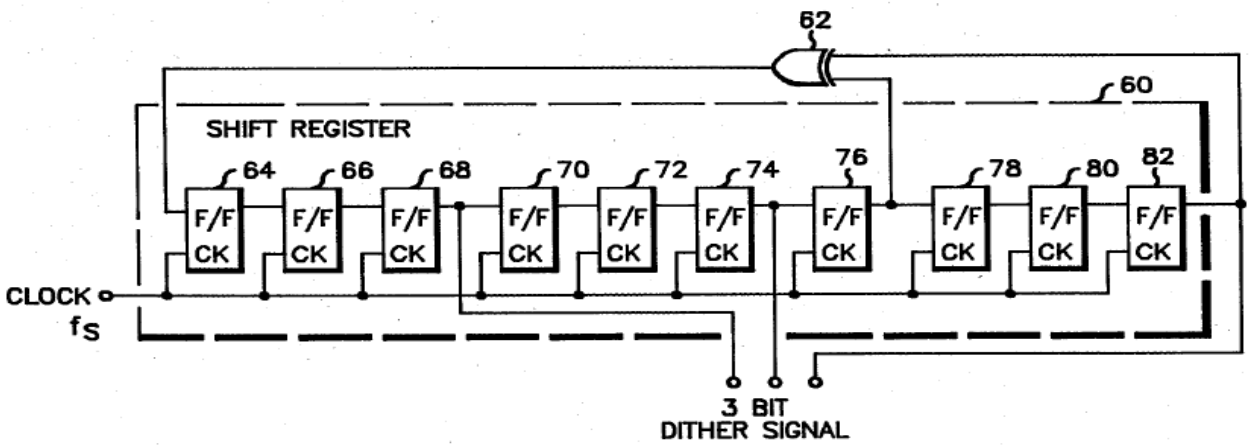

Figure 4.3: Pseudo-Random Sequence Generator [4]

compares the basic DDS to the DDS with the pseudo-random generator.

A very important advantage of using the method of dithering is that it reduces spurs in the output during direct digital frequency synthesis with a minimum complexity of the circuit. Figures 4.4 and 4.5 illustrate the advantage of using technique of dithering to reduce spurs in DDS. Figure 4.4 shows the power spectrum of a sine wave with a frequency of 4300 Hz having a phase truncation of 5 bits. The plot on the left shows the power spectrum of the basic DDS, where it can be observed that the fundamental frequency is at 4300 Hz and phase truncation spur at 3900 Hz with a power of -25 dBc (decibels relative to the carrier). The plot on the right shows the power spectrum of a sine wave with same specifications but in this case a pseudo-random sequence is added to the DDS. It can observed that the spur at 3900 Hz is reduced by 25 dBc when the pseudo-random sequence is added to the DDS. Similar observations can be made from the plots in figure 4.5 where the phase is truncated by 8 bits. The figure on the left shows a power spectrum of the sine wave with a frequency of 2000 Hz, where the -40 dBc spur due to

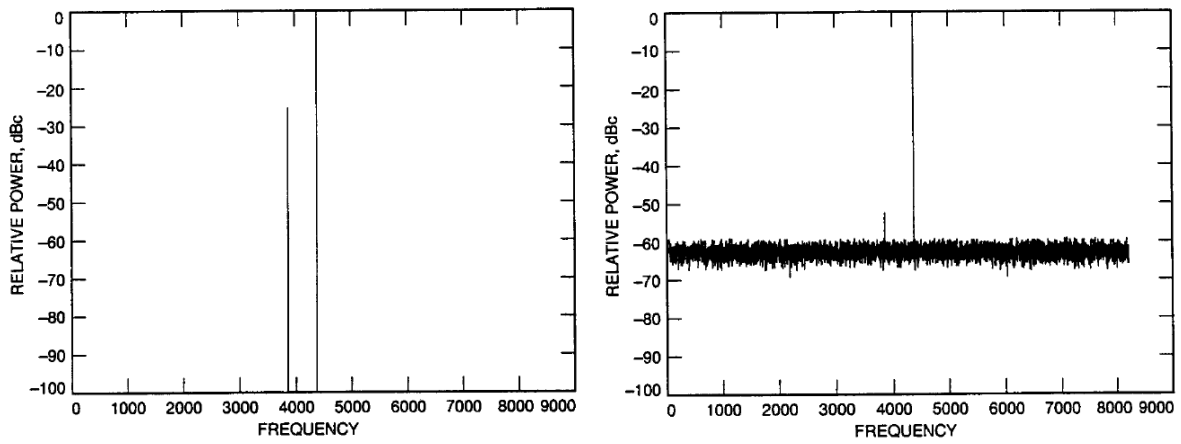

Figure 4.4: Power spectrum of 5-bit phase truncated sine wave without dithering (Left) and with dithering (Right) [6]

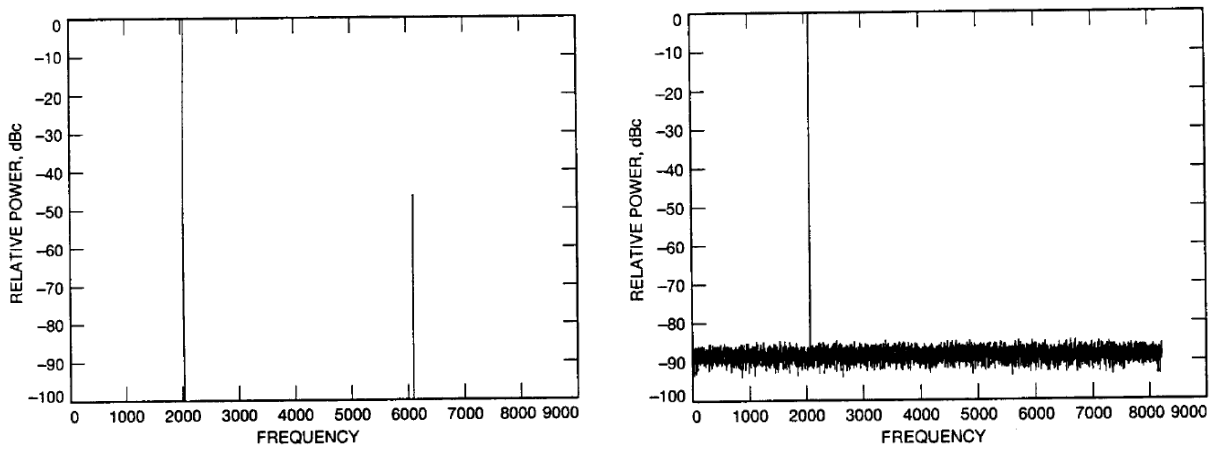

Figure 4.5: Power spectrum of 8-bit phase truncated sine wave without dithering (Left) and with dithering (Right) [6]

truncation can be observed at 6050 Hz. On the other hand, the plot on the right shows a power Spectrum of the sine wave with dithering where the spur at 6050 Hz is completely disappeared.

As oppose to the advantage of reducing the spurs in the DDS, it can be observed from the plots on the right of figures 4.4 and 4.5 that the floor noise of the output sine wave has increased due of the addition of the pseudo-random sequence into the system which is disadvantage of using the technique of dithering to reduce spurs in the DDS.

Therefore, on the one hand the technique of dithering can be used to reduce the spur in the DDS without largely increasing the complexity of the circuit but on the other hand it is the cost of adding the pseudo-random sequence to the DDS by increased floor noise in the output of DDS. Thus, the technique of dithering can only be used in the system which does not require very high spectral purity at the output.

CHAPTER 5

DISCUSSION

5.1 Conclusion

The objective of the present thesis is to introduce Direct Digital Synthesizer (DDS) also known as numerically controlled oscillator (NCO) and discuss the basic DDS in detail. The part of the thesis included implementation of a basic DDS on FPGA and results obtained by simulating DDS with virtex 6 FPGA. Lastly, technique of dithering was discussed which is used to reduce truncation and quantization spurs in the DDS.

Direct Digital Synthesis is a technique of using digital signal processing blocks as a means to generate a frequency and phase-tunable output signal referenced to a fixed precision clock source. It consists of a PA, LUT, DAC and Low-Pass Filter (LPF). At every clock period, the FTW gets added to output of the PA and output of the PA is sent to LUT. The LUT changes the phase to a discrete sine amplitude, which is the converted to an analog sine wave by the DAC. It is then passed through the LPF to remove high-frequency elements from the output, thereby producing high-resolution output sine wave.

Practically, the output of PA is truncated to realize the size of the LUT and output of the LUT is truncated to match the bit-width of input of the DAC. By truncating the output of the LUT and the DAC, resolution of the output is reduced. There are many solutions to improve the resolution of the output and to reduce the spurs in the DDS. For

the present thesis technique the of dithering was discussed, which is a method of introducing a pseudo-random sequence on the DDS so that the spurs caused due to truncation are randomized and the resolution of the output signal is improved at the cost of increased floor noise.

5.2 Future Work

For the present thesis, the basic DDS with only ¼ sine wave stored in the LUT and the phase truncation was designed with Verilog and simulated with a virtex 6 FPGA. As discussed in Chapter 4, in future dithering source should be designed with Verilog and its output should be added before and after the LUT and tested individually. The results obtained by testing should be compared with the results of the basic DDS and further improvement in spectral purity should be made by using different techniques.

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