Latency Insertion Method for the Analysis of Steady State On-Chip Power Distribution Networks and Transient Simulation of Lossy Interconnects

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Introduction

Process scaling has led to a significant growth in the number of devices on a chip. Consequently, the length and density of interconnects has increased dramatically. As a result, present day circuit designers are facing the problem of analysis of networks with millions of nodes. Traditional matrix-vector product based circuit simulators such as SPICE are not computationally efficient for analysis of large circuit problems. The latency insertion method (LIM) was proposed as an alternative transient simulation technique to efficiently model large networks. The method is based on a finite-difference formulation; it solves circuit equations in time domain. The algorithm makes use or introduces reactive latency in all branches and nodes of a circuit to generate update algorithms for the voltage and current quantities. Because of its linear numerical complexity it greatly outperforms conventional matrix-based methods and enables analysis of very large networks [1].

One of the examples of extremely large networks, which are hard to analyze using conventional methods, is power grids. Recently LIM was successfully applied to the transient analysis of on-chip power distribution networks (PDN) [2]. In this paper we show that LIM is also capable of efficient steady state (IR drop) analysis of a PDN.

Integrated circuits are not only becoming increasingly complex, they are also being operated at higher frequencies. As frequencies of operation get well into the gigahertz range, frequency-dependent effects can no longer be ignored in the analysis of circuit interconnects. In this work we demonstrate that LIM algorithm can be extended to incorporate frequency dependent behavior of circuit elements in the simulation.

Latency Insertion Method (LIM)

The Latency Insertion Method (LIM) [1] treats a network as a grid composed of nodes interconnected with branches. Each branch is represented as a combination of a voltage source, an inductor, and a resistor in series. Each node is modeled as a combination of a current source, a conductance, and a capacitor to the ground. The method solves time-domain circuit equations for branch currents and node voltages in the same way as the Finite-Difference Time-Domain (FDTD) method [3] solves Maxwell's equations for electric and magnetic fields.

On-chip Power Distribution Network (PDN) Analysis

In present day power grids large amounts of current are distributed through large scale networks at low voltages, which causes significant voltage drop (IR drop) on the grid, seriously compromising the performance of the chip. Therefore, efficient and accurate analysis of the IR drop in power distribution network becomes a critical issue.

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Following [4] a power grid at DC can be represented as a regular network where power supplies are modeled as independent constant voltage sources, and current sources represent constant leakage currents through transistors. Metal wires and vias can be modeled as a regular two-dimensional grid of linear constant resistors. A basic circuit that represents a segment of a large power grid is shown in Fig. 1. If we set $R_b = 1\ \Omega$, $I_D = 0.1$ A, $V_0 = 1.8$ V, then voltage at node 5 is 1.7125 V.

The circuit in Fig. 1 does not contain latency; therefore, we cannot directly apply LIM to its analysis. In order to simulate such circuit we need to implement the augmented network, adding inductor to every branch and capacitor at every node excluding the source nodes. The modified network can then be simulated with LIM. Results of the simulation are shown in Fig. 2. Figure 2 demonstrates that voltage at node 5 quickly converges to the correct value.

LIM was used for simulation of several large circuits that represented power grid networks of different sizes. Runtimes of the LIM simulations were compared to the ones of Random Walk method. Computations using Random Walk method were carried out on a Linux workstation with 2.4 GHz CPU and 2-GB of RAM [4]. For the simulation with LIM a Windows workstation with the same characteristics was used. All the algorithms were implemented using C++. Results are summarized in Table 1.

Table 1: Runtime comparison between Random Walk method and LIM

Number of Nodes	Random Walk	LIM
	CPU Time (min:sec)	CPU Time (min:sec)
10K	0:10	0:00
250K	12:21	0:18
1M	43:47	1:16

From Table 1 we observe that LIM significantly outperforms the Random Walk algorithm.

Transient Simulation of Lossy Interconnects

At high frequencies of operation frequency-dependent effects such as conductor loss due to skin effect and substrate loss in on-chip interconnects become major factors and have to be accounted for in a simulation.

The discrete model used for the representation of interconnects with frequency-dependent parameters is shown in Fig. 3. Series elements of the network in Fig. 3 are modified branches of the standard LIM network, parameters of the modified representation change with frequency. Likewise, shunt elements in Fig. 3, represent frequency-dependent nodes.

Branch impedance $Z_{ij}(\omega)$ and node admittance $Y_i(\omega)$ are represented with low-order rational function approximations. Parameters of those models are extracted using vector fitting technique. Update equations for node voltages and branch currents in the time domain are obtained using recursive convolution.

Circuit interconnects that exhibit frequency-dependent behavior can be modeled as lossy transmission lines with frequency-dependent parameters. Figure 4 illustrates the setup used in the simulation: open-ended lossy transmission line is driven by a $50\,\Omega$ pulse source.

At each iteration of the algorithm voltage values at the near and far ends of the line were recorded. Figure 5 shows the results of the simulations: first a lossless case was modeled; then frequency-dependent conductor loss was added to the simulation; and finally frequency-dependent substrate loss was taken into account.

Conclusions

The latency insertion method was applied to the analysis of steady-state on-chip power distribution network. Experimental results show that LIM outperforms the Random Walk method, especially for circuits with large numbers of nodes. Also, expansion of the LIM algorithm to the treatment of networks with frequency-dependent parameters was presented. The ability of the expanded algorithm to model lossy interconnects was demonstrated.

References

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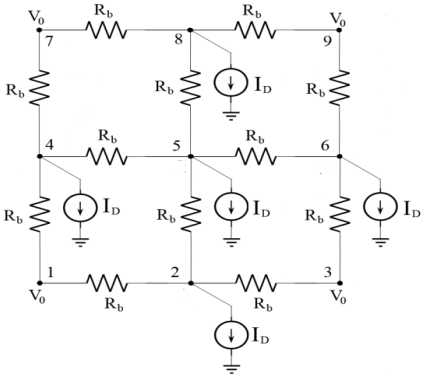

Figure 1. Basic circuit example

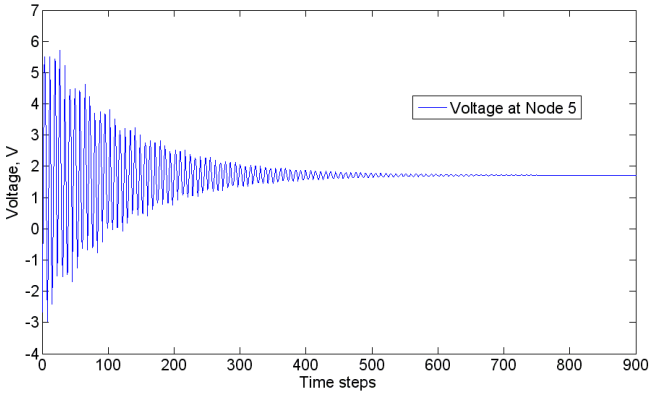

Figure 2. Simulation of the basic circuit

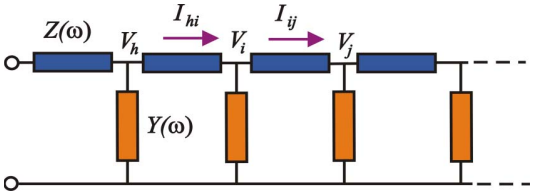

Figure 3. Model of an interconnect with frequency-dependent parameters

Figure 4. Transmission line configuration used in the simulation

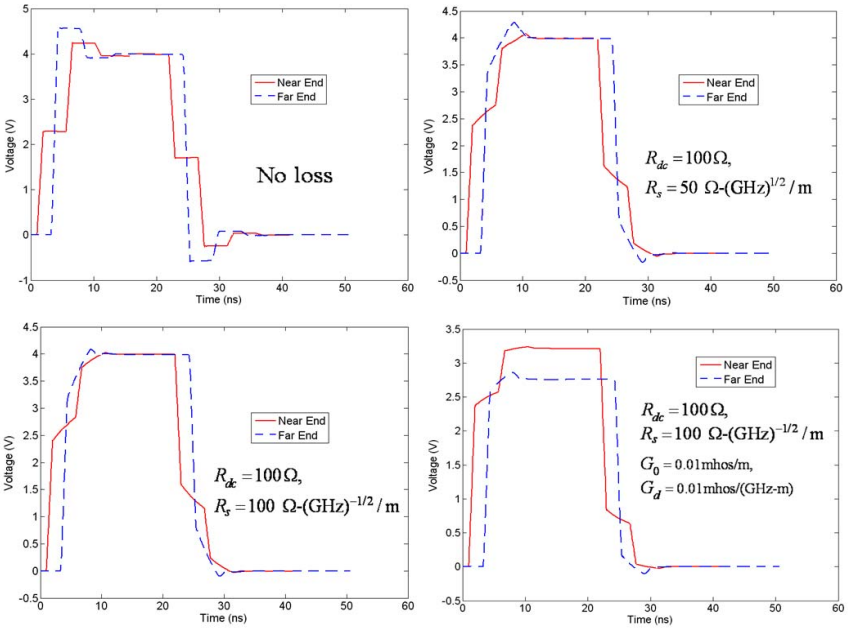

Figure 5. Shape of the pulse at the near and far ends of the line