Application of the Latency Insertion Method (LIM) to the Modeling of CDM ESD Events

Dmitri Klokotov, Vrashank Shukla, José Schutt-Ainé and Elyse Rosenbaum
Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign, Urbana, IL, USA
dklokot2@illinois.edu, vshukla2@illinois.edu, elyse@illinois.edu, jschutt@emlab.illinois.edu

Abstract

In this paper, the application of the latency insertion method (LIM) to the analysis of charged device model (CDM) electrostatic discharge (ESD) events in integrated circuits (ICs) is discussed. LIM is proposed as an alternative to existing techniques commonly used for chip-level circuit simulation of CDM ESD. Such simulators, based on the modified nodal analysis (MNA) method, can underperform in cases that require very large model sizes. LIM was developed specifically for the analysis of fast transient phenomena in very large networks and is more robust and less resource-hungry than conventional methods.

Introduction

Electrostatic discharge (ESD) has become a major consideration in the design and manufacture of integrated circuits (ICs). ESD impacts production yields, manufacturing costs, quality, and reliability of contemporary semiconductor devices. Problems related to ESD events are increasing as the trends continue toward higher speed and smaller device sizes. As the nanoscale CMOS devices are fabricated with thinner gate oxide, ICs become more susceptible to oxide breakdowns. At the same time, more function blocks are being integrated into a single chip, which increases a die size and leads to larger amounts of static charge stored in the body of the circuit, and consequently, higher ESD current and voltage spikes. To avoid device failures due to ESD, preventive measures must be taken. Such measures include providing safe paths for the discharge current to flow off chip by equipping each IC with ESD protection circuitry. Design and placement of such circuitry requires identification of current and voltage distribution during ESD. Therefore, understanding mechanisms of ESD, ability to test, analyze and model ESD events are now crucial parts of the IC design process.

A number of different models have been developed to simulate different ESD conditions that cause device failures. These include the human body model (HBM), the machine model (MM), and the charged-device model (CDM). In this paper we focus on CDM, which is currently the dominant ESD model as it is particularly effective at simulating damage induced by automated equipment, present in every modern manufacturing facility. Also, as the dielectric failure has become more prominent with scaled semiconductor devices, the CDM accounts for the majority of ESD failures during chip manufacturing [1].

The CDM assumes that the IC package is charged either directly via triboelectric effect (i.e., via frictional contact with some material), or due to induction in the presence of an external electric field. One or more package pins (e.g., leads, solder balls) subsequently contact a conductive surface at or near ground potential. The charge stored on the metal parts of the device flows through in a very fast "spark discharge" and causes failures of junctions, dielectrics, and components along the discharge path [2].

Various hardware test setups have been developed and are used to physically replicate real-world CDM failures. In these tests, the electrostatic charge is induced on a device, and then a discharge path is created, emulating the ESD event. Although successful at stress-testing production devices, physical tests often do not provide enough information about the exact mechanisms of ESD. In particular, the effects of substrate resistivity, as well as the cases of failures occurring at internal nodes of a chip, are hard to investigate via test chip design and hardware testing. Circuit simulation presents an attractive time- and cost-effective alternative to physical tests.

Circuit simulations are particularly useful for modeling of the failures at internal nodes of a chip, which occur due to ESD currents flowing through the substrate of an IC. In order to capture the effects of substrate conductivity, a suitable model has to be used to represent the substrate material in a simulation. Since on-chip devices are represented with their circuit models, it is desirable to use a circuit level model for a substrate. Discrete distributed resistive or resistive-capacitive models can be employed to model a substrate material with finite resistivity. However, such representation may result in very large networks since the number of substrate network nodes is related to the number of substrate taps (i.e. Vss bus connections to the substrate) and the number of substrate taps can be very big. The size of such model makes analysis of the circuit with conventional matrix-based methods inefficient or even prohibitive due to prolonged runtimes and excessive memory requirements. In this paper we propose an alternative simulation technique based on the latency insertion method (LIM) [3]. The method is based on the finite-difference formulation similar to the one used by the well-known finite-difference time-domain (FDTD) method [4]. LIM iteratively solves circuit equations for voltages and currents using a time-stepping scheme; therefore, it eliminates the need for large matrix equations employed in modified nodal analysis. The method is particularly efficient at modeling very fast transients, such as those occurring during CDM ESD events. The method enables the simulation of substrate models with very high levels of discretization in a reasonable amount of time; provides access to voltage and current values at any point of a circuit model; and allows mapping of the current distribution in the circuit with very high precision.

The LIM simulation of CDM ESD is based on the circuit representation of the industry-standard field induced charged device model (FICDM) ESD test setup [2]. Although the circuit model emulating the CDM event is uncommon for a

LIM simulation, the method was found capable of efficient and accurate modeling of ESD transients.

Field-Induced CDM ESD test setup and the equivalent circuit model

There are several types of CDM test methods. The one on which we based our simulations is the field-induced method. In the actual test the chip is placed pins-up ("dead bug" position) on a thin dielectric layer on top of a field-charging electrode. The chip capacitance is charged indirectly to a desired stress voltage by a high voltage source. Next, one of the package pins is touched with a pogo pin, which creates a connection to the top ground plane and triggers the discharge event. The tester setup is shown in Fig.1.

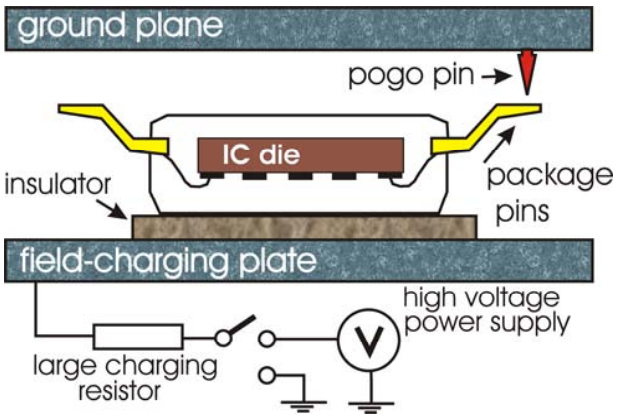

Figure 1: Field-induced CDM ESD test setup. Chip in the "dead bug" position.

The setup in Fig.1 can be represented with the equivalent circuit model (Fig.2) [5], [6].

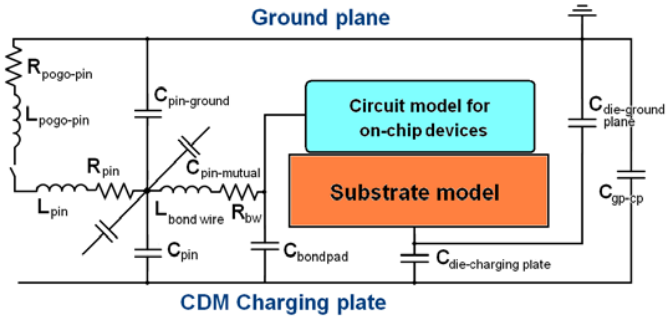

Figure 2: Circuit model of CDM test setup.

The model in Fig.2 represents an IC in a wirebonded, leaded package. The circuit model for on-chip devices includes power busses, ESD protection circuitry, and decoupling capacitors. The substrate can be modeled as three-dimensional resistive grid. The package pins as well as the pogo-pin are represented by series combinations of resistance and inductance. The charge stored on the elements of the chip and the package is contained in capacitances formed between these elements and the two plates of the tester. Using the model in Fig.2 the CDM ESD event can be successfully simulated using SPICE-like tools. The simulation, however, becomes very time-consuming if the high-resolution substrate model is used. Another limiting factor is the size of the on-chip power distribution network. Using high-resolution substrate model and large on-chip interconnect network may result in a circuit netlist with more than a million nodes. In such cases, conventional circuit simulators are ineffective and the use of alternative methods (such as LIM) is desirable.

Basic LIM Formulation

Latency Insertion Method (LIM) treats a network as a grid composed of nodes interconnected with branches. Each branch is represented as a combination of a voltage source, an inductor, and a resistor in series (as shown in Figure 3).

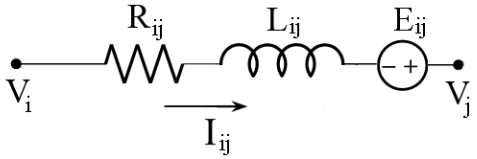

Figure 3: LIM branch representation

Current I_{ij} is assumed to be directed from node i at voltage V_i to node j at potential V_j.

Each node is modeled as a combination of a current source, a conductance, and a capacitor to the ground (as in Fig.4).

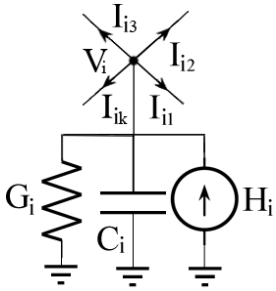

Figure 4: LIM node representation

Solution of the discrete time equation for the branch in Fig.3 yields the following expression for branch currents:

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n} + E_{ij}^{n+1/2}\right) \qquad (1)$$

The equation for node voltages (Fig. 2) reads:

$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{N_b} I_{ik}^n}{\dfrac{C_i}{\Delta t}} \qquad (2)$$

In the above equation, N_b is the number of branches connected to the node i (excluding connections to the ground).

Superscript n in (1) and (2) denotes discrete time. Currents are computed at whole time intervals, voltages at half intervals. In this way, computations of voltages and currents are alternated in time. This scheme is known as the "leapfrog" algorithm and is similar to the Yee algorithm used in the finite-difference time-domain method [7].

As seen from (1) and (2), the presence of latency generated by reactive elements L_{ij} and C_i is required for the algorithm to function. If reactive elements are not present in the circuit, small fictitious inductors must be inserted in each branch, and capacitors must be added at every node to enable LIM formulation. It can be shown that if the values of those fictitious elements are small enough, the accuracy of the simulation is not compromised [3].

The LIM algorithm uses central difference based finite-difference approximation, which is conditionally stable. The condition for the numerical stability of the method can be written as [8]

$$\Delta t < \sqrt{2} \min_{i=1}^{N_n} \left(\sqrt{\frac{C_i}{N_b^i} \min_{p=1}^{N_b^i} \left(L_{i,p} \right)} \right) \tag{3}$$

where N_n is the total number of nodes, N_b^i is the number of branches connected to node i, C_i is capacitance at the node, $L_{i,p}$ is the value of pth inductor connected to node i, Condition (3) is formulated for the semi-implicit update scheme, under the assumption that G_i=0. A more conservative (and more robust) upper bound for the time step is

$$\Delta t \le \min_{i,p} \left(\frac{\sqrt{L_{i,p} C_{ii}}}{\sqrt{N_b^i}} \right) \tag{4}$$

The condition for the time step in (4) was observed to be working when floating capacitors were present in the circuit.

ESD event simulation using LIM

To illustrate how LIM can be applied to the simulation of ESD events, we consider a simple circuit example shown in Fig.5. The circuit in Fig.5 represents a lumped model of all the key elements of the CDM test model in Fig.2. The circuit essentially represents a single pin between the two plates of the tester, with a single resistor R_{sub} modeling the substrate, and a diode representing on-chip circuitry. All nodes of the circuit are precharged to the desired stress voltage, then the switch is closed, the connection to the ground plane is established, and the discharge through the pogo-pin occurs.

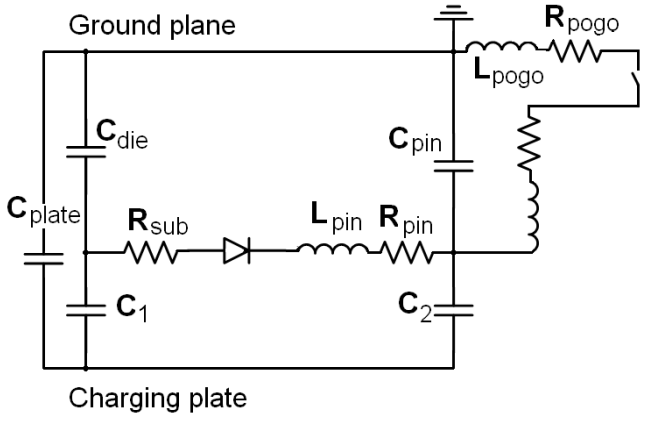

Figure 5: Simple circuit example

As mentioned earlier, the LIM algorithm requires that the circuit be represented as a network of nodes and branches containing latency elements. To enable the LIM simulation, the circuit in Fig.5 must be augmented. The three nodes of the circuit have capacitors connecting them to the ground plane. Since in the LIM simulation the ground plane is treated as the ideal circuit ground with constant zero voltage, these capacitors can be treated as standard node capacitors in the LIM scheme. However, capacitors C_1 and C_2 are floating, and thus do not fit into the standard LIM format. Branch capacitors require special treatment in the LIM and are processed using the direct integration method [8]. Some nodes of the circuit do not have capacitance; small fictitious capacitors to ground are added at such nodes to create latency. Small fictitious inductors must also be inserted into some of the branches. The resulting augmented circuit is shown in Fig.6.

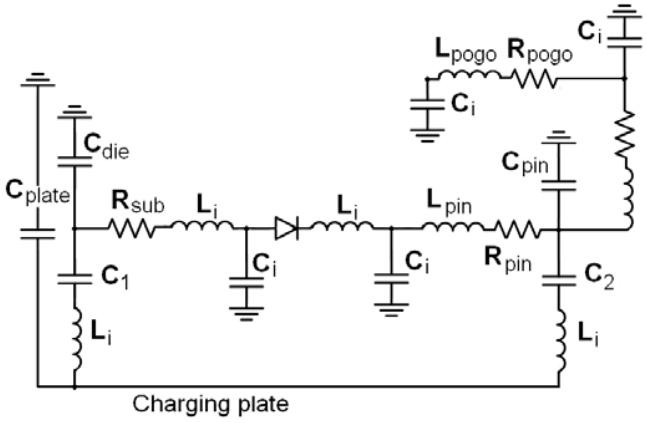

Figure 6: LIM-enabled simple circuit schematic

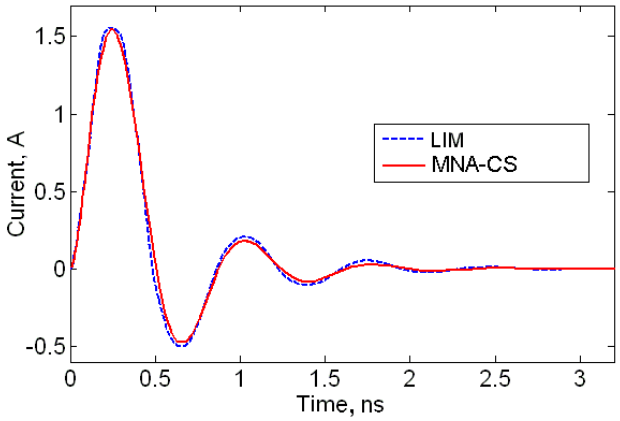

Figure 7: Small circuit ESD current waveform. Current is probed at the pogo-pin.

Finally, the test circuit contains a nonlinear element, a diode. Nonlinear devices can be incorporated into the LIM algorithm as shown in [3]. The nonlinear equation for current flowing through the diode is solved iteratively at each step of the simulation.

Initially, voltage at all nodes of the circuit is set to the precharge value; then, voltage at the node representing the ground plane is forced to zero, and the simulation begins.

Results of the LIM simulation are shown in Fig.7. The circuit was precharged to 300 V. Fig.7 shows a typical ESD transient current waveform with a very sharp spike occurring within the first 0.5 ns. The whole discharge event takes less

than 3 ns. To verify the LIM results, the same simulation was performed using an MNA-based commercial circuit simulator (MNA-CS). As evident from Fig.7, there is a good agreement with the LIM results.

Analysis of the full chip model using LIM

The full chip model used for the simulation includes the discrete distributed resistive model for the substrate in the form of a three-dimensional resistive grid [5], [6]. The grid is composed of cells; each cell contains 6 resistors (as shown in Fig. 8).

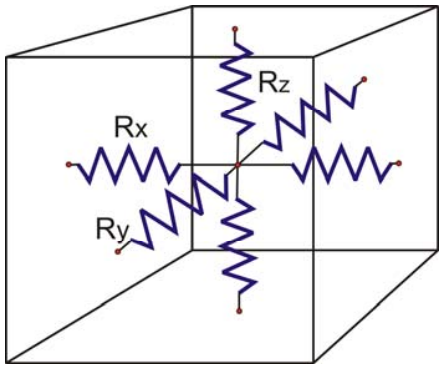

Figure 8: Unit cell of a lumped resistive substrate model.

The model for the on-chip circuitry includes power buses, modeled with resistive chains. Diode-based ESD protection circuitry is also included as well as decoupling capacitors. The resulting netlist contains over 82,000 nodes. The circuit is precharged to 300 V, the discharge connection is realized via the low resistance (20 Ohms) pogo-pin. The resulting current transient current flowing through the pogo-pin is shown in Fig.9. MNA-CS is again used to verify the LIM results. Close agreement between LIM and MNA-CS results is observed.

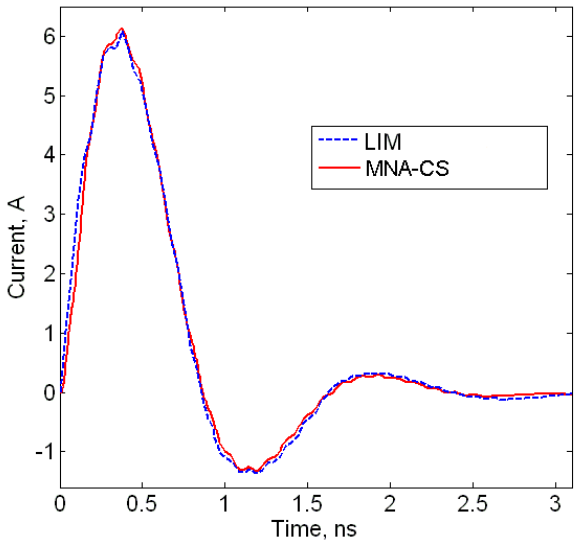

Figure 9: CDM ESD current waveform.

The discharge current waveform observed at the pogo-pin has the shape characteristic for the CDM ESD event. The first current spike exceeds 6 A, with a very fast rise time of roughly 0.5 ns.

In the LIM simulation we can probe voltage at any node and current through any branch in the circuit. For example, we can observe transient voltage waveform at one of the nodes inside the substrate (Fig.10).

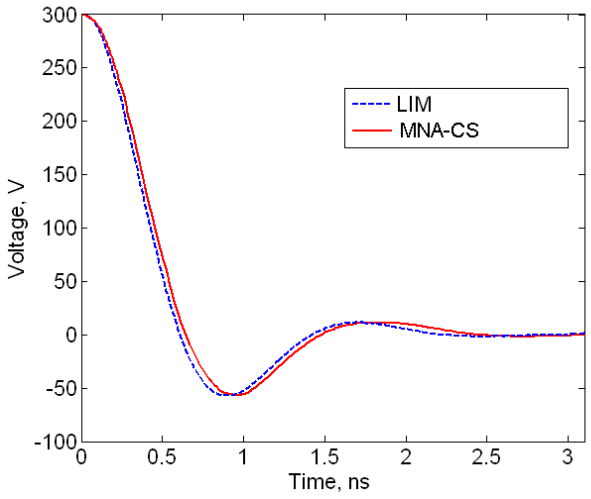

Figure 10: Transient voltage at one of the nodes inside the substrate.

Again, close agreement with the results of the simulation with the commercial tool can be observed.

Conclusions

The latency insertion method was applied to the analysis of the CDM ESD event. It was demonstrated that the LIM can accurately simulate the fast transients emerging during the discharge event. The full chip model that accounted for substrate conductivity and stresses occurring at the internal nodes of the chip was used in the simulation. Results of the LIM simulations are in close agreement with the ones obtained using a commercial MNA-based circuit simulator. While for small test cases conventional tools were observed to be faster than the LIM, as the circuit size increases the LIM becomes more efficient, and can significantly outperform other methods when the node count is in the millions.

References

1. Lee, J., K.-W. Kim, Y. Huh, P. Bendix, S.-MKang, "Chip-Level Charged-Device Modeling and Simulation in CMOS Integrated Circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 22, No. 1, 2003, pp. 67-81.
2. *ADI Reliability Handbook*. Analog devices, Inc., Norwood, MA, 2000.
3. Schutt-Ainé, J. E., "Latency insertion method (LIM) for the fast transient simulation of large networks," *IEEE Trans. Circuit Syst*., vol. 48, Jan. 2001, pp. 81-89.
4. A. Taflove, *Computation Electrodynamics: The Finite-Difference Time-Domain Method*. Boston, MA: Artech House, 1995.

5. M.S.B Sworariraj, Smedes T, Salm C., Mouthaan, A.J. and Kuper, F.G, “Role of package parasitics and substrate resistance on the CDM failure levels”, *Microelectronics Reliability*, vol. 43, pp. 1569-1575, 2003.
6. Shukla, V. Jack, N and Rosenbaum, E., "Predictive Simulation of CDM Events to Study Effects of Package, Substrate Resistivity and Placement of ESD Protection Circuits on Reliability of Integrated Circuits", In press, *IEEE International Reliability Physics Symposium 2010*.
7. Yee, K. S., “Numerical solution of initial boundary value problems involving Maxwell’s equation in isotropic media,” *IEEE Antennas Propagat*., vol. AP-14, May 1996, pp. 303-307.
8. Lalgudi, S. L., Swaminathan, M., and Kretchmer, Y., “On-chip power-grid simulation using latency insertion method,” *IEEE Trans. Circuit Syst*., vol. 55, no. 3, Apr. 2008, pp. 914–931.