Application of the Latency Insertion Method to Electro-Thermal Circuit Analysis

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Abstract— **In this paper, a fast circuit simulation technique based on the Latency Insertion Method (LIM) is proposed for the electro-thermal analysis of circuits and high-performance systems. The method is applied to the modeling of on-chip and off-chip 3D-interconnect networks. The proposed method is shown to be capable of modeling both electrical and thermal phenomena occurring in high speed, high performance VLSI circuits at the pre-layout design stages.**

Keywords-circuit simulation; electro-thermal analysis; latency insertion; IR drop; power integrity

I. INTRODUCTION

Advances in the silicon industry led to a variety of signal and power integrity issues. As the designs get more complicated and design margins shrink, those issues have to be addressed at the earliest (at architecture or floor planning) stages of the design flow. The pre-layout stage becomes extremely important as the errors introduced at that stage are fundamental, likely to affect the performance and placement of all system components, and can potentially be fatal for the product, thus leading to a necessity for complete redesign and to unacceptable time-to-market delays.

At the pre-layout stage, the detailed information about system components and their characteristics are not available. Therefore, the models used in the analysis can be relatively simple. However, with the ever-increasing complexity of integrated circuits, these simplified models constantly grow in size. The sheer size of such models creates computational challenges that are not handled well by most of the industry-standard, matrix-based CAD tools. Also, at that stage of the design process there is a need for quick estimates, and simulations have to be run multiple times with minor adjustments to the model. Hence, there is a need for tools that are capable of performing fast and efficient analysis of relatively simple but potentially very large networks. It is desirable to simultaneously address multiple interdependent issues in various components of the system, ensuring electrical, thermal, and mechanical reliability of the future product.

In this paper we propose the latency insertion method (LIM) as the tool that has the power and versatility necessary for performing a complex electrical and thermal analysis of the systems at early design stages. Our focus is on the modeling of on-chip interconnect networks and phenomena that affect their performance in tightly packed, very dense modern ICs. In particular, we consider on-chip power delivery system, with such effects as the steady-state IR drop and its dependence on temperature.

The latency insertion method was initially proposed as a transient simulation technique to efficiently model large networks [1]. LIM applies the finite-difference technique to circuit equations for voltages and currents. The method iteratively solves circuit equations using a time-stepping scheme; therefore, it avoids construction and computation of a large matrix (as opposed to SPICE). The method demonstrates linear numerical complexity, enables analysis of very large networks and can greatly outperform conventional matrix-based methods.

It has been previously demonstrated that LIM can be successfully applied to the problem of the DC IR drop analysis [2] as well as the transient simulation of on-chip power distribution networks [3]. In this work we consider application of the method to the problems specific to the early, pre-layout design stages, and demonstrate the capability of LIM to perform steady-state and potentially transient thermal analysis of the IC structure. We suggest that the method can be used for electro-thermal co-simulation that will address the interdependence of electrical and thermal parameters.

The rest of the paper is organized as follows. In Section II, the formulation of the LIM method is described. Section III demonstrates application of the LIM method to the IR drop analysis of the power delivery network structure. In section IV, application of LIM to the thermal and electro-thermal analysis is considered. Finally, in Section V, the conclusions are presented.

II. LIM FORMULATION

LIM treats a circuit as a grid composed of nodes interconnected with branches. Each branch is represented by a series resistor-inductor model as shown in Fig. 1. Each node is modeled as a combination of a current source, and a shunt capacitor to the ground as shown in Fig. 2.

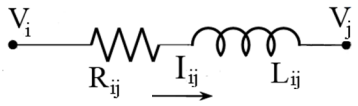

Figure 1. LIM branch equivalent circuit

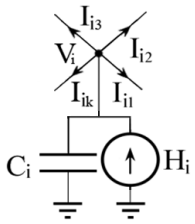

Figure 2. LIM node equivalent circuit.

Using Kirchoff's voltage law (KVL) for the circuit in Fig. 1, the solution of the discrete time equation yields the following expression for branch currents:

$$I_{ij}^{n+1} = 2\Delta t \frac{\left(V_i^{n+1/2} - V_j^{n+1/2}\right)}{\left(2L_{ij} + R\Delta t\right)} + I_{ij}^{n} \frac{\left(2L_{ij} - R\Delta t\right)}{\left(2L_{ij} + R\Delta t\right)} \quad (1)$$

Superscripts in (1) represent discrete time. Currents are computed at whole time intervals $t = n\Delta t$, while voltages are computed at half intervals $t = (n+1/2)\Delta t$, where Δt is the time step.

Solution of Kirchoff's current law (KCL) for the LIM node equivalent circuit yields the expression for node voltages:

$$V_i^{n+1/2} = V_i^{n-1/2} - \frac{\Delta t}{C_i}\left(\sum_{k=1}^{N_a} I_{ik}^{n} - H_i^{n}\right), \quad (2)$$

where N_a is the total number of branches connected to node i.

As can be seen from (1) and (2), the presence of latency generated by reactive elements L_{ij} and C_i is required for the algorithm to function. If reactive elements are not present in the circuit, small fictitious ones have to be added to enable the LIM formulation. It can be shown that if values of those fictitious elements are small enough, the accuracy of the transient simulation is not compromised [1]. In the case of steady-state analysis, the values of the fictitious elements do not affect the results of the simulation [2].

III. Steady-State IR Drop Analysis Using LIM

At the pre-layout stage, information about the circuit is available in the form of a floor plan, a pad out, and current and voltage budgets. The model for power integrity analysis is then built based on the process parameters, supply voltage values, required current loads, general geometry and the floor plan

We consider a simple example based on the structure in Fig. 3. The subject of the analysis is the VDD net in the top two metal layers. The floor plan is divided into six rows and six columns. The connections to the voltage supply (C4 bumps) are on the top level in the two middle rows (as shown in Fig. 3(a)). The power is drawn from the second metal layer at the top and bottom rows. Each metal segment (a square in Fig. 3(a)) is represented with a resistive grid of the form shown in Fig. 3(b). Metals in two layers are orthogonal to each other and interconnected by vias. If the segment has a connection to the power supply, a constant voltage source is inserted in the center (a bump). If the segment has connections to the active devices, the power drawn by those devices is modeled with constant current sources (current loads).

The resulting resistive network has the structure common for steady-state IR drop problems and can be efficiently analyzed with LIM. The results of the LIM simulation are verified by simulating the same structure in HSPICE. The results are shown in Fig. 4.

The supply voltage level in this example is 1 V. Fig. 4 displays voltage at four load points of each segment. It is clear that voltage is higher in the midsection at the locations of the supply connections. Voltage levels drop toward the top and the bottom parts of the plots which correspond to the rows where current is drawn from the supply.

In general, in this example the voltage across the whole structure stays very close to the nominal supply value and the range of values is only 6 millivolts. The benchmark HSPICE simulation (Fig. 4(a)) assumes the temperature of 85°C. The first simulation of the structure with LIM is performed using nominal values of resistances (at 25°C). It can be seen from Fig. 4(b) that voltage values predicted by the simulation are overestimated. In the next LIM simulation the temperature is taken into account and set to 85 °C.

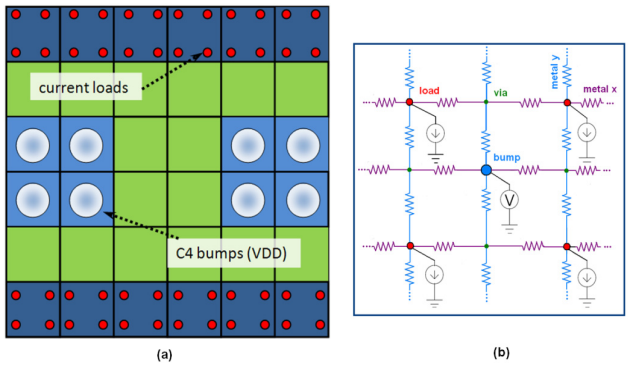

Figure 3. Model structure for IR drop analysis

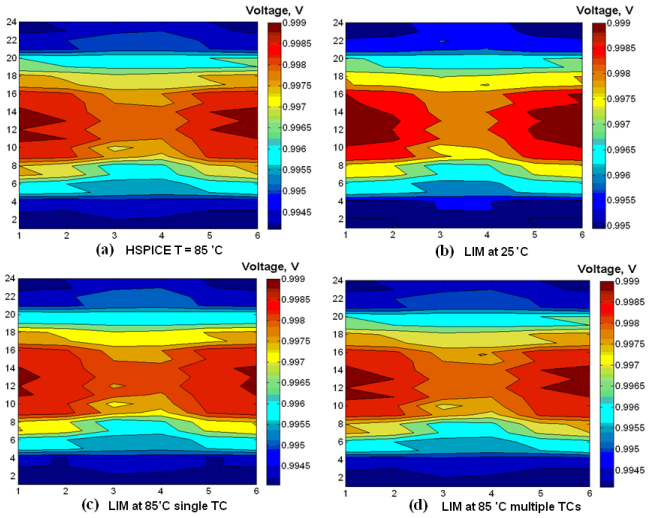

Figure 4. IR drop analysis results

For simplicity, a single value of the temperature coefficient was used for resistances in all metal layers. The voltage distribution in Fig. 4(c) very closely matched to that of the benchmark. Finally, with difference in thermal coefficients of resistances of the three metals taken into account, Fig. 4(d) is almost identical to the results from the HSPICE benchmark. It can be seen from Fig. 4 that LIM has enough precision to correctly resolve voltage values in the narrow range of 6 mV.

IV. Electro-Thermal Analysis Using LIM

The differences in Fig. 4(a), (b) and (c) demonstrate the well-known fact that resistance has a strong dependence on temperature. To obtain the correct estimate of the IR drop profile in the power grid the operating temperature of the chip must be factored in.

There are two main sources of interconnect heating: the self heating (or Joule heating) due to current passing through resistive wires, and the raised temperature of the substrate due to power dissipated by the active devices.

The problem of self heating can be modeled by creating an equivalent thermal-electrical network based on thermal electrical analogy. In such a network thermal resistances account for the thermal conductivity of the material; heat flux is then represented by the electrical current, and voltage is equivalent to temperature [4]. The equivalent steady state thermal problem essentially becomes a problem of steady-state IR drop analysis in the equivalent network. The resulting network can be solved using an electrical simulator (such as SPICE). However, the electrical and thermal simulations are interdependent and therefore have to be iterated until convergence is achieved. The size of such electro-thermal problem makes traditional matrix-based direct solvers inefficient since the complexity of these methods does not scale well with the size of the model. A number of alternative techniques have been proposed to address this issue [5],[6]. We suggest that the LIM can be successfully applied to the electro-thermal analysis of large on-chip and off-chip interconnect systems. The added advantage of the LIM is its ability to efficiently model transient behavior, while the majority of other techniques targeting the steady-state IR-drop analysis cannot perform transient simulations.

Another source of interconnect heating (and the dominant one) is the heat generated by the active devices which raises the overall temperature of the substrate. While the problem of self heating of interconnects is addressed in [5], the substrate temperature is assumed to be known. In reality, particularly at the early design stages, the temperature profile of the substrate is not readily available and needs to be calculated. Therefore, the problem of thermal analysis of the substrate containing the interconnect network is added to the problem of electro-thermal analysis of the interconnect system itself. The size of the resulting problem almost inevitably exceeds the capabilities of traditional methods. In this work we show that LIM can be employed to obtain the thermal solution for the system and hence, potentially, LIM can be used for the complete analysis of on-chip power integrity problem.

To demonstrate the application of the LIM to thermal analysis we consider an example of 2D heat transfer problem with convection shown in Fig. 5, for which the analytical solution exists [7]. The structure in Fig. 5 represents a solid block of a material with the thermal conductivity of 52 W/m°C. The source of heat is the edge AB with constant temperature of 100°C. The heat can only escape through edges BC and CD via convection to the ambient temperature of 0°C. The surface convective heat transfer coefficient on edges BC and CD is h = 750 W/m^2°C. The target solution for temperature at point E is 18.3°C.

We employ the analogy between thermal and electrical circuits. The bulk of the material is modeled with two-dimensional resistive grid. Values of the grid resistors are calculated based on the thermal conductivity of the material and the unit cell size. The fixed raised temperature on the edge AB is introduced via constant voltage sources along the boundary. Boundary conditions on the convective edges are modeled with resistances connected from the grid nodes on the edges to constant voltage sources (the ambient temperature) [4], [8]. Values of the interface resistors are derived from the heat transfer coefficient as

$$R_h = 1/(h A_e)\,, \tag{3}$$

where A_e is the effective area of a unit cell of the grid.

Adiabatic boundary conditions are assumed on the AD side of the structure. The general cell structure of the equivalent network is shown in Fig. 6.

Results of the LIM simulation for the example problem match the target analytic solution almost exactly (Fig. 7).

Next, we consider the 3D model of the structure in Fig. 8, which consists of two silicon chips with a composite interposer substrate. We again use a resistive grid to model the structure, but now we add the third dimension. The power dissipated by the active devices is represented by constant current sources.

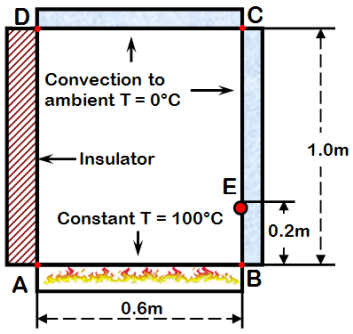

Figure 5. Test example structure

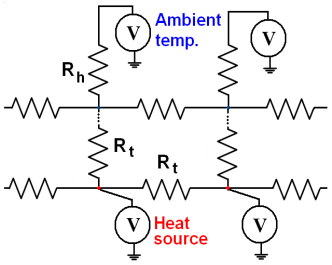

Figure 6. Thermal-electrical model structure

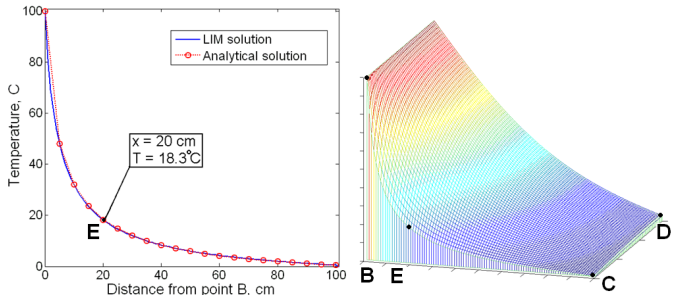

Figure 7. Simulation results for the test example

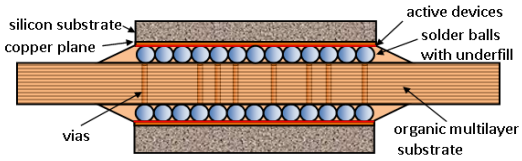

Figure 8. System of two chips with an interposer substrate

The resulting thermal-electrical model is simulated with LIM. For verification, the same structure is modeled in the commercial CAD tool ANSYS® Icepak® [9]. The results are shown in Fig. 9.

In Fig. 9, the chip on top dissipates almost four times more power than the one at the bottom and reaches temperatures close to 100 °C. The ambient temperature is set to 25 °C. The organic interposer substrate has low thermal conductivity intrinsically. However, the substrate is interlaid with copper planes which increase heat spreading in lateral directions. Top and bottom chips have vertical interconnect structures between them, which increase heat transfer across the substrate.

In the case of Icepak® simulation, forced air cooling is assumed at 2 m/s, with airflow from left to right. For that reason, the resulting temperature distribution is not symmetric. The heat transfer is more efficient at the leading (left) edge of the structure, where the air is the coolest and the boundary layer has not been formed yet. The cooling is much less efficient on the right side of the structure. In the LIM simulation we use the effective heat transfer coefficient h_e to calculate the value of the resistance R_h that models the convective boundary (conjugate heat transfer) as in (3) [4].

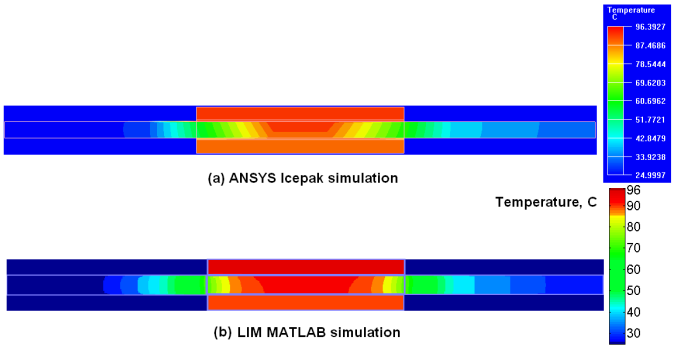

Figure 9. Temperature distribution within the structure (cross-section)

For purposes of this example, we want to keep our model as simple as possible. For that reason, uniform mean values of R_h are used in the LIM model for the left and right parts of the structure (higher R_h on the right). In general, a good agreement of the LIM and Icepak® results can be observed in Fig. 9. We are not concerned with the detailed modeling of the heat transfer between the chip and the ambient air. Our goal is to get a quick and reasonably accurate estimate of the temperature profile of the chip and use that information in the subsequent power integrity analysis. For those purposes the LIM performance is more than adequate. Fig. 9(b) demonstrates the correct temperature range and distribution when compared to the results obtained with the commercial CAE tool.

V. Conclusion

In this work, we have proposed the latency insertion method (LIM) for the complex analysis of integrated circuits and systems at the pre-layout stages. We have demonstrated that LIM can be successfully used to address both electrical and thermal aspects of the circuit design and potentially combine the two and perform complete electro-thermal analysis of on-chip and off-chip interconnect networks. The size of the full electro-thermal model of the integrated circuit at the latest technology nodes can be prohibitively large for traditional circuit simulators. Such model becomes very large even at the earliest stages of the design when there is a need for quick assessments and repeated simulations with minor adjustments to the model. LIM demonstrates linear numerical complexity and hence scales well with the size of the model, unlike the traditional matrix-based methods. The LIM provides the capability of performing both steady-state and transient analysis within the scope of a single method.

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