Cut-off Frequency Enhanced Hybrid Electromagnetic Bandgap (EBG) Structures with Wideband Noise Suppression Characteristics

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***Abstract:** A cut-off frequency characteristic enhanced hybrid EBG structure is proposed. In the proposed EBG structure, inductive bridges between neighboring metal patches are designed using lumped chip inductors instead of conventional microstrip lines. From 75 MHz to 4830 MHz a stopband bandwidth of 4.755 GHz is achieved at a -30 dB noise suppression level.*

Introduction

Due to continuous increase of CMOS device cut-off frequencies (f_Ts) single chip integrations of high speed mixed-signal systems are widely researched. One of the design and testing issues of such high speed mixed-signal designs is the simultaneous switching noise (SSN) coupling through solid power/ground plane pairs. The increased operating speed of digital blocks results in large SSN, which degrades not only the noise margins of digital circuits, but also the performance of analog circuits. At PCB/package level, the generated SSN can propagate through parallel plate waveguides which are formed by the solid power/ground plane pairs.

In order to suppress the noise coupling at the PCB/package level, Wu *et al.* used a uniplanar EBG structure in the design of the power/ground plane pairs [1]. The uniplanar EBG structure consists of a 2-dimensional array of metal patches and microstrip line bridges between the neighboring patches. Wu's EBG structure showed a wideband noise suppression characteristic with a 3 GHz stopband bandwidth, however, due to low inductance of the bridges the stopband cut-off frequency of the EBG structure was around 1 GHz. In order to reduce the cut-off frequency, several high inductance microstrip line bridges are proposed [2], [3]. However, the lowest cut-off frequency of the previously reported EBG structures is around 300 MHz, which is still higher than the clock frequencies of current mixed-signal systems.

In this work, an EBG structure with VHF-band cut-off frequency is proposed by replacing the microstrip line bridges with lumped chip inductors. A one-dimensional analysis model is developed to provide the mathematical foundation for the use of lumped chip inductors in the EBG structure design.

One-Dimensional Analysis of Planar EBG Structure

Fig. 1 shows a one-dimensional equivalent circuit of the planar EBG structure, where *a* and *g* are the center-to-center distance and the gap size between

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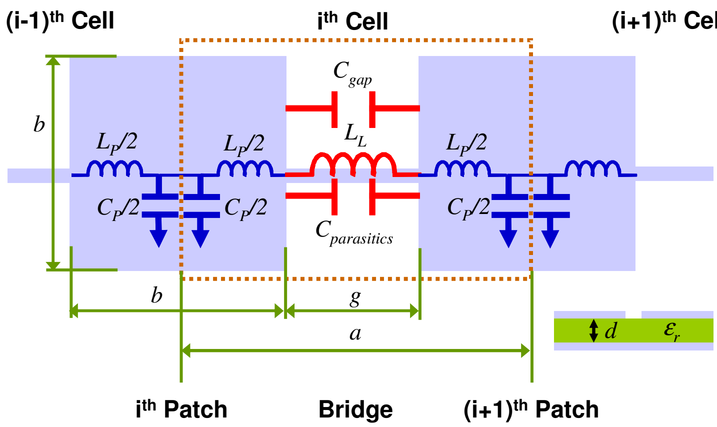

Fig. 1. One-dimensional Equivalent Circuits of the EBG structure

two neighboring patches, respectively, b is the width of the rectangular patches, and d is the height of the dielectric substrate. L_P and C_P are the inductance and the capacitance of each square metal patch, respectively, L_L is the inductance of the bridge, and C_T is the series parasitic capacitance between two patches including the gap capacitance (C_{gap}) and the parasitic capacitance of the bridge ($C_{parasitics}$).

L_P, C_P, and C_{gap} can be calculated using published quasi-static models [4]. $C_{parasitics}$ varies depending on the physical implementation of the bridges, and typical values of $C_{parasitics}$ for lumped chip inductors are less than 0.24 pF [5]. C_{gap} is larger than $C_{parasitics}$ under the condition that $b{\cdot}(1+\varepsilon_r)$ is larger than $C_{parasitics}{\cdot}$(118.6e+12) mm for the EBG structures with g=0.1·a. For the 0.24 pF series parasitic capacitance, the calculated value of $C_{parasitics}{\cdot}$(118.6e+12) is 28.5 mm, which is only 22.6 % of the calculated values of $b{\cdot}(1+\varepsilon_r)$ using parameters of the previous EBG structures [1–3]. The capacitances ratio C_{gap}/C_P is very small for typical PCB/package structures, since the values of b are much larger than those of d. The typical value of d is in the range of 0.4 – 1.6 mm, and the width of the patches is around 30 mm [1–3].

By applying the image parameter method [4] and the above two capacitance ratios, the lower (f_{lower}) and upper (f_{upper}) cut-off frequencies of Fig. 1 can be derived as

$$f_{lower} = \left[\pi\sqrt{C_P(L_P + L_L)}\right]^{-1} \quad (1)$$

$$f_{upper} = \left[2\pi\sqrt{C_T C_P L_P/(4C_T + C_P)}\right]^{-1}. \quad (2)$$

f_{lower} and f_{upper} are not related to C_T and L_L, respectively. That is, although lumped chip inductors have low self resonant frequencies (SRFs) due to their series parasitic capacitances, the cut-off frequency of the EBG structure can be lowered by using the high inductance chip inductors as the bridges. And the replacements cause no degradation of the other high frequency characteristics.

Design and Experimental Verification of Proposed Hybrid EBG Structure

Fig. 2 (a) shows the fabricated hybrid EBG structure. In order to directly compare the noise suppression performances, physical dimensions and port locations of the proposed EBG structure are the same with those of reference [2], and captioned in the figure. The thickness and the dielectric constant of the substrate are 0.4 mm and 4.4, respectively, and Coilcraft, Inc., 0603LS-561X 560 nH chip inductors are used as the bridges instead of the microstrip lines.

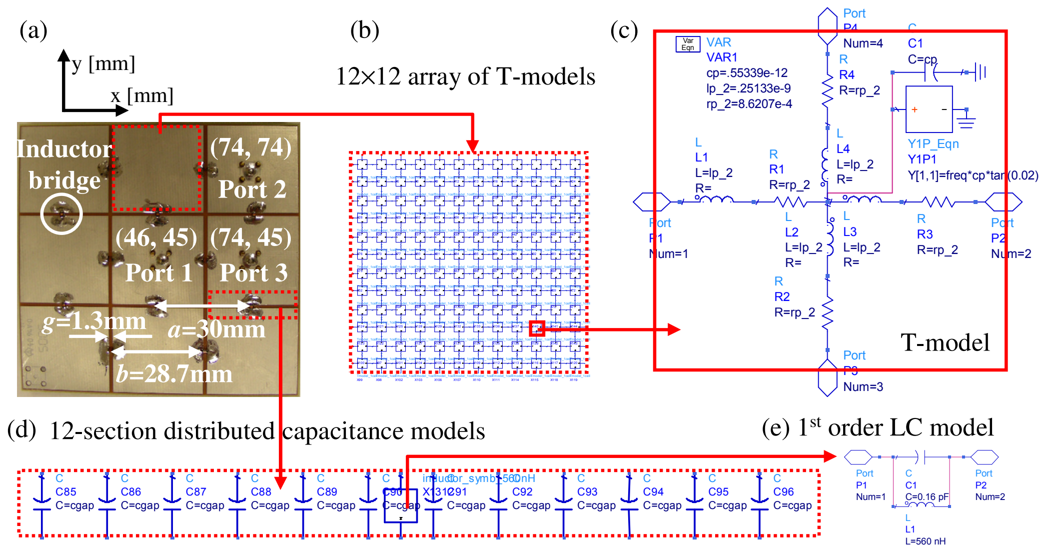

Fig. 2. Schematic of Proposed EBG PDN and corresponding ADS simulation models

Fig. 2 (b) to (e) show the ADS simulation models for the patches, the gaps, and the lumped chip inductors, respectively. The 2-dimensional array of distributed RLCG element method [6] is used to model the patches. 12-section distributed C models and 1st-order parallel LC models are used to model the gap capacitances and the lumped chip inductors, respectively. Parasitic series capacitances of the chip inductors are calculated from the self resonant frequencies (SFRs) of the lumped chip inductors in datasheets [5].

Fig. 3 shows simulated and measured insertion loss responses of the proposed and the reference EBG structures [2]. An Agilent E8358A PNA Series Network Analyzer is used to measure the S-parameters, and for brevity of figure only |S21| responses are plotted. The open circles represent the measured |S21| response of a structure without the EBG structure, while open and solid rectangles represent simulated and measured |S21| responses of the proposed EBG structure, respectively. The reference EBG structure [2] is simulated using Ansoft HFSS, and the solid circles represent simulated |S21| responses. The calculated, simulated and measured cut-off frequencies of the proposed structure are 47.5, 49.2 and 47.2 MHz, respectively. The measured stopband bandwidth of the proposed EBG structure at the -30 dB noise suppression level is 4755 MHz (75 – 4830 MHz), while the simulated stopband bandwidth of the reference EBG structure is only 4325 MHz (555 – 4875 MHz).

Conclusions

In this work, a hybrid EBG structure with a cut-off frequency of 47.2 MHz and a noise suppression bandwidth of 4.755 GHz is proposed by using lumped chip inductors instead of microstrip lines. The stopband bandwidth is enhanced by more than 430 MHz and the enhancement can be further increased by using higher values of chip inductors. The 1-dimensional analysis model and the ADS circuit level simulation models are also developed for the proposed EBG structure. The simulated and measured |S21| responses of the proposed EBG structure are in substantial agreement with each other.

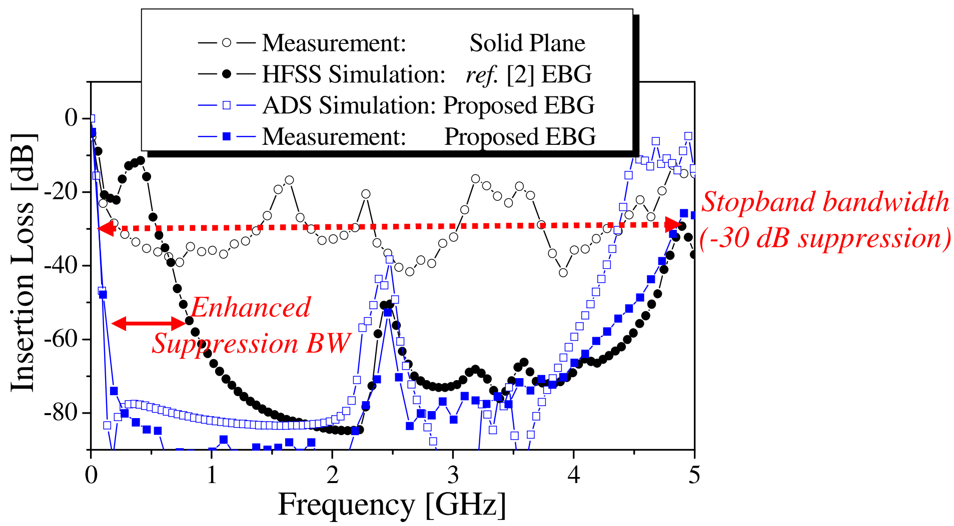

Fig. 3. |S21| Insertion Loss Characteristics of the Proposed EBG Structure

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