Latency Insertion Method (LIM) for CMOS Circuit Simulations with Multi-rate Considerations

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***Abstract*—In this paper, we present an application of the latency insertion method (LIM) to the transient simulations of CMOS circuits and compare it to traditional SPICE based methods. In addition, we extend the multi-rate simulation technique and apply it to the simulation of CMOS circuits in the LIM environment and illustrate its computational efficiently over the basic LIM.**

Keywords-circuit simulation; latency insertion method (LIM); CMOS; multi-rate simulation;

I. INTRODUCTION

With the increase in density of interconnects and the complexity of high-speed packages, signal integrity becomes an important aspect in the design of modern devices. Circuit designers are constantly in need of newer and better methods that are able to capture the complicated electromagnetic behaviors of complex circuits. In this aspect, the ability to accurately simulate large circuits in a reasonable amount of time is invaluable in the design of any circuit. As a result, there is a constant need and push towards faster circuit simulation methods that are able to handle large circuits in a fraction of the time of conventional circuit simulators.

The latency insertion method (LIM) [1] has recently emerged as an efficient approach for performing fast simulations of very large circuits. By exploiting latencies in the circuit, LIM is able to solve the voltages and the currents in the circuit explicitly at each time step. This results in a computationally efficient algorithm that is able to simulate large circuits significantly faster than conventional matrix-inversion based methods.

The LIM method has recently been extended to handle CMOS devices [2],[3]. However, in [2], only the simulations of simple inverters were shown while [3] only shows the simulation of a CMOS NAND. In this paper, we study the simulations of larger CMOS circuits and compare the performance of LIM versus conventional circuit simulators such as SPICE. In addition, we extend the multi-rate LIM simulation technique [4–6] to CMOS devices and show how it can be applied to basic CMOS circuit structures. Comparisons with the traditional LIM will be depicted.

The remainder of the paper is organized as follows. Section II reviews the LIM formulation. Section III presents the application of LIM to CMOS circuits while section IV explains the multi-rate simulation technique. Numerical examples will be depicted in section V and a conclusion is given in section VI.

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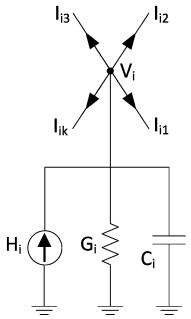

Fig. 1. Node topology.

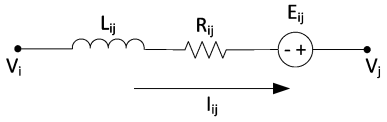

Fig. 2. Branch topology.

II. BASIC LIM FORMULATION

LIM can be applied to any arbitrary network, where it is assumed that through the use of Thévenin and Norton transformations, the branches and nodes of the circuit can be described by the general topologies shown in Fig. 1 and Fig. 2. Each node is represented by a parallel combination of a current source, a conductance, and a capacitor to ground. The connection between two different nodes forms a branch and it is represented by a series combination of a voltage source, a resistor and an inductor. In order to solve for the voltages and currents in the circuit, LIM discretizes the time variable whereby the voltages and currents are collated in half time steps. Specifically, the voltages are solved at half time steps while the currents are solved at full time steps. From Fig. 1, writing Kirchhoff's current law (KCL) at node *i* yields

$$C_i\left(\frac{V_i^{n+1/2}-V_i^{n-1/2}}{\Delta t}\right)+G_iV_i^{n+1/2}-H_i^n=-\sum_{k=1}^{M_i}I_{ik}^n \qquad (1)$$

where the superscript n is the index of the current time step, Δt is the time step and M_i is the number of branches connected to node i. Solving for the unknown voltage yields

$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n}{\dfrac{C_i}{\Delta t} + G_i} \tag{2}$$

for i = 1, 2, …, N_n where N_n is the number of nodes in the circuit.

From Fig. 2, writing Kirchhoff's voltage law (KVL) at branch ij yields

$$V_i^{n+1/2} - V_j^{n+1/2} = L_{ij}\left(\frac{I_{ij}^{n+1} - I_{ij}^n}{\Delta t}\right) + R_{ij} I_{ij}^n - E_{ij}^{n+1/2}. \tag{3}$$

Solving for the unknown current yields

$$I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^n + E_{ij}^{n+1/2}\right). \tag{4}$$

The computation of the node voltages and the branch currents are alternated as time progresses in a leapfrog manner. In this aspect, LIM is similar to the Yee's algorithm for the solution of Maxwell's equations in the finite difference time domain (FDTD) method [7]. It is clear that the LIM algorithm relies on the latencies in the network to perform the leapfrog time stepping formulation. Thus, at every node, a capacitor to ground has to be present. If it is not, a small fictitious capacitor is inserted. Similarly, small fictitious inductors are inserted into branches without latencies.

As with the FDTD method, LIM is only conditionally stable. In other words, there is an upper bound on the time step that will result in a numerically stable solution to (2) and (4). Numerous work on the study of the stability of LIM have been done in [8–10].

III. Application to CMOS Circuits

LIM can be easily applied to CMOS circuits. When a CMOS device is present, the drain current of the CMOS is used as the branch current in place of (4). The CMOS drain current can be calculated using the appropriate model for the device. In this work, we adopt the Shichman-Hodges model as used in [2],[3] to model the CMOS devices where the drain current for an NMOS, I_{Dn} is given by

$$I_{Dn} = 0, \quad V_G - V_S < V_{Tn}; \quad V_D - V_S \geq 0 \quad (cutoff) \tag{5a}$$

$$I_{Dn} = \frac{K_n W_n}{L_n}\left(V_G - V_S - V_{Tn} - 0.5(V_D - V_S)\right)\left(V_D - V_S\right), \tag{5b}$$
$$V_G - V_S > V_{Tn}; \quad 0 < V_D - V_S < V_G - V_S - V_{Tn} \quad (ohmic)$$

$$I_{Dn} = \frac{K_n W_n}{2L_n}\left(V_G - V_S - V_{Tn}\right)^2, \tag{5c}$$
$$V_G - V_S > V_{Tn}; \quad V_D - V_S > V_G - V_S - V_{Tn} \quad (saturation)$$

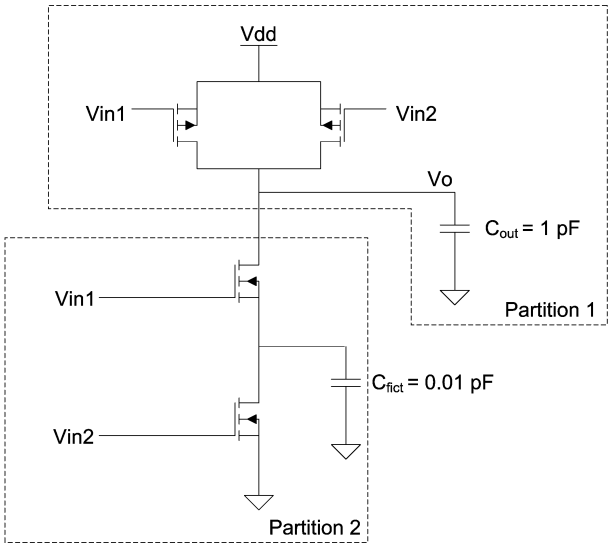

Fig. 3. CMOS NAND.

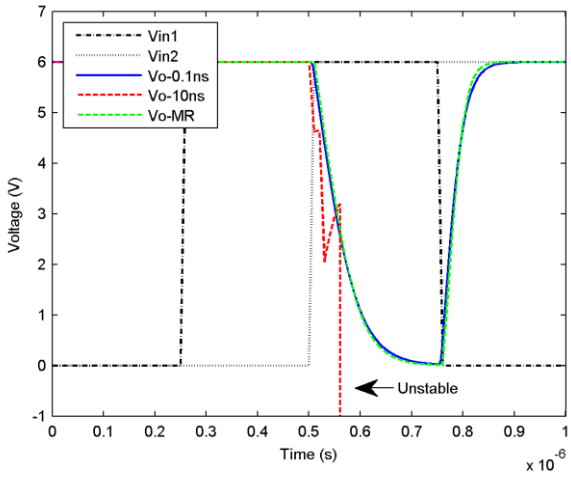

Fig. 4. Simulation of CMOS NAND.

where K_n, W_n, L_n, and V_{Tn} are the transconductance, channel width, channel length, and threshold voltage for the NMOS device respectively, V_G is the gate voltage, V_S is the source voltage and V_D is the drain voltage. Similarly, the drain current of a PMOS, I_{Dp} is given by

$$I_{Dp} = 0, \quad V_G - V_S > V_{Tp}; \quad V_D - V_S \leq 0 \quad (cutoff) \tag{6a}$$

$$I_{Dp} = \frac{-K_p W_p}{L_p}\left(V_G - V_S - V_{Tp} - 0.5(V_D - V_S)\right)\left(V_D - V_S\right), \tag{6b}$$
$$V_G - V_S < V_{Tp}; \quad 0 > V_D - V_S > V_G - V_S - V_{Tp} \quad (ohmic)$$

$$I_{Dp} = \frac{-K_p W_p}{2L_p}\left(V_G - V_S - V_{Tp}\right)^2, \tag{6c}$$
$$V_G - V_S < V_{Tp}; \quad V_D - V_S < V_G - V_S - V_{Tp} \quad (saturation)$$

where K_p, W_p, L_p, and V_{Tp} are the transconductance, channel width, channel length, and threshold voltage for the PMOS

device respectively. Note that in SPICE, this model is selected by using the option "*LEVEL=1*" in the *.MODEL* statement.

It has been shown that (5) and (6) can be most easily solved, without much loss of accuracy, if we adopt an explicit formulation, where the voltages at the previous time step are used in solving for the drain currents [3].

IV. Multi-rate Simulation for CMOS Circuits

It is well known that the choice of a stable time step for a LIM simulation depends on the capacitances at each node [8–10]. Specifically, circuits that contain smaller capacitances require smaller time steps for a stable simulation. The multi-rate technique has been applied to speed up LIM simulations without violating the stability criteria, whereby the circuit is first partitioned into smaller subcircuits and different time steps are used for different partitions depending on the maximum stable time step [4–6]. In this work, we apply the multi-rate simulation technique on a node-by-node basis. Instead of partitioning the entire circuit into smaller partitions, we evaluate each node with its own maximum stable time step depending on the value of the capacitance at that node. Since we are dealing with CMOS circuits, the problem is simplified as we are not dealing with branch inductances. We will illustrate this idea by means of an example.

Consider the CMOS NAND circuit shown in Fig. 3 where we have assumed an output capacitance of 1 pF and a small fictitious capacitance of 0.01 pF at the inner node. Deriving an analytical stability condition for this circuit would require a rigorous mathematical analysis which is beyond the scope of this paper. However, by trial and error, we have determined the maximum stable time step to be 0.1 ns. Note that this time step is due to the small fictitious capacitor and if we split the circuit into two partitions as shown in Fig. 3, the upper node can be simulated using a time step of 10 ns without violating the stability criteria. Thus the idea is to simulate the circuit using the two time steps, one of each node. By doing so, we are able to speed up the simulation as the upper partition is only evaluated once for every 100 times of the lower partition. Fig. 4 shows the simulation of the circuit in Fig. 3 using the traditional LIM with time steps of 0.1 ns, 10 ns, and a multi-rate simulation with time steps of 0.1 ns and 10 ns. We see that the multi-rate simulation retains the accuracy of the 0.1 ns simulation while the simulation with time step of 10 ns results in an erroneous solution as expected.

V. Numerical Examples

In this section, two numerical examples will be presented. First a CMOS RAM circuit will be simulated in LIM and SPECTRE [11], a commercial circuit solver from Cadence Design Systems in order to illustrate the speed improvement of LIM compared to SPICE based methods. Then a chain of ripple-carry adders will be used to illustrate the application of the multi-rate simulation technique with CMOS devices.

A. RAM Circuit

In this example, a RAM circuit is simulated in LIM and in SPECTRE. The circuit contains 4850 nodes and 13,880 MOSFETs. A 1 pF capacitor is assumed to be present at each node to enable LIM. A time step of 0.5 ns is used in LIM in order to obtain a stable and accurate result while SPECTRE is allowed to determine its own suitable time step. The simulation length in both cases is 600 ns. Fig. 5 and 6 show the results at select nodes in both the LIM and SPECTRE simulation, respectively. We see that both methods produce comparable results. In terms of runtime, the LIM simulation required 1.59 seconds for 1200 time steps while SPECTRE required 22.24 seconds for 1146 time steps. We see that LIM is about 14× faster in this example. The advantage of LIM in terms of run-time is expected to increase as the circuit size increases, as LIM exhibits a linear numerical complexity with respect to the number of nodes [12].

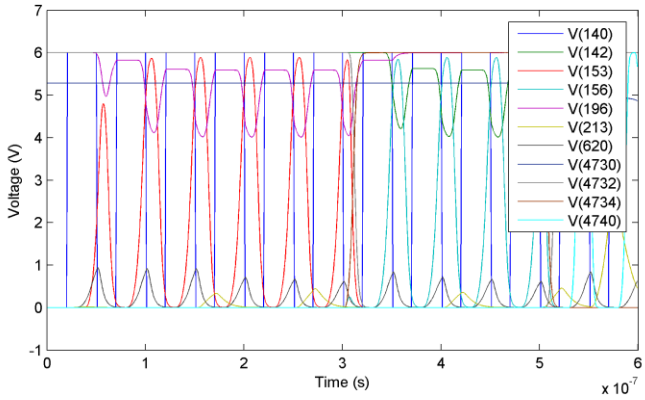

Fig. 5. LIM simulation of RAM circuit.

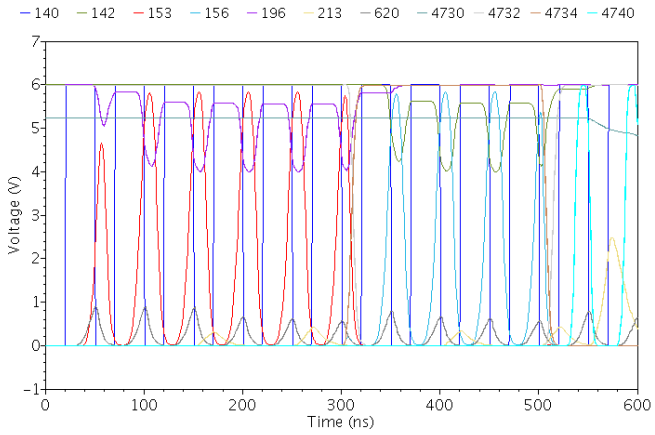

Fig. 6. SPECTRE simulation of RAM circuit.

B. Ripple-carry Adder

In this example, a chain of eight ripple-carry adders is simulated in order to illustrate an application of the multi-rate simulation technique. The circuit is shown in Fig. 7 where each NAND is as shown in Fig. 3. The regular LIM required the use of a 0.1 ns time step in order to obtain a stable result while the multi-rate LIM operated at time steps of 0.1 ns and 10 ns as explained in section IV. The total simulation time was 2 μs which resulted in 20,000 time steps. In the LIM simulation, the CMOS model is evaluated 5,759,712 times while the nodes were evaluated a total of 2,899,855 times. On

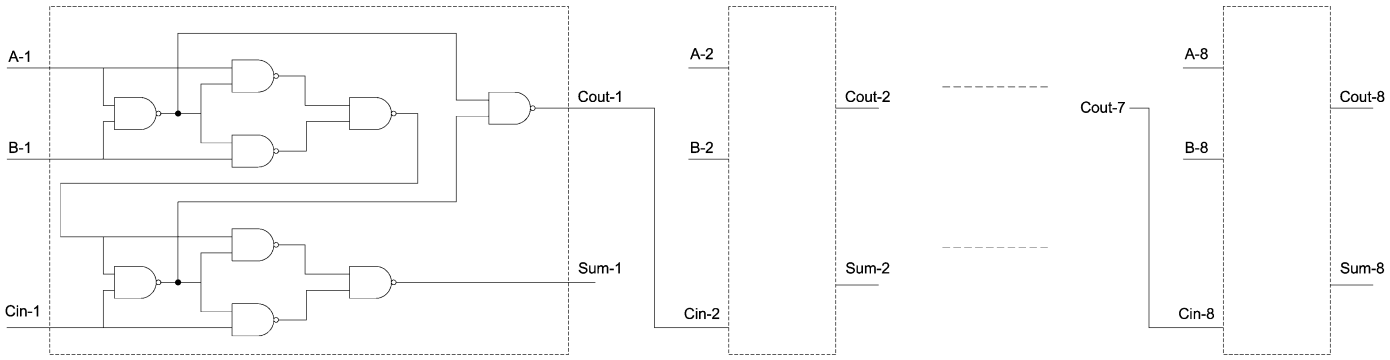

Fig. 7. Chain of eight ripple-carry adders.

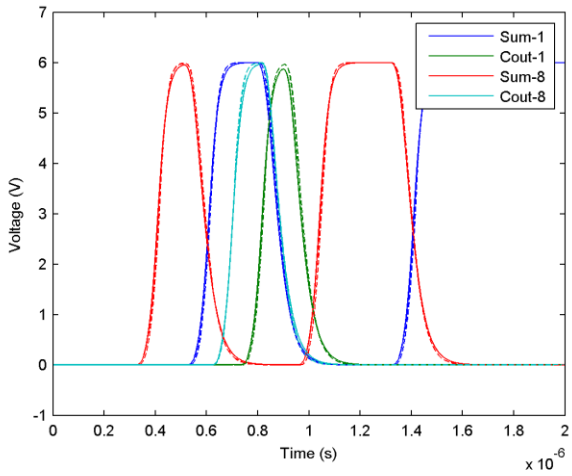

Fig. 8. Simulation of ripple-carry adders in LIM (solid lines) and multi-rate LIM (dotted lines).

the other hand, in the multi-rate LIM, the CMOS model is evaluated 2,908,800 times while the nodes were evaluated a total of 1,474,399 times. We see that by using the multi-rate technique, we are able to cut down the number of node and branch evaluations by almost a factor of one half for this circuit. Fig. 8 shows the simulation result at the output of the first and last ripple-carry adders for both the regular LIM and the multi-rate LIM. Comparable accuracy is observed between the two.

VI. Conclusion

In this work, we have applied the latency insertion method to the simulation of larger CMOS circuits and compared it to traditional SPICE based methods. It is found that LIM is able to simulate CMOS circuits as accurate as SPICE while being over an order of magnitude faster. This speed-up is expected to increase as the circuit size is increased due to the linear numerical complexity of LIM. In addition, the multi-rate simulation technique has been successfully applied to the simulation of CMOS circuits and its computational efficiency over the traditional LIM has been illustrated.

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