Partitioned Latency Insertion Method with a Generalized Stability Criteria

Patrick Goh, José E. Schutt-Ainé, *Fellow, IEEE*, Dmitri Klokotov, Jilin Tan, *Senior Member, IEEE*, Ping Liu, Wenliang Dai, and Feras Al-Hawari

***Abstract*— This paper presents a modular approach to the high-frequency simulation of large networks. By utilizing the latency insertion method (LIM) and by studying the stability criteria of partitions of different latencies in the circuit, a robust method is formulated that is able to perform transient simulations significantly faster than the conventional LIM method. The LIM method is also extended to handle dependent sources, and a general stability criterion for selecting the time step, independent of the topology of the circuit, is proposed. The new method is verified with existing commercial tools for circuit simulations, and the improvement in run time is also depicted.**

***Index Terms*— Circuit simulation, dependent sources, latency insertion method, partitioned latency insertion method, stability.**

I. Introduction

With the increase in the density of interconnects and the complexity of high-speed packages, signal integrity becomes an important aspect in the design of modern devices. Circuit designers are constantly in need of newer and better methods that are able to capture the complicated electromagnetic behaviors of complex circuits. In this aspect, the ability to accurately simulate large circuits in a reasonable amount of time is invaluable in the design of any circuit. As a result, there is a constant need and push toward faster circuit simulation methods that are able to handle large circuits in a fraction of the time taken by conventional circuit simulators.

The latency insertion method (LIM) [1] has recently emerged as an efficient approach for performing fast simulations of very large circuits. By exploiting latencies in the circuit, LIM is able to solve the voltages and the currents in the circuit explicitly at each time step. This results in a computationally efficient algorithm that is able to simulate large circuits significantly faster than conventional matrix inversion–based methods such as SPICE [2].

The two main advantages of LIM over SPICE-like simulators for transient simulations are its linear numerical complexity and its linear memory requirement [3]. For this reason, LIM is most efficiently used for solving large circuits where the number of elements is in the order of millions. For example, in [4]–[8], LIM has been used in both the transient and steady-state analysis of power distribution networks, where the usage of conventional simulators is prohibited by the large circuit size. In addition, LIM is also well suited to handle simulations of high-frequency circuits such as the tightly coupled transmission lines [9], [10] and circuits with frequency-dependent effects [11]–[13]. On the other hand, one of the disadvantages of LIM is its reliance on latency elements in the circuit in order to perform its time-stepping algorithm. The LIM algorithm is only conditionally stable, with an upper bound on the maximum time step which depends mainly on the smallest inductance and capacitance in the circuit. When the circuit contains very small latency elements, the time step required for a stable simulation could be equally small, which would result in a large number of time steps in a transient simulation. In order to alleviate this problem, a block-processing technique has been proposed [14]–[16], which utilizes different time steps for different parts of the circuit. However, selecting the maximum time step for each part of the circuit is still a challenging task, and the basic method used in [14]–[16] to select the time step can only be applied under very restrictive assumptions [17]. Specifically, each node in the circuit has to be connected to only two branches, and the values of the circuit elements have to be the same everywhere in each subcircuit. In this paper, we propose a more robust method to select the maximum time step of the LIM simulation, which is independent of the circuit topology. We then apply the method, along with the block-processing technique, to the simulation of circuits with partitions of different latencies, and demonstrate the accuracy and speed improvements of the proposed method over the basic LIM. In addition, we will also extend the basic LIM to handle dependent sources.

The remainder of this paper is organized as follows. Section II reviews the basic LIM formulation. Section III presents the matrix version of the semi-implicit LIM formulation, along with the usage of the amplification matrix to predict the stability of a time step. Section IV details the modification to the circuit parameter matrices to include dependent sources, and the resulting modifications to the amplification matrix. Section V will present the usage of multiple time steps to simulate circuits with partitions of different latencies, by applying the amplification matrix to select the time steps for each partition, and the speed improvement over the regular LIM.

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P. Goh, J. E. Schutt-Ainé, and D. Klokotov are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA (e-mail: pgoh@illinois.edu; jschutt@emlab.uiuc.edu; dklokot2@illinois.edu).

J. Tan, P. Liu, W. Dai, and F. Al-Hawari are with Cadence Design Systems, Inc., Chelmsford, MA 01824 USA (e-mail: tanjilin@gmail.com; liuping@cadence.com; wldai@cadence.com; feras@cadence.com).

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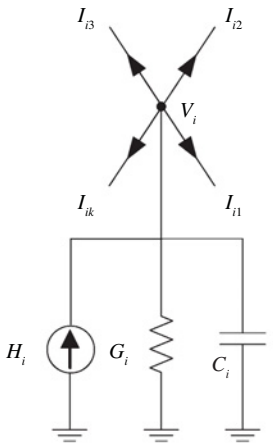

Fig. 1. Node topology.

Numerical results are shown in Section VI, and a conclusion is given in Section VII.

II. Basic LIM Formulation

In this section, the formulation of the basic LIM will be reviewed. LIM can be applied to any arbitrary network, where it is assumed that through the use of Thévenin and Norton transformations, the branches and nodes of the circuit can be described by a general topology. Each node is represented by a parallel combination of a current source, a conductance, and a capacitor to ground. The connection between two different nodes forms a branch and it is represented by a series combination of a voltage source, a resistor, and an inductor. Fig. 1 shows a node i with k branches connected to it, while Fig. 2 shows a branch connecting nodes i and j. The voltage at node i is defined as V_i while the current flowing from node i to j is defined as I_{ij}. In order to solve for the voltages and currents in the circuit, LIM discretizes the time variable whereby the voltages and currents are collated in half time steps. Specifically, the voltages are solved at half time steps while the currents are solved at full time steps. From Fig. 1, writing Kirchhoff's current law (KCL) at node i yields

$$C_i\left(\frac{V_i^{\frac{n+1}{2}}-V_i^{\frac{n-1}{2}}}{\Delta t}\right)+G_iV_i^{\frac{n+1}{2}}-H_i^n=-\sum_{k=1}^{M_i}I_{ik}^n \quad (1)$$

where the superscript n is the index of the current time step, Δt is the time step, and M_i is the number of branches connected to node i. Solving for the unknown voltage yields

$$V_i^{\frac{n+1}{2}}=\frac{\frac{C_iV_i^{\frac{n-1}{2}}}{\Delta t}+H_i^n-\sum_{k=1}^{M_i}I_{ik}^n}{\frac{C_i}{\Delta t}+G_i} \quad (2)$$

for $i=1,2,\ldots,N_n$, where N_n is the number of nodes in the circuit.

From Fig. 2, writing Kirchhoff's voltage law (KVL) at branch ij yields

$$V_i^{\frac{n+1}{2}}-V_j^{\frac{n+1}{2}}=L_{ij}\left(\frac{I_{ij}^{n+1}-I_{ij}^n}{\Delta t}\right)+R_{ij}I_{ij}^n-E_{ij}^{\frac{n+1}{2}}. \quad (3)$$

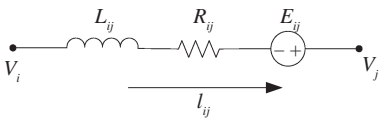

Fig. 2. Branch topology.

Solving for the unknown current yields

$$I_{ij}^{n+1}=I_{ij}^n+\frac{\Delta t}{L_{ij}}\left(V_i^{\frac{n+1}{2}}-V_j^{\frac{n+1}{2}}-R_{ij}I_{ij}^n+E_{ij}^{\frac{n+1}{2}}\right). \quad (4)$$

The computation of the node voltages and the branch currents are alternated as time progresses in a leapfrog manner. In this aspect, LIM is similar to Yee's algorithm for the solution of Maxwell's equations in the finite difference time domain (FDTD) method [18]. It is clear that the LIM algorithm relies on the latencies in the network to perform the leapfrog time-stepping formulation. Thus, at every node, a capacitor to ground has to be present. If it is not, a small fictitious capacitor is inserted. Similarly, small fictitious inductors are inserted into branches without latencies. The effects of these fictitious elements on the accuracy of the general LIM has been studied in [3]. In Section V, we will examine the effects of these elements on the speed of the LIM and propose a generalized solution to improve the speed of the simulations of circuits with partitions of different latencies.

As with the traditional FDTD method [18], LIM is only conditionally stable. In other words, there is an upper bound on the time step that will result in a numerically stable solution to (2) and (4). Previous work on the subject has resulted in an analytical stability condition on the time step for stable simulations in the case of resistance-inductance-capacitance (RLC) and gate-level characterization (GLC) circuits [3], [19]. However, there has not been any analytical method to predict the stability of a time step for a general RLGC circuit. In Section III, we will show a numerical method to predict the stability of a time step for any general circuit topology. Since this method does not impose any requirement on the circuit topology, it can also be used to predict the stability of a time step in the presence of dependent sources as will be shown in Section IV.

III. Vector-Matrix Semi-Implicit LIM Formulation

In this section, the formulation of the vector-matrix version of the semi-implicit LIM [20] will be reviewed. From (1), we may write the semi-implicit formulation as

$$C_i\left(\frac{V_i^{\frac{n+1}{2}}-V_i^{\frac{n-1}{2}}}{\Delta t}\right)+G_i\left(\frac{V_i^{\frac{n+1}{2}}+V_i^{\frac{n-1}{2}}}{2}\right)-H_i^n=-\sum_{k=1}^{M_i}I_{ik}^n. \quad (5)$$

Equation (5) can then be written in a vector-matrix formulation as

$$\mathbf{C}\left(\frac{\mathbf{v}^{\frac{n+1}{2}}-\mathbf{v}^{\frac{n-1}{2}}}{\Delta t}\right)+\frac{1}{2}\mathbf{G}\left(\mathbf{v}^{\frac{n+1}{2}}+\mathbf{v}^{\frac{n-1}{2}}\right)-\mathbf{h}^{\mathbf{n}}=-\mathbf{M}\mathbf{i}^{\mathbf{n}} \quad (6)$$

where $\mathbf{v}$ is the node voltage vector of dimension N_n, $\mathbf{i}$ is the branch current vector of dimension N_b, $\mathbf{C}$ and $\mathbf{G}$ are diagonal matrices, respectively, of dimensions $N_n \times N_n$, with the values of the capacitors and conductances at each node on the main diagonal, $\mathbf{h}$ is a vector of dimension N_n containing all the current sources at the nodes, and $\mathbf{M}$ is the $N_n \times N_b$ incidence matrix defined as follows:

$$M_{qp} = 1 \quad if\ branch\ \ p\ is\ incident\ at\ node\ q\ and\ the\ current\ flows\ away\ from\ node\ q.$$
$$M_{qp} = -1 \quad if\ branch\ \ p\ is\ incident\ at\ node\ q\ and\ the\ current\ flows\ into\ node\ q.$$
$$M_{qp} = 0 \quad if\ branch\ \ p\ is\ not\ incident\ at\ node\ q.$$

Solving (6) for $\mathbf{v}^{n+1/2}$ yields

$$\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left[\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2}\right)\mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}} + \mathbf{h^n} - \mathbf{Mi^n}\right]. \tag{7}$$

Similarly, we may write the semi-implicit formulation of (3) in vector-matrix form as

$$\mathbf{M^T v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} = \frac{\mathbf{L}}{\Delta t}\left(\mathbf{i^{n+1}} - \mathbf{i^n}\right) + \frac{\mathbf{R}}{2}\left(\mathbf{i^{n+1}} + \mathbf{i^n}\right) - \mathbf{e}^{\frac{\mathbf{n+1}}{\mathbf{2}}} \tag{8}$$

where $\mathbf{L}$ and $\mathbf{R}$ are diagonal matrices, of dimensions $N_b \times N_b$, with the values of the inductances and resistances at each branch on the main diagonal, and $\mathbf{e}$ is a vector of dimension N_b containing all the voltage sources at the branches. Solving (8) for $\mathbf{i}^{n+1}$ yields

$$\mathbf{i^{n+1}} = \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R}}{2}\right)^{-1}\left[\left(\frac{\mathbf{L}}{\Delta t} - \frac{\mathbf{R}}{2}\right)\mathbf{i^n} + \mathbf{e}^{\frac{\mathbf{n+1}}{\mathbf{2}}} + \mathbf{M^T v}^{\frac{\mathbf{n+1}}{\mathbf{2}}}\right]. \tag{9}$$

Equations (7) and (9) can then be used in place of (2) and (4) as the update equations to calculate the voltage and currents at each time step.

The advantage of the vector-matrix formulation lies in its ability to accurately predict if a time step will be stable. To see this, we return to (7) and (9) and expand them to get

$$\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} = \mathbf{P_+P_-v}^{\frac{\mathbf{n-1}}{\mathbf{2}}} - \mathbf{P_+Mi^n} + \mathbf{P_+h^n} \tag{10}$$
$$\mathbf{i^{n+1}} = \mathbf{Q_+Q_-i^n} + \mathbf{Q_+M^T v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} + \mathbf{Q_+e}^{\frac{\mathbf{n+1}}{\mathbf{2}}} \tag{11}$$

where we have made the definitions

$$\mathbf{P_+} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1} \quad \mathbf{P_-} = \left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2}\right) \tag{12}$$
$$\mathbf{Q_+} = \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R}}{2}\right)^{-1} \quad \mathbf{Q_-} = \left(\frac{\mathbf{L}}{\Delta t} - \frac{\mathbf{R}}{2}\right). \tag{13}$$

Substituting (10) into (11) and rearranging the terms, we obtain

$$\mathbf{i^{n+1}} = \mathbf{Q_+M^T P_+P_-v}^{\frac{\mathbf{n-1}}{\mathbf{2}}} + \left(\mathbf{Q_+Q_-} - \mathbf{Q_+M^T P_+M}\right)\mathbf{i^n} + \mathbf{Q_+e}^{\frac{\mathbf{n+1}}{\mathbf{2}}} + \mathbf{Q_+M^T P_+h^n}. \tag{14}$$

Equations (10) and (14) can then be grouped together to obtain

$$\begin{bmatrix}\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} \\ \mathbf{i^{n+1}}\end{bmatrix} = \begin{bmatrix}\mathbf{P_+P_-} & -\mathbf{P_+M} \\ \mathbf{Q_+M^T P_+P_-} & \mathbf{Q_+Q_-} - \mathbf{Q_+M^T P_+M}\end{bmatrix} \times \begin{bmatrix}\mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}} \\ \mathbf{i^n}\end{bmatrix} + \begin{bmatrix}0 & \mathbf{P_+} \\ \mathbf{Q_+} & \mathbf{Q_+M^T P_+}\end{bmatrix}\begin{bmatrix}\mathbf{e}^{\frac{\mathbf{n+1}}{\mathbf{2}}} \\ \mathbf{h^n}\end{bmatrix}. \tag{15}$$

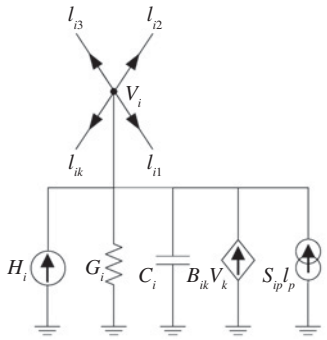

Fig. 3. Node topology with dependent sources.

Equation (15) defines a discrete linear time invariant (DLTI) system in the form of

$$x(t+1) = Ax(t) + Bu(t). \tag{16}$$

Theorem 1: The DLTI given in (16) is asymptotically stable if and only if all the eigenvalues of $\mathbf{A}$ have magnitude strictly smaller than 1. The reader is referred to [21] for a proof of this theorem.

Comparing (15) and (16), we define matrix $\mathbf{A}$ as

$$A = \begin{bmatrix}\mathbf{P_+P_-} & -\mathbf{P_+M} \\ \mathbf{Q_+M^T P_+P_-} & \mathbf{Q_+Q_-} - \mathbf{Q_+M^T P_+M}\end{bmatrix} \tag{17}$$

and call it the amplification matrix since in the absence of input, the voltages and the currents in the circuit will be amplified by matrix $\mathbf{A}$ at each time step. From Theorem 1, we see that *all the eigenvalues of the amplification matrix defined in (17) must have magnitude strictly smaller than* 1 for the simulation to be stable. Thus, we can use the amplification matrix to predict the stability of a time step Δt.

IV. Dependent Sources

In this section, we develop the voltage and current update equations in the presence of dependent sources, and the resulting modification to the amplification matrix.

Fig. 3 shows the node topology with a voltage-controlled current source (VCCS) and a current-controlled current source (CCCS) connected to it. Writing the KCL at the node, in semi-implicit form, gives

$$C_i\left(\frac{V_i^{\frac{n+1}{2}} - V_i^{\frac{n-1}{2}}}{\Delta t}\right) + G_i\left(\frac{V_i^{\frac{n+1}{2}} + V_i^{\frac{n-1}{2}}}{2}\right) - H_i^n - B_{ik}\left(\frac{V_k^{\frac{n+1}{2}} + V_k^{\frac{n-1}{2}}}{2}\right) - S_{ip}I_p^n = -\sum_{k=1}^{M_i} I_{ik}^n \tag{18}$$

where B_{ik} is the coefficient of the VCCS at node i due to node k and S_{ip} is the coefficient of the CCCS at node i due to branch p. Equation (18) can then be written in vector-matrix form as

$$\mathbf{C}\left(\frac{\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} - \mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}}}{\Delta t}\right) + \frac{1}{2}\mathbf{G}\left(\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} + \mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}}\right) - \mathbf{h^n} - \frac{1}{2}\mathbf{B}\left(\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}} + \mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}}\right) - \mathbf{Si^n} = -\mathbf{Mi^n}. \tag{19}$$

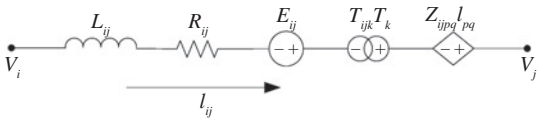

Fig. 4. Branch topology with dependent sources.

which can be rearranged to read

$$\mathbf{C}\left(\frac{\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}}-\mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}}}{\Delta t}\right)+\frac{1}{2}\mathbf{G}'\left(\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}}+\mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}}\right)-\mathbf{h}^{\mathbf{n}}=-\mathbf{M}'\mathbf{i}^{\mathbf{n}} \quad (20)$$

where

$$\mathbf{G}'=\mathbf{G}-\mathbf{B} \text{ and } \mathbf{M}'=\mathbf{M}-\mathbf{S}. \quad (21)$$

Solving (20) for $\mathbf{v}^{n+1/2}$ yields

$$\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}}=\left(\frac{\mathbf{C}}{\Delta t}+\frac{\mathbf{G}'}{2}\right)^{-1}\left[\left(\frac{\mathbf{C}}{\Delta t}-\frac{\mathbf{G}'}{2}\right)\mathbf{v}^{\frac{\mathbf{n-1}}{\mathbf{2}}}+\mathbf{h}^{\mathbf{n}}-\mathbf{M}'\mathbf{i}^{\mathbf{n}}\right] \quad (22)$$

which is the voltage update equation in the presence of dependent sources.

Fig. 4 shows the branch topology with a voltage-controlled voltage source (VCVS) and a current-controlled voltage source (CCVS) connected to it. KVL at the branch, in semi-implicit form, gives

$$V_i^{\frac{n+1}{2}}-V_j^{\frac{n+1}{2}}=L_{ij}\left(\frac{I_{ij}^{n+1}-I_{ij}^{n}}{\Delta t}\right)+R_{ij}\left(\frac{I_{ij}^{n+1}+I_{ij}^{n}}{2}\right)$$
$$-E_{ij}^{\frac{n+1}{2}}-T_{ijk}V_k^{\frac{n+1}{2}}-Z_{ijpq}\left(\frac{I_{pq}^{n+1}+I_{pq}^{n}}{2}\right) \quad (23)$$

where T_{ijk} is the coefficient of the VCVS at branch ij due to node k, and Z_{ijpq} is the coefficient of the CCVS at branch ij due to branch pq. Writing (23) in vector-matrix form and rearranging the terms, we obtain

$$\mathbf{M}^{\mathbf{T}'}\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}}=\frac{\mathbf{L}}{\Delta t}\left(\mathbf{i}^{\mathbf{n+1}}-\mathbf{i}^{\mathbf{n}}\right)+\frac{\mathbf{R}'}{2}\left(\mathbf{i}^{\mathbf{n+1}}+\mathbf{i}^{\mathbf{n}}\right)-\mathbf{e}^{\frac{\mathbf{n+1}}{\mathbf{2}}} \quad (24)$$

where

$$\mathbf{M}^{\mathbf{T}'}=\mathbf{M}^{\mathbf{T}}+\mathbf{T} \text{ and } \mathbf{R}'=\mathbf{R}-\mathbf{Z}. \quad (25)$$

Solving (24) for $\mathbf{i}^{n+1}$ yields

$$\mathbf{i}^{\mathbf{n+1}}=\left(\frac{\mathbf{L}}{\Delta t}+\frac{\mathbf{R}'}{2}\right)^{-1}\left[\left(\frac{\mathbf{L}}{\Delta t}-\frac{\mathbf{R}'}{2}\right)\mathbf{i}^{\mathbf{n}}+\mathbf{e}^{\frac{\mathbf{n+1}}{\mathbf{2}}}+\mathbf{M}^{\mathbf{T}'}\mathbf{v}^{\frac{\mathbf{n+1}}{\mathbf{2}}}\right]. \quad (26)$$

Equations (22) and (26) then give the new update equations for circuits with dependent sources. Note that in the absence of dependent sources, all the **G'**, **M'**, $\mathbf{M}^{T}$', and **R'** will converge to **G**, **M**, $\mathbf{M}^{T}$,and **R**, and (22) and (26) will converge to (7) and (9) as expected.

In order to analyze the stability of a time step in the presence of dependent sources, we proceed as in Section III, to obtain the new amplification matrix **A/**, where we now have

$$A'=\begin{bmatrix}\mathbf{P}'_+\mathbf{P}'_- & -\mathbf{P}'_+\mathbf{M}' \\ \mathbf{Q}'_+\mathbf{M}^{\mathbf{T}'}\mathbf{P}'_+\mathbf{P}'_- & \mathbf{Q}'_+\mathbf{Q}'_- - \mathbf{Q}'_+\mathbf{M}^{\mathbf{T}'}\mathbf{P}'_+\mathbf{M}'\end{bmatrix} \quad (27)$$

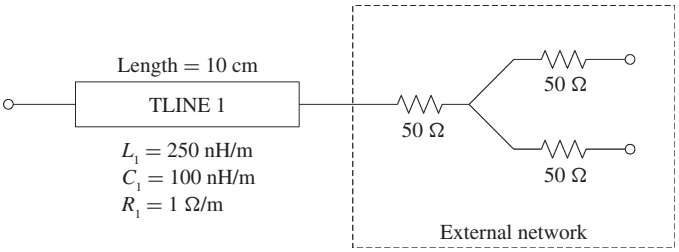

Fig. 5. Transmission line connected to an external network.

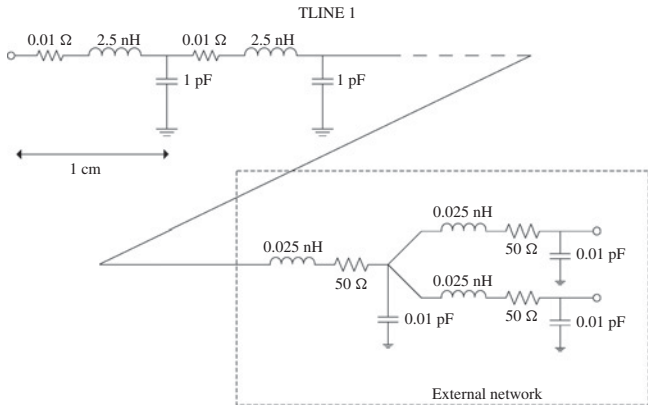

Fig. 6. LIM enabled circuit.

where

$$\mathbf{P}'_+=\left(\frac{\mathbf{C}}{\Delta t}+\frac{\mathbf{G}'}{2}\right)^{-1} \quad \mathbf{P}'_-=\left(\frac{\mathbf{C}}{\Delta t}-\frac{\mathbf{G}'}{2}\right) \quad (28)$$

$$\mathbf{Q}'_+=\left(\frac{\mathbf{L}}{\Delta t}+\frac{\mathbf{R}'}{2}\right)^{-1} \quad \mathbf{Q}'_-=\left(\frac{\mathbf{L}}{\Delta t}-\frac{\mathbf{R}'}{2}\right). \quad (29)$$

From Theorem 1, we see that *all the eigenvalues of the amplification matrix* **A'**, *defined in* (27), *must have magnitude strictly smaller than* 1 for the simulation with dependent sources to be stable. This is written compactly as follows:

$$\left|\lambda_i\left(A'(\Delta t)\right)\right|<1 \qquad i=1,2,\ldots,N_n+N_b. \quad (30)$$

Thus, we can use the new amplification matrix **A'**, to predict the stability of a time step Δt in the presence of dependent sources.

V. Simulating Circuits with Partitions of Different Latencies

In this section, we present a robust method to simulate circuits with partitions of different latencies. We first illustrate the motivation of the method via an example. Consider a case where LIM is used to simulate a circuit consisting of a transmission line TLINE 1 connected to a purely resistive external network as shown in Fig. 5. The transmission line has RLCG values shown in Fig. 5 where for simplicity we have assumed that G = 0 such that the method presented in [3] for selecting the time step for an RLC circuit can be applied. In order to simulate this circuit in LIM, we model the transmission line with 10 segments of RLC lumped elements, and insert fictitious latency elements into the external network

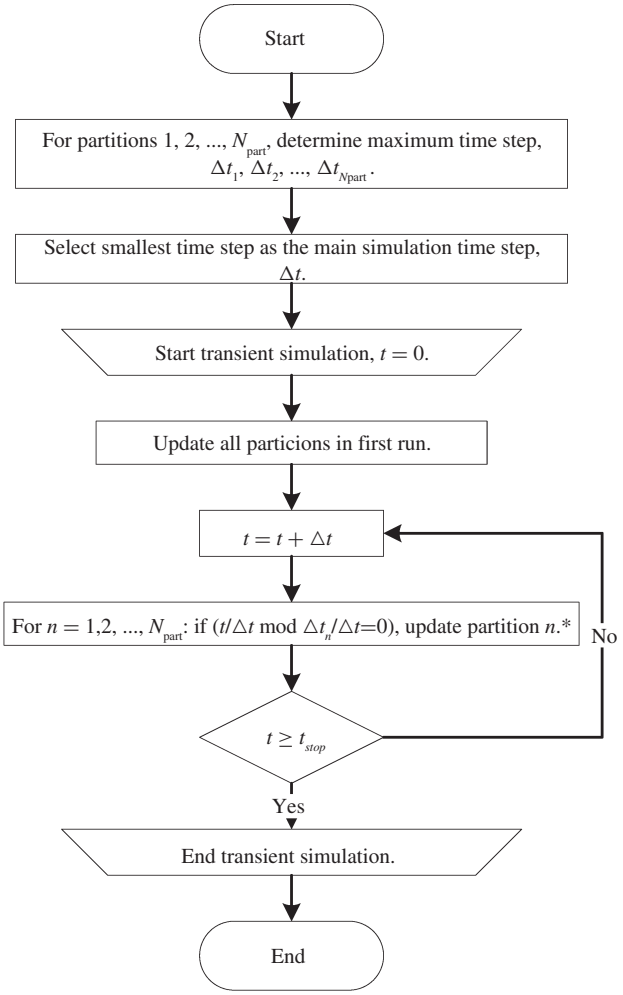

Fig. 7. Simulation algorithm for partitioned LIM.

as shown in Fig. 6, where the fictitious elements have been made small so as not to affect the accuracy of the solution.

The time step required for a stable simulation of this RLC circuit can then be shown to be [3]

$$\Delta t < \sqrt{2} \min_{i=1}^{N_n} \left(\sqrt{\frac{C_i}{M_i} \min_{p=1}^{M_i} \left(L_{i,p} \right)} \right) < \sqrt{2} \left(\sqrt{\frac{0.01p}{3} 0.025n} \right) = 4.08 \times 10^{-13}\text{s} \quad (31)$$

where $L_{i,p}$ denotes the value of the pth inductor connected to node i. Notice that in this case, the L and C of the external network completely determine the maximum time step. In other words, the maximum time step to ensure stability is dictated by the section with the smallest latency. However, note that if we had considered a circuit with only the transmission line TLINE 1, the maximum time step would have been

$$\Delta t < \sqrt{2.5n \cdot 1p} = 5 \times 10^{-11}\text{s}. \quad (32)$$

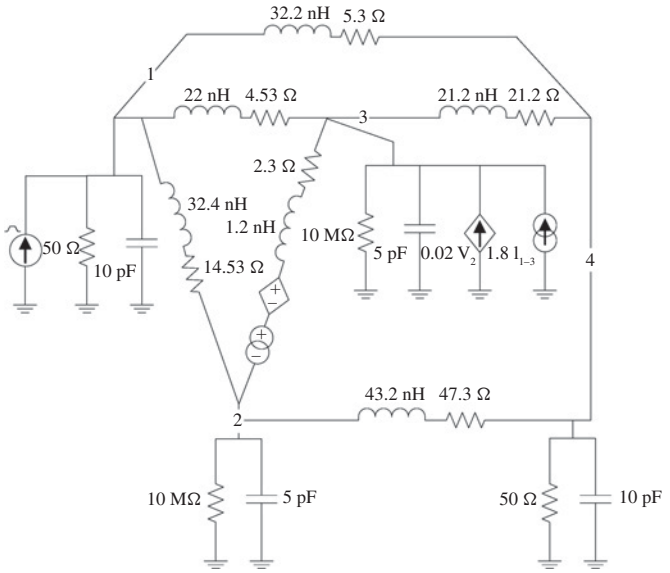

Fig. 8. Circuit in example A.

This suggests that the section with higher latency can be simulated with a larger time step without violating the stability criteria.

Consider then the following method for simulating circuits with partitions of different latencies. First, a stable time step is determined for each partition. In the case of an RLC or a GLC circuit, the method in [3] and [19] is employed as shown in (31). However, for a general circuit (or in the presence of dependent sources), (31) cannot be applied and the more general numerical method presented in Theorem 1 must be used. Once all the time steps have been determined, the smallest time step is used in LIM to simulate the circuit, but each partition is updated only as needed, depending on its maximum stable time step. This results in a computationally efficient algorithm, with large speed-ups in the simulation time, especially when the partition with the smallest latency is small compared to the rest of the circuit. The method is summarized in Fig. 7.

VI. Numerical Results

In this section, the methods presented in Section IV and V are applied to perform simulations of circuits using LIM in the presence of dependent sources and with partitions of different latencies. First, the formulation in Section IV is used to simulate a circuit with four dependent sources (VCCS, CCCS, VCVS, and CCVS). In order to validate the method, the same circuit is simulated in SPECTRE [22], a commercial circuit solver from Cadence Design Systems utilizing the modified nodal analysis (CS-MNA) method, and the results are compared. Next, the usage of multiple time steps is depicted with an example circuit with partitions of different latencies. Speed improvements over the conventional LIM will be illustrated.

A. Dependent Sources

In this example, the circuit shown in Fig. 8 is simulated in the LIM environment. It is assumed that all the branches and

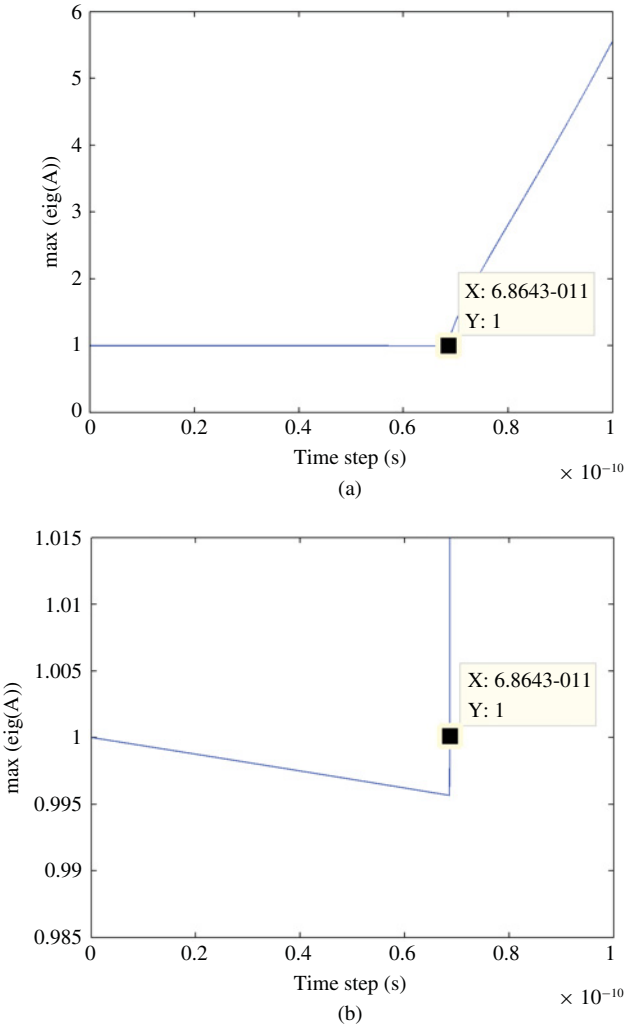

Fig. 9. Sweep of eigenvalues of the amplification matrix, A. (a) Broad view. (b) Expanded view.

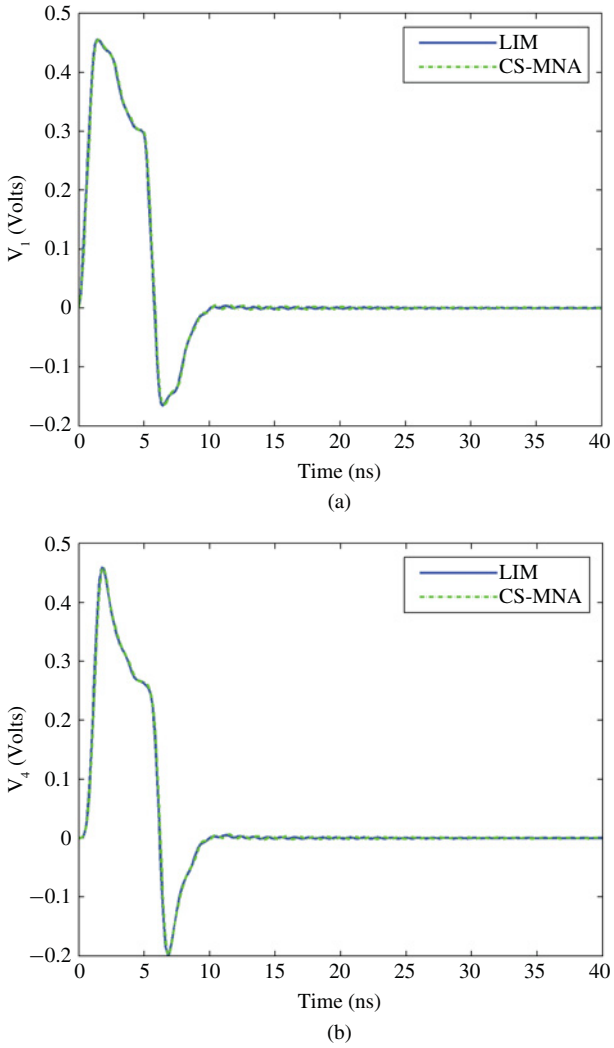

Fig. 10. Simulation of circuit in Fig. 8 with $\triangle t = 6.8 \times 10^{-11}$ s. (a) Voltage at node 1. (b) Voltage at node 4.

the nodes in the circuit have inherent latencies as shown in the figure such that no fictitious elements have to be inserted. The input is a current source with a single trapezoidal pulse of rise and fall times equal to 1 ns and a pulse width of 4 ns. The maximum amplitude is 0.02 A. In order to validate Theorem 1 and the subsequent result in (30), a sweep of the eigenvalues of the amplification matrix **A** is performed and the maximum time step for stability is determined from where the magnitude of the maximum eigenvalue equals 1. This is shown in Fig. 9. Note that in practice, this process can be time consuming, especially when the circuit under consideration is large. In that case, the circuit can be partitioned into multiple segments, and the method presented in Section V can be used to simulate the different partitions with different time steps. Also, a more effective search algorithm can be employed to determine the maximum time step.

From Fig. 9, the maximum time step is determined to be $\Delta t_{\max} < 6.864 \times 10^{-11}$s. We then perform two transient simulations, first using a time step slightly smaller than the maximum time step, and then using a time step slightly larger than the maximum time step. Plots of the resulting waveforms at the input (node 1) and output (node 4) are shown in Fig. 10. We see that the simulation using the properly chosen time step

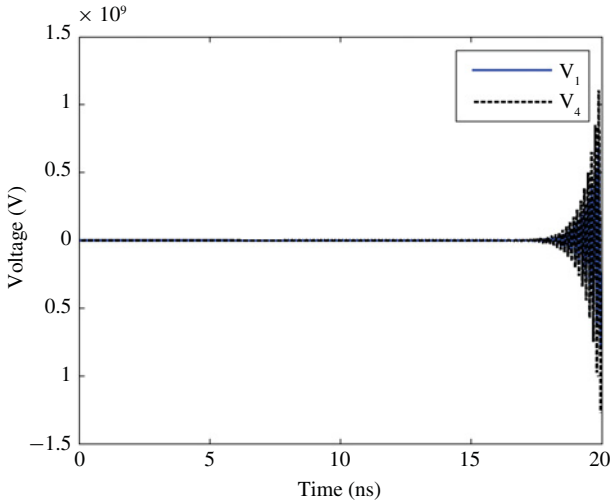

Fig. 11. Simulation of circuit in Fig. 8 with $\triangle t = 6.9 \times 10^{-11}$ s.

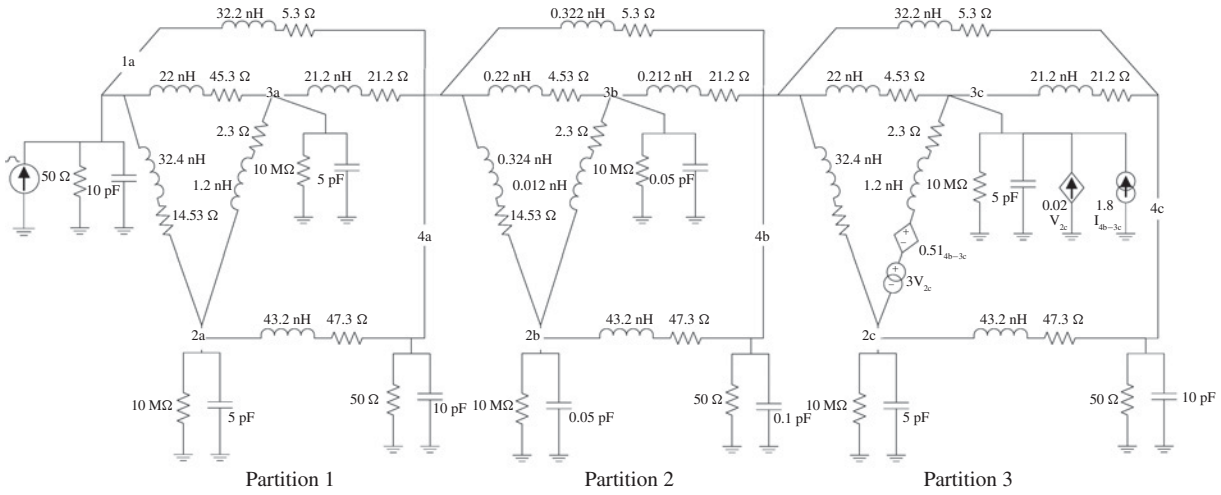

Fig. 12. Circuit in example B.

results in a stable and accurate solution, which can be seen from the comparison with the CS-MNA shown in Fig. 10. On the other hand, the simulation using the time step slightly larger than $\Delta t_{\max}$ results in an unstable simulation as can be seen in Fig. 11. Note that selecting a time step to ensure stability does not necessarily ensure accuracy. In general, the time step must also be small enough for sufficient accuracy. However, typically for an LIM simulation, the time step to ensure stability is small enough such that the accuracy is also preserved.

B. Multiple Time Steps for Partitions of Different Latencies

In this example, the circuit in Fig. 12 is simulated in the LIM environment. The circuit consists of three partitions detailed as follows.

1) Partition 1: High-latency partition.
2) Partition 2: Low-latency partition. (In practice, this could be a partition with no latency, whereby small fictitious elements have been inserted to enable LIM.)
3) Partition 3: Dependent sources.

Using the method in Sections III and IV, the maximum time step of each partition is determined to be $\Delta t_1 = 1.0486 \times 10^{-10}$ s, $\Delta t_2 = 1.07 \times 10^{-12}$ s, and $\Delta t_3 = 6.741 \times 10^{-11}$ s, corresponding to partitions 1, 2, and 3, respectively. Note that we have chosen the time steps to be the integer multiples of the smallest time step (in this case Δt_2) as mentioned in Section V.

The circuit is then simulated using the algorithm in Fig. 7 for performing LIM with partitions of different latencies, that is, partitioned latency insertion method (PLIM), and the results at the input (node 1a) and output (node 4c) are shown in Fig. 13. Next, the same circuit is simulated using the traditional LIM with time step $\Delta t = \Delta t_2 = 1.07 \times 10^{-12}$ s and the results are also plotted in Fig. 13. No loss in accuracy is observed when using PLIM compared to the regular LIM.

Next, PLIM is used to simulate a large circuit where the partition with the smallest latency is small compared to the rest of the circuit. To construct this circuit, partition 1 is cascaded N times and the simulation time is recorded for PLIM and LIM. The results are summarized in Table I. We observe that

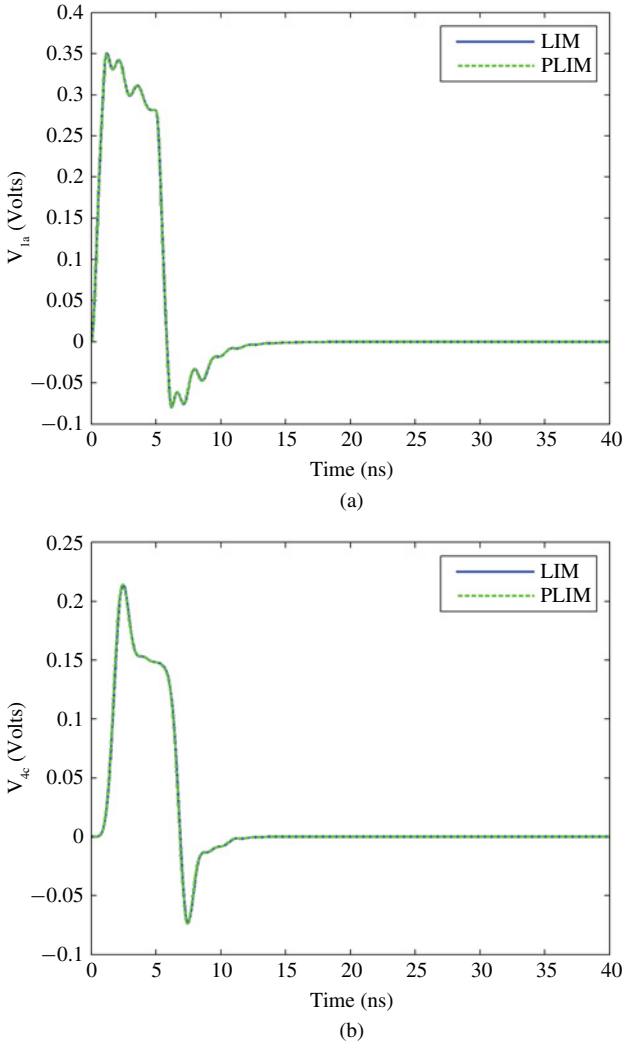

Fig. 13. Simulation of circuit in Fig. 12. (a) Voltage at node 1a. (b) Voltage at node 4c.

TABLE I
COMPARISON OF RUN TIMES

N	LIM (s)	PLIM (s)	Speed-up
1	0.11	0.01	11.0
10	0.23	0.02	11.5
100	1.40	0.03	46.7
500	7.15	0.08	89.4
1000	13.52	0.15	90.1
2000	26.21	0.28	93.6
5000	64.52	0.68	94.9

when the sizes of the partitions are comparable, a small speed-up is obtained when using PLIM. On the other hand, when the partition with the smallest latency is small compared to the rest of the circuit, a large speed-up is obtained which approaches the limit of $\Delta t_{\text{large}}/\Delta t_{\text{min}}$where Δt_{large} is the time step of the largest partition and Δt_{min} is the smallest time step in the circuit, which also dictates the maximum time step of the regular LIM.

VII. CONCLUSION

An improved version of the LIM, called PLIM, has been proposed. The PLIM is capable of simulating large circuits with partitions of different latencies significantly faster than the conventional LIM. The LIM method has also been extended to handle dependent sources, and a general stability condition for selecting the time step of the simulation has been shown. The validity of the method has been verified and significant speed-ups were observed when using the new method.

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Patrick Goh received the B.S. and M.S. degrees in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC), Urbana, in 2007 and 2009, respectively, where he is currently pursuing the Ph.D. degree.

He has held a Teaching Assistant position with the Department of Electrical and Computer Engineering, UIUC, since August 2007. His current research interests include circuit simulation for high-speed interconnects, modeling, and computer-aided design tools.

Mr. Goh is a reviewer for the IEEE TRANSACTIONS ON ADVANCED PACKAGING and the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY.

José E. Schutt-Ainé (S'86–M'86–SM'98–F'07) received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, in 1981, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC), Urbana, in 1984 and 1988, respectively.

He joined Hewlett-Packard Technology Center, Santa Rosa, CA, as an Application Engineer involved with microwave transistors and high-frequency circuits. In 1983, he joined UIUC, and then joined the Electrical and Computer Engineering Department as a member of the Electromagnetics and Coordinated Science Laboratories where he currently specializes in the study of signal integrity for high-speed digital and high-frequency applications. He has been a Consultant for several corporations. His current interests include spectrum from microwave measurements to the generation of computer-aided design tools for electronic systems.

Dr. Schutt-Ainé was the recipient of several research awards including the National Science Foundation (NSF) Major Research Instrumentation Award in 1991, the National Aeronautics and Space Administration Faculty Award for Research in 1992, the NSF Mid-Career Advancement Award in 1996, and the UIUC-National Center for Superconducting Applications Faculty Fellow Award in 2000. He is currently serving as Editor-in-Chief of the IEEE TRANSACTIONS ON ADVANCED PACKAGING.

Dmitri Klokotov received the B.S. degree in physics from Saratov State University, Saratov, Russia, in 2001, and the M.S. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, in 2007. He is currently pursuing the Ph.D. degree.

His current research interests include numerical methods, computational electromagnetics, circuit simulation, interconnect analysis, and signal and power integrity.

Jilin Tan (S'95–M'96–SM'07) received the Diploma degree in theoretical physics from Beijing Normal University, Beijing, China, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from the University of Wisconsin-Madison, Madison, in 1991 and 1994, respectively.

He joined AnSoft Corporation, Pittsburgh, PA, in 1996, as a Research and Development Engineer after one-year post-doctoral study in Arizona State University, Tempe. After working with Intel Corporation, Hillsboro, OR, as a Senior Signal Integrity Engineer for one year, he joined Cadence Design Systems, Inc. Chelmsford, MA, as a Senior Member of the Consulting Staff in 2000, and became an Architect in 2005. He has focused on the advanced EM modeling and simulation of interconnects and devices, developing a 3-D full-wave electromagnetic solver and full-wave simulator in time domain for printed circuit board (PCB) and packaging signal integrity. He has been coordinating the Cadence-UIUC joint program since 2006. His current research interests include signal integrity analysis for high-speed digital PCB design and packaging design.

Dr. Tan is an Associate Editor of the IEEE TRANSACTIONS ON ADVANCED PACKAGING.

Ping Liu was born in China, in 1979. She received the B.S. and M.S. degrees in communications engineering from Beijing Jiao Tong University, Beijing, China, in 2000 and 2003, respectively, and the Ph.D. degree in electromagnetic fields and microwave engineering from Shanghai Jiao Tong University, Shanghai, China, in 2006.

She is now with Silicon Package Board Division, Cadence Design Systems Inc., Shanghai, working on the model extraction and circuit simulation tools research and development in high-speed circuits and systems. Her current research interests include field solver modeling of high-speed interconnects, large-scale circuit system simulation, and power and signal integrity analysis in high-speed circuits.

Wenliang Dai received the M.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2001, and the Ph.D. degree in electronic engineering from Shanghai Jiao Tong University, Shanghai, China, in 2004.

He was with the Silicon-Package-Board Research and Development Center, Cadence Design Systems Inc., San Jose, CA, from 2004 to 2011, as a Senior Member of the Consulting Staff. He is currently with Xpeedic Technology Inc., Issaquah, WA. He has also published more than 20 journal and conference papers as first author in the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEE PROCEEDINGS ON MICROWAVES, ANTENNAS AND PROPAGATION, the *Institute of Electronics Information and Communication Engineers Transactions on Electronics*, and the *International Journal of Electronics*. He had one issued and three pending U.S. patents for high-speed circuit analysis. His current research interests include computational electromagnetic fields, microwave and millimeter-wave circuitry design, parameter extraction for on-chip interconnects (complementary metal-oxide-semiconductor process), radio frequency (RF) components, design and measurement of RF-integrated circuits and high-speed integrated circuits, and signal/power integrity analysis for high-speed circuit systems in chip-package-board codesign flow.

Dr. Dai is a Reviewer for the IEEE TRANSCTIONS ON ANTENNAS AND PROPAGATION, the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the Institute of Engineering and Technology Proceeding, and the Design Automation Conference.

Feras Al-Hawari received the B.S. degree in electrical engineering from Jordan University of Science and Technology, Al Ramtha, Jordan, in 1993, the M.S. degree in computer engineering from Florida Institute of Technology, Melbourne, in 1995, and the Ph.D. degree in electrical engineering from Northeastern University, Boston, MA, in 2007.

He joined Cadence Design Systems Inc., Chelmsford, MA, in 1995. Currently, he is a Senior Member of the Consulting Staff as well as a Technical Lead for the circuit simulation and signal integrity analysis technologies in the Allegro Printed Circuit Board (PCB) SI Research and Development Group. Recently, he developed efficient and accurate methods to model and simulate S-parameter black boxes, multiconductor transmission lines, and I/O buffer information specification devices. He also architected the bus analysis flow that is used to design and verify source synchronous memory interfaces such as double data rate type three. He filed six patents in the past two years. His current research interests include signal integrity, PCB design, circuit simulation, modeling of I/O devices and interconnects, and multithreaded and distributed computing.