

On-chip Oscilloscope for Signal Integrity Characterization of Interconnects in 130nm CMOS Technology

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Abstract

In this work, the design of a prototype chip for signal integrity characterization in 130nm CMOS technology is discussed. Measurement results for several interconnect configurations are presented. The goal is to accurately capture and characterize the transmission line properties of deep-submicron interconnects in order to generate guidelines for multi-GHz clock rate designs.

I. Introduction

There is an increasing need for accurate and easily implementable measurements of both active devices and interconnects in modern deep-submicrometer CMOS technology [1]. As the minimum feature size continues to shrink, integrated circuit designs tend to grow in complexity, due to tighter integration and reduced voltage. Existing analytical formulations fail to capture the parasitic effects, therefore accurate measurements are needed in order to support new design tools and new technology generations. It has also been demonstrated that the traditional RC-circuit representation for on-chip interconnects is not accurate when switching speeds are in the multi-GHz range [2]. Existing off-chip measurement techniques are invasive, or require prohibitively costly or delicate platforms. To avoid those drawbacks, one possible approach is to place the measurement circuitry directly on chip, in close proximity to the structures being measured. This technique has been proven to work successfully for older technology nodes [3]. An extension to newer technology nodes is explored in this work.

II. Principle of Operation

The on-chip oscilloscope circuit operation is based on subsampling (Fig. 1) of a repeatable voltage phenomenon. As shown in Fig. 2, an external trigger 1) produces an on-chip generated switching phenomenon; 2) the voltage is sampled by a transmission gate switch after an externally controlled delay; 3) the sampled analog voltage is stored in an op-amp input capacitance, buffered, and exported off chip where it is digitized and stored; 4) steps 1-3 are repeated, varying the delay (and thus sample time); 5) the samples are assembled in post-processing, and time-domain signal is reconstructed. By carefully controlling the delay produced by the delay cell, this approach allows sampling at Nyquist rate. This is not possible in real time, since the circuits performing measurements are in the same technology as the circuits being measured, and therefore can not be made to switch at the rate faster than the technology maximum.

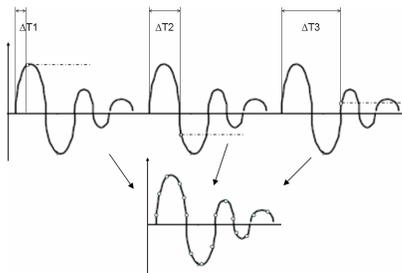


Figure 1. Subsampling and reassembly principle

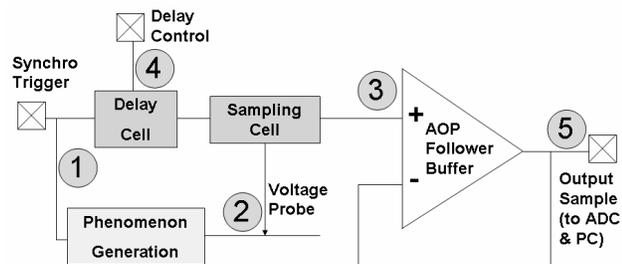


Figure 2. Basic block diagram of on-chip sampling circuit

III. Implementation Details

The circuit implementation follows the general pattern that was previously applied to older technology nodes [4], customized to the specifics of the available 130 nm process. In order to better utilize the limited range of control voltages, the linearity requirement of the delay cell is relaxed, resulting in non-uniform sampling points in time, which is accounted for in post-processing by time-domain interpolation. To avoid leakage of high-speed transistors which can corrupt the sampled signal during the hold phase, both

transmission gate transistors in the sampling head are placed in strong inversion mode, by making the rail-to-rail voltage of control inverters greater than the nominal 1.2V of the used UMC mixed-mode/RF process (overdriving both rails by 500mV). To avoid body effect, the chip substrate is also biased lower than the digital ground value. This has a beneficial effect on the sampling cell 3-dB bandwidth, increasing it from nominal value of 24.3 GHz to 70.9 GHz (as verified by simulation), several times higher than the Nyquist frequency for the projected time resolution of 5 ps. This also affects the digital switching logic controlling other blocks of the oscilloscope circuit, but since all the blocks are switching relative to the external trigger, the added delay does not affect the functionality of the complete system.

The layout of a single oscilloscope block, consisting of the 4-probe sensor and switching control system, is shown in Fig. 3. The probe sensor allows interleaved measurements of two neighboring lines at both near and far ends, and the switching control system allows independent excitation of each line in a pattern, driven by strong inverters (45ps rise time for the unburdened Victim and 55ps rise time for the Aggressor inverter, as predicted by simulations).

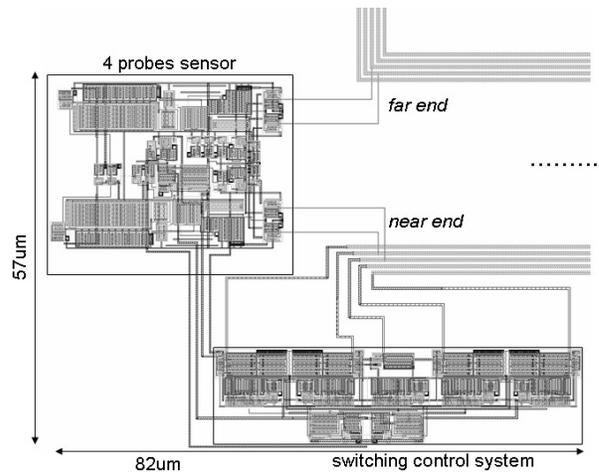


Figure 3. Layout of a single oscilloscope block.

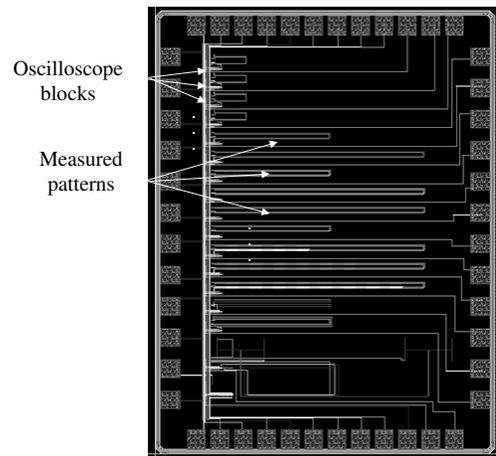


Figure 4. Layout of die showing measurement patterns

Measurement Patterns - Based on previous work in exploring signal integrity of interconnects, total of 20 patterns consisting of 5 coupled Metal3 lines each was selected. By varying the interconnect width (0.4 – 0.6 μm), spacing (0.4 – 3.6 μm) and length (0.3 – 3 mm), the complete characterization of the Metal3 process is possible, enabling exploration of propagation delay, crosstalk, and crosstalk-induced delay. In order to avoid the effect of long probe tips introducing unwanted parasitics, the near and far ends of each measurement pattern were implemented by folding the interconnects one or more times, depending on line length and available chip space. Also implemented were several experimental patterns, to allow for characterization of metal resistance, inductive effects of vias, propagation modes and process variations in clock distribution trees. Each pattern possesses its own oscilloscope, and independent time calibration and offset calibration circuits are placed on each die. Due to multiplexed outputs, up to 16 patterns can be placed on a single die (dimensions 1.45 mm x 1.9 mm). Two dice with different patterns were designed, as shown in Fig. 4 (for brevity, only one die layout is shown, with the difference being only in pattern layout).

Measurement Setup and Performance - Due to a large number of control signals needed to select various patterns, the chips were packaged in an LQFP 48-pin package. The subsampling rate of 1Ms/s makes it possible to use a low-cost package, FR-4 PCB (Fig. 5) and standard laboratory equipment for the test setup (Fig. 6). The use of a low supply voltage made it necessary to reduce of the analog control signals. Consequently, in order to eliminate the effects of noise on the sensitive delay cell, an average of 50 samples was taken for each delay value, resulting in a standard deviation of 2 mV between the samples in a Gaussian distribution.

Based on the measurement results, the system exhibits good repeatability (on the order of 5 mV), as well as adequate temporal resolution (down to 6.5 ps), with analog bandwidth greater than 20 GHz. Span of measured signals is from 1 ns (with maximum time resolution) up to 15 ns, for slow-changing phenomena.

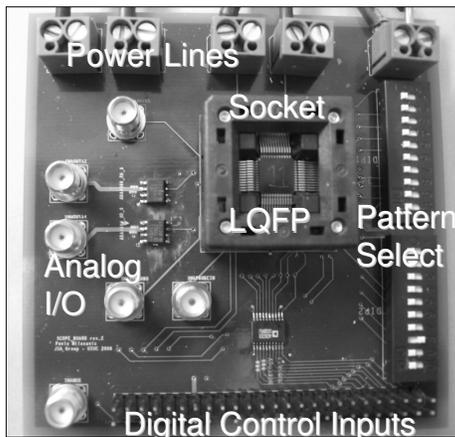


Figure 5. Test Printed Circuit Board

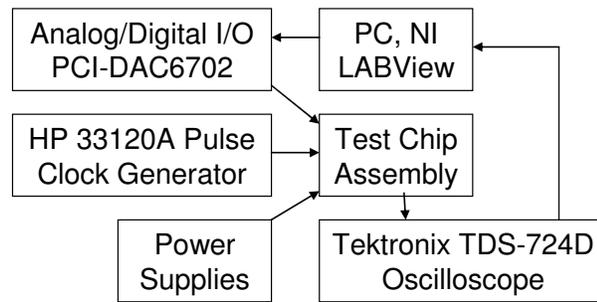


Figure 6. Test and Measurement Environment

IV. Measurements and Signal Integrity Characterization

After post-processing the measured samples and reconstructing the voltage waveforms, it is possible to observe both the timing and signal quality of the responses generated by the inverter drivers. From those measurements, various signal integrity parameters can be determined. In order to validate the functionality of the measurement circuit, several characteristic patterns were first chosen and measurement results were compared with the simulated models extracted by Cadence Assura. One such comparison is shown in Fig. 7, revealing good general agreement (with the simulated circuit switching about 20% faster, as expected).

Propagation Delay - For SI applications, it is important that the measured and simulated delays agree within the time resolution of the circuit. This is critical for accurate parameter extraction based on the propagation delay. Fig. 8 shows the relative propagation delays per unit length of lines in different metals, with lines in Metal1 having the largest RC constant, due to its highest capacitance per unit length (relative to the substrate).

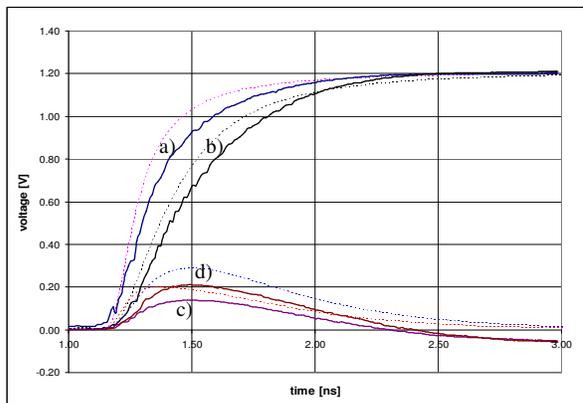


Figure 7. Measured (solid) and simulated (dashed lines) crosstalk induced on quiet victim line: a) near- and b) far-end of Aggressor2; c) near- and d) far-end Victim; width=spacing=0.4um, length=1mm

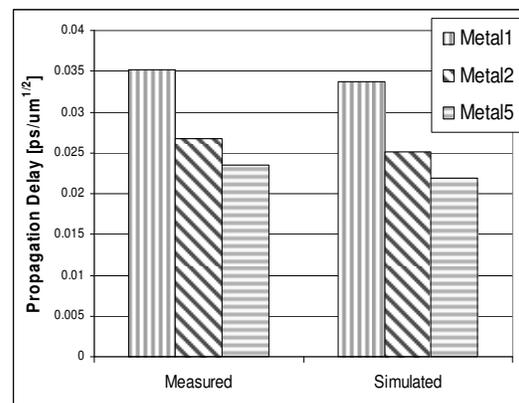


Figure 8. Simulated and measured propagation delays (normalized to unit RC) for three different metal layers

Fig. 9 shows the delay for several line lengths, measured for two different spacings. The measured data confirms quadratic RC delay dependence of line length, since resistance and capacitance both increase linearly with length. The increase in delay for reduced spacing is observed, which allows extraction of coupling capacitances between neighboring lines.

Crosstalk and Crosstalk-Induced Delay - Also of interest for modern IC designs with high interconnect density is to explore the effect of crosstalk induced on the quiet lines when neighboring lines are switching (Fig. 7). Measurements reveal that crosstalk induced on a pair of neighboring lines is almost doubled as spacing is reduced by 55%, as Fig. 10 demonstrates.

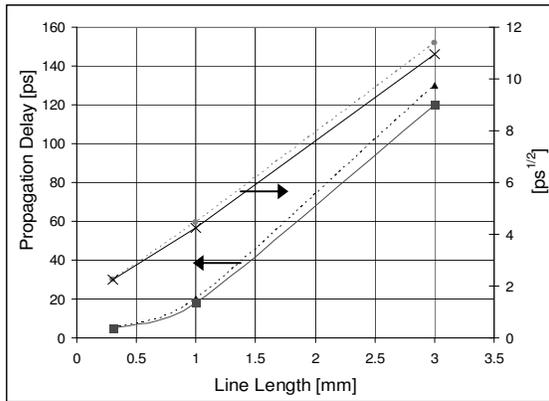


Figure 9. Measured propagation delay for different lengths of pairs of coupled Metal3 lines: a) width=0.4um, spacing=0.4um (solid) and b) width=0.4um, spacing=0.6um (dashed lines)

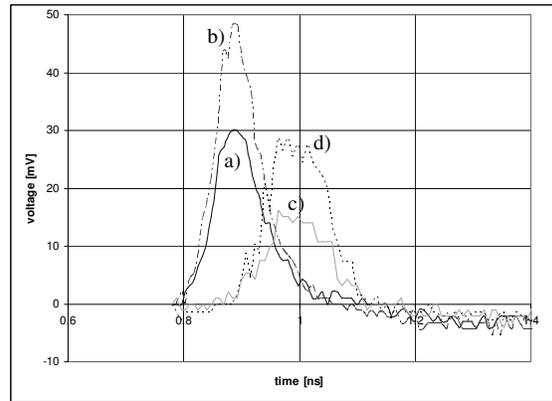


Figure 10. Crosstalk induced by switching Aggressor1 on quiet Aggressor2 line, width=0.4um, length=1mm; a) near- and b) far-end, spacing=1.6um; c) near- and d) far-end, spacing=3.6um

Crosstalk-induced delay is added to the switching delay of a driver, causing synchronization and latch errors. Fig. 11 shows the worst-case effect of strongly driven neighboring aggressor switching in the direction opposite of the observed victim line. By switching the aggressors at different times relative to the switching of the victim, the series of plots shown in Fig. 12 is obtained, revealing a constant induced delay of about 0.4ns (with fluctuations attributed to the effect of weak victim line switching on the aggressors).

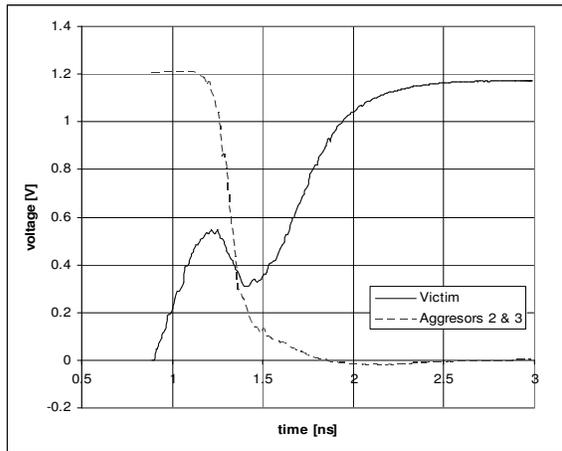


Figure 11. Measurement of victim and aggressor lines switching concurrently (width=spacing=0.4um, length=1mm, metal=M3)

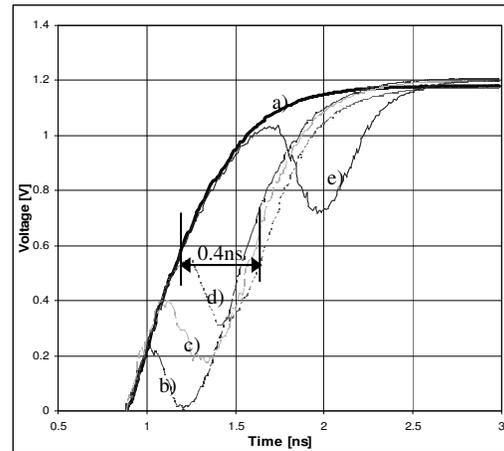


Figure 12. Measurement of crosstalk-induced delay: a) aggressors 2 & 3 quiet; b) simultaneous switching; and aggressors delayed by: c) 100ps, d) 200ps, and e) 700ps

V. Conclusion

This work demonstrated the design, implementation and testing of an on-chip oscilloscope using 130nm CMOS technology. The chip was used to characterize various types of deep-submicron interconnect structures. In particular, special attention was devoted to delay and crosstalk measurements. Future work will include a study of interconnect performance and ensuing signal integrity consequences in the presence of process variations.

References

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