Design of a 12Gb/s Transceiver for High-Density Links with Discontinuities using Modal Signaling

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***Abstract*—In high-speed chip-to-chip single-ended signaling links, far-end crosstalk presents one of the dominant noise sources, limiting the link performance. Diagonalizing the channel using modal decomposition has been proposed to mitigate the crosstalk, but so far only the transceiver designed for uniform low-loss homogenous media channels has been investigated. In this paper, the design of a transceiver system which takes advantage of modal decomposition over a typical memory bus with discontinuities is presented. The proposed approach is verified using circuit-based link simulation.**

Keywords- Crosstalk mitigation; modal decomposition; high-speed signaling.

I. INTRODUCTION

In order to achieve the increasing demands of chip-to-chip data throughput, off-chip signaling speeds and edge rates are being increased as well, and interconnects are routed at greater density. In particular, for interconnects in an inhomogeneous medium, such as microstrip parallel links on a low-cost PCB substrate, far-end crosstalk (FEXT) becomes the dominant noise source, resulting in both amplitude noise and crosstalk-induced jitter (CIJ), which limits the system performance.

A signaling scheme for coupled interconnects called *multimode signaling* was suggested by [1], which takes advantage of the multiconductor transmission line theory to encode the parallel signals onto fundamental transmission line modes. Due to the linear independence of modes, the signals are decoupled; such signaling is theoretically free of crosstalk, and therefore could allow the data transfer at the channel capacity. For the special case of uniform interconnects in homogenous media, a modal transceiver prototype has been reported [2], which significantly reduces crosstalk in inter-chip signaling. However, most practical interconnect channels consist of multiple cascaded uniform line segments with different cross-sections (i.e. package and PCB traces), as well as other discontinuities (i.e. vias and connectors). Modal decomposition of such channels with discontinuities has been theoretically explored and is expected to result in significant crosstalk reduction [3]. However, the circuits realizing such a signaling system would need to be examined in detail. In this paper, we present the design flow for a modal signaling system using a typical low-power CMOS process and analyze its performance and power metrics for a typical memory bus.

II. MODAL TRANSCEIVER SYSTEM ARCHITECTURE

A. Overview

Basic building blocks of a modal transceiver system are shown in Fig. 1: the encoder (mapping the data bits to be transmitted onto modal signals), the decoder (mapping the modal signals to the received data bits) and the termination network (to prevent reflections and mode conversion), in line with the blocks of the mathematical modal decomposition operations. There are different possible options for implementing the building blocks, depending on the channel over which the signaling is to take place, the process that is available to the designer, and speed, power and design complexity requirements.

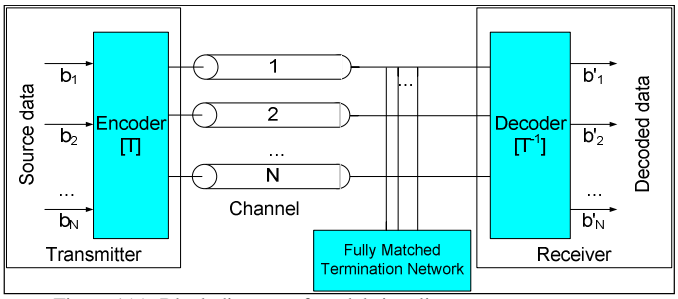

Figure 1(a). Block diagram of modal signaling system components

This paper will present the design flow suitable for short tightly coupled chip-to-chip interconnects, in particular the 4-line system as detailed in [3], consisting of 4-inch PCB traces on FR4 substrate, but also the package traces, vias and connectors. Each line has 0.5pF of equivalent capacitive loading, due to pad and receiver input capacitance. The technology node used is 1.2V IBM 90nm low-power digital CMOS, a typical process used for controller-memory links.

Some of the modal signaling blocks can be integrated with existing transceiver blocks for better efficiency. One such example is the modal encoder block, which for the case of binary NRZ signaling lends itself naturally to integration with the line drivers. In the following subsections, the details of the proposed modal signaling implementation will be given, referring to Fig. 2 for the proposed transmitter architecture blocks and Fig. 3 for the receiver blocks.

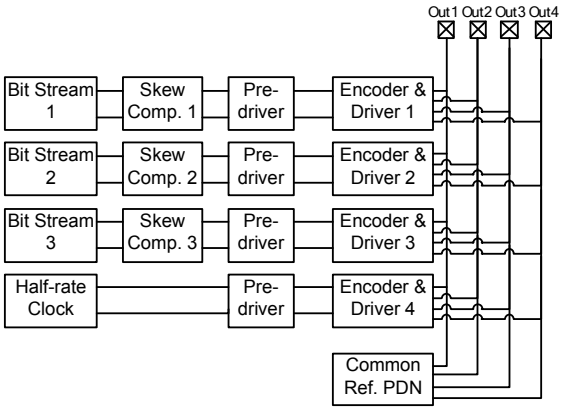

Figure 2. Proposed transmitter architecture for modal signaling

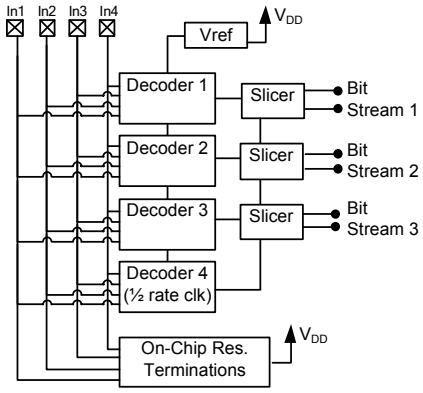

Figure 3. Proposed receiver architecture for modal signaling

B. Encoder/Driver Blocks

The generalized modal decomposition for nonuniform transmission lines, as presented in [4], was applied to the channel to obtain the encoder coefficients. As shown in previous work exploring modal decomposition of buses with discontinuities [3], it is preferred to use voltage waves for modal signaling, as opposed to current waves, due to the frequency-dependent behavior of current eigenvectors. For each combination of binary data signals at the input of the encoder, a particular linear combination of modal voltages needs to be excited at the near ends of the transmission line bundle. Based on the peak power limit for the low-voltage power supply used, the maximum swing at the output of each transmitter block was set to $250mV_{pp}$, by appropriately scaling the modal voltage excursions given in [3].

For high-speed data transmission, the preferred output stage configuration for single-ended signaling is a push-pull topology [5]. However, if such an output stage is treated as a voltage source, in advanced low-power CMOS processes its output resistance of push-pull transistors will be comparable to the characteristic impedance of the line [6], thus preventing accurate generation of linear combinations of voltages.

Rather than attempting to reduce the output impedance by placing the buffers in parallel [6], a converse approach of using current sources with high output impedance is proposed. To achieve the target $250mV_{pp}$ swing, an appropriate set of currents that need to be injected into the line bundle was calculated and is presented in Table I. A NMOS-only realization is preferred for better high-speed performance (due to higher carrier mobility), so the common mode at each line was set to V_{cm}=1V using open drain drivers realized as four self-cascode structures, shown in Fig. 4(a), with the gate bias set to V_{bias1}=0.9V, to ensure operation in saturation at all times. Self-cascode with m=4 is chosen for its large effective channel length and low effective output conductance [7].

TABLE I. Current changes to generate modal signals and the reference voltage level; positive sign denotes more current should be sourced from line

	ΔI [mA]				
Line	Mode 1	Mode 2	Mode 3	Mode 4	Common
1	1.0650	1.1950	-0.7970	0.5270	0.6740
2	0.4670	-1.0000	1.6773	0.6060	0.0252
3	-0.4670	-1.0000	-1.6773	0.6060	0.0252
4	-1.0650	1.1950	0.7970	0.5270	0.6740

Examining the changes in currents required to create modal voltages, we can notice from Table I that, due to channel symmetry, lines 1 and 4 in mode 1 can share the same current sources, as well as lines 2 and 3, and similarly for mode 3. A current-steering differential pair structure shown in Fig. 4(b) is therefore used to fully steer the constant current between lines, based on the bit value dictated by the pre-drivers. For modes 2 and 4, not all the currents can be shared; additional currents need to be injected (e.g. in case of mode 2, outer lines should receive 0.195mA more). For this purpose, a structure shown in Fig. 4(c) is used, also in a differential pair configuration to ensure linearity during transitions. Compared to the implementation presented in [2], only the currents steered into dummy resistors R and the common-level currents are not used in actual information signal generation, thus resulting in a much increased power efficiency.

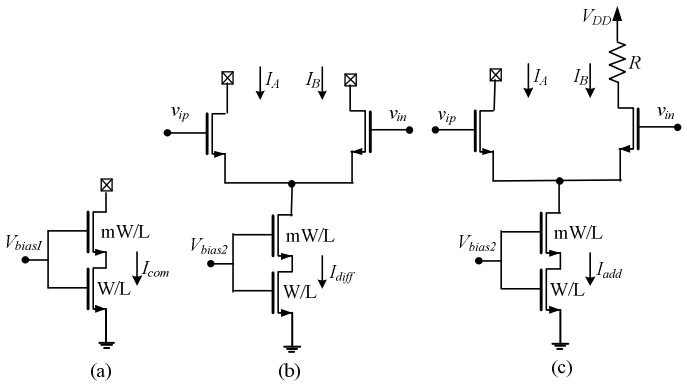

Figure 4. (a) Open-drain drivers producing the common-voltage levels; (b) Current-steering for shared currents, and (c) for non-shared currents

Each current source is realized as a set of pre-programmable binary-sized NMOS transistors (with those turned on receiving a constant bias of V_{bias2}=0.6V to ensure self-cascode saturation), so that the encoder coefficients can be adapted to the particular channel. The total average power of encoder/driver blocks is about 11mW. This does not include the pre-drivers, realized in a simple differential pair structure producing a swing of $300mV_{pp}$ at each drain node.

C. Line Termination Block

An important requirement for modal signaling is to provide an appropriate termination for modal waves, in order to eliminate reflections and modal conversion (which directly translates to crosstalk). For a realistic memory bus system, due to the presence of discontinuities and loss, the matching terminations will be frequency dependent; all the ideal termination elements will be complex (due to finite conductivity and dielectric loss); finally, the termination network will be a full matrix; all of which could present practical challenges in circuit realization.

One possible solution is the implementation of a low-order frequency dependent matching network [8]. However, this requires utilizing a number of precision capacitors and inductors, which might prove impractical to implement on chip; pushing these passive elements out into package would increase the system cost and design complexity. A compromise solution explored in this work is to implement a full grid of on-chip resistors between each line pair, and to utilize mode 4 (the "ground mode", most dependent on a frequency dependent matching network) to transmit a clock signal with a reduced data rate (source-synchronous signaling). The resistors are terminated to V_{DD} to provide the pull-up termination network to the open drain transmitter drivers, and their values are given in [3].

D. Modal Skew Compensation Block

After decoding the signals transmitted over fundamental modes, there will be additional modal skew introduced, based on the propagation velocities of the modes onto which the signals were encoded. Deskew circuitry on the transmitter side can delay the generation of modal signals, so that they all arrive at the far end of the line bundle synchronized with each other. This pre-delay is realized using simple double-inverter delay elements [9].

As discussed in previous sub-sections, in order to minimize the impact of the limited bandwidth of mode 4, a half-rate (2Gb/s) source-synchronous clock is transmitted over this mode, and full-rate (4Gb/s) data is transferred over other three modes and sampled on both edges of the clock. For a realistic chip-to-chip communication system consisting of many bundles, some type of master clock realignment circuitry might still be needed [9], such as a simple delay locked loop (DLL) to realign the signals to a particular global reference.

E. Decoder Block

Once the line voltages have been sensed, they need to be decoded back from the modal space to the line space, in order for the SISO receiver blocks to decide which binary symbol was transmitted. The decoder block is most naturally realized by converting the received voltages to current, and then creating the desired linear combinations by simple KCL summation. A current subtractor similar to the one presented in [10], which allows simultaneous voltage-to-current conversion and reference level removal is shown in Fig. 5. The cell operation is based on its large-signal behavior in response to a differential input signal, as given by [11]:

$$I_O = I_1 - I_2 = \frac{1}{2} k_n' \frac{W}{L} (V_1 - V_2) \sqrt{\frac{4I_{SS}}{k_n' \frac{W}{L}} - (V_1 - V_2)^2} \approx \sqrt{k_n' \frac{W}{L} I_{SS}} (V_1 - V_2) \quad (1)$$

The linear approximation in (1) is valid for suitably chosen transistor sizes and bias current (which ensures complete switching does not take place); they are also used to set the decoding coefficient. This versatile block can produce either the positive (when $V_1=V_{far}$, $V_2=V_{cm}$) or negative current (with the opposite wiring) proportional to received signal on the far-end of a line, or the direct difference of two line signals (when $V_1=V_{farA}$, $V_2=V_{farB}$). The currents are then summed over a suitably sized resistor to produce the slicer input voltage.

Again, each current source is realized as a set of pre-programmable binary-sized NMOS transistors, so that the decoder coefficients can be adapted to the particular channel. The target coefficients should take into account both the channel properties (through eigenvalue decomposition) and the noise present in the system, since simply inverting the channel might enhance noise at particular frequencies. A well-known technique from MIMO communication theory which approximates the optimal solution is to use a LMMSE criterion for the decoder matrix coefficients [12].

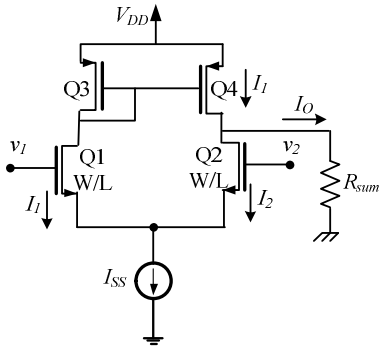

Figure 5. Current subtractor for modal decoder realization

F. Receiver Block

Assuming that the system under consideration is crosstalk-dominated, the SISO receiver blocks have a simple task of deciding on the signals sent by comparing the received signals with the generated reference voltage; this can be performed by using a standard differential pair configuration operating as a slicer. If the channel had a significant level of intersymbol interference (ISI) present, receiver-side equalization [13] could be used on a per-channel basis.

III. Simulation Results

To demonstrate the crosstalk mitigation performance of the system, Fig. 6 shows the simulated 4Gb/s NRZ pulse responses of signals transmitted over the equivalent modal channels. As expected, each modal signal creates a greatly reduced crosstalk disturbance on the other modes, mainly due to circuit linearity limitations. Also notable is the low amount

of ISI present, due to the full matching matrix for this short channel, but the internal reflections which can not be removed this way are still visible[1], mainly in mode 4.

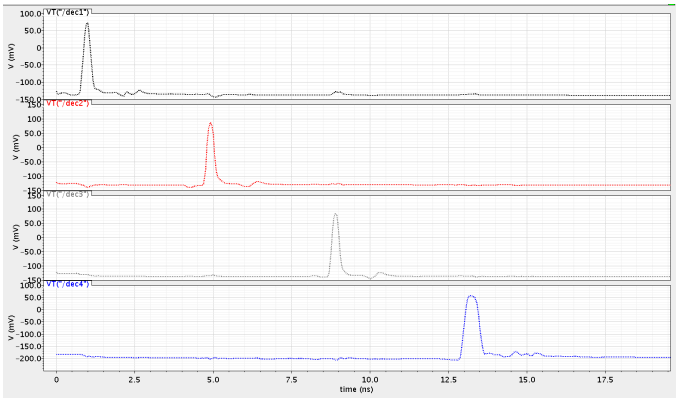

Figure 6. Unit pulse responses of signals over equivalent modal channels

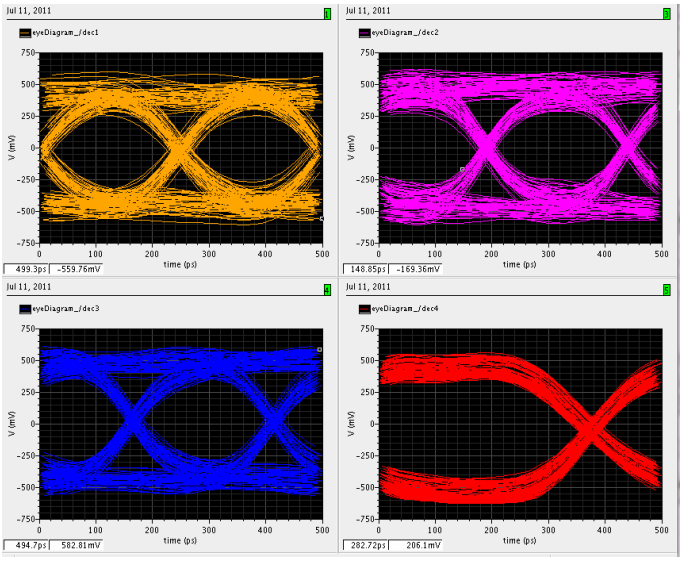

Figure 7. Eye diagrams of decoded modal signals (normalized to $1V_{pp}$)

To verify the overall system performance, the eye diagrams of decoded modal signals using 2^8-1 PRBS sequences are shown in Fig. 7. The modal skew compensation block was not activated, to demonstrate arrival times of source-synchronous clock in relation to the three data lines. Maximum peak-to-peak jitter present in the system is $J_{p,p}$=39ps (mainly due to ISI), which is only 47% of the target jitter value allocated for interconnects (in this case UI/3=83ps). The eye opening of 150mV should present a sufficient voltage margin for the slicer to operate on for reliable detection (BER<10^{-12}), with assumed noise σ=2mV_{rms} and offset and sensitivity of 10mV total. However, this analysis would for completeness need to include Tx jitter and power supply fluctuations as well.

[1] Note that S-parameters cannot be used for complete system characterization, due to the integrated encoder/driver structure. A large-signal description such as X-parameters [14] needs to be used instead.

IV. Conclusion

In this paper, the design of a multimode signaling transceiver for a chip-to-chip channel with discontinuities has been investigated. Starting from the generalized modal decomposition of nonuniform lines, suitable encoder, decoder, skew compensation and termination structures were proposed. Circuit-level simulations confirm the robust performance of the system in mitigating far-end crosstalk. The total bit rate of the transceiver is 3x4=12Gb/s, along with the source-synchronous transmitted half-rate clock.

The tunability of encoder and decoder coefficients produces quantization noise. Another noise source is the imperfect matching of differential pairs and resistor mismatches due to process variations. Also, single-ended signaling is prone to the simultaneous switching output (SSO) noise, which injects variations into reference voltages. The impact of noise should be studied in more detail, during layout and manufacturing of the test transceiver system.

Acknowledgment

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