ON-CHIP VOLTAGE CONTROLLED OSCILLATOR FOR CLOCK DATA RECOVERY SYSTEMS

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THESIS

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ABSTRACT

As the clock rate of microprocessors keep increasing, high data rate IO should be designed to realize their maximum benefit. However designing robust, low power high speed IO links is very chanllenging due to the increased transmission line loss, crosstalk, and signal distortion resulting in intersymbol interference. Synchronous sampling is often employed to overcome these challenges. However synchronous sampling makes use of a high purity oscillator to minimize the clock jitter. This thesis focuses on the design of a high purity, low power voltage controlled oscillator to be used as part of clock data recovery system in 25 Gb/s serial IO link.

To my parents.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

1.1 Background

Oscillators are an integral part of many electronic systems. They represent an essential building block in most modern communication systems. Communication transceivers rely heavily on frequency translation which is made possible by the use of local oscillators. Oscillators are also employed to generate clock signals required by modern microprocessors and synthesize carrier signals used in cellular telephones. However the design of high purity, robust oscillators in deep sub-micron CMOS technology continues to pose numerous challenges.

An oscillator is an electrical circuit that generates a periodic signal like a sine wave or square wave. A voltage controlled oscillator is a specialized oscillator whose frequency of oscillation can be tuned based on an external signal. Oscillators in general are divided into two categories depending on the signal they produce. Harmonic oscillators generate sinusoidal signals and are referred to as 'linear' oscillators while relaxation oscillators produce non sinusoidal signals such as square wave.

Both harmonic and relaxation oscillators are commonly characterized based on their amplitude instability, frequency instability, power consumption and area requirement. These performance metrics are not always independent of one another and a trade-off generally exists between them [1] as shown in Figure 1.1. Amplitude instability represents the fluctuation in the amplitude of oscillation as compared to

the expected amplitude. Similarly frequency instability represents the fluctuation in the frequency of oscillation as compared to the expected frequency.

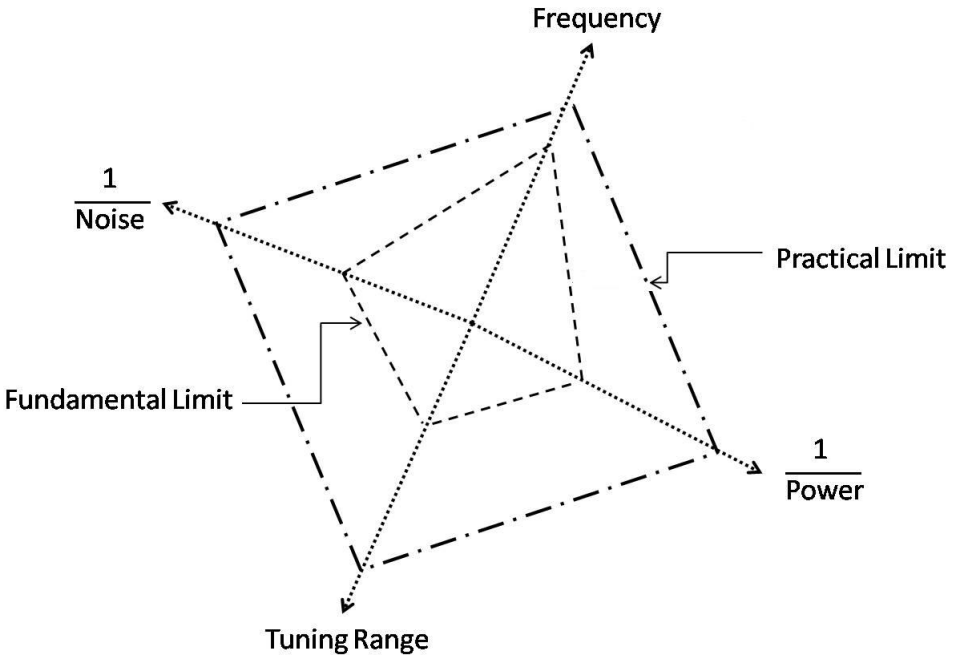

Figure 1.1: Trade-offs between the performance metrics of an oscillator.

1.2 Motivation

In the past decade there has been tremendous growth in integrated circuits (ICs) due to their ability to realize high performance, low power mixed signal systems at low cost. Among various technologies complementary metal-oxide-semiconductor (CMOS) technology has led the growth in microprocessor computing capability [2]. The rapid increase in computational capability has given rise to the need for high data rate communication between ICs. However higher data rates consume more power limiting the number of high speed links that can be integrated into a single IC. Hence high speed links that consume less power while operating at high data rates is critical in utilizing the increased computational capabilities of the microprocessor.

This thesis is part of an ongoing high-speed link design project at University of Illinois, Urbana-Champaign which aims to implement a 25 Gb/s serial IO link while minimizing power consumption using advanced adaptation algorithms, reconfigurable circuit blocks and system-aware design techniques.

A high-speed serial link is made up of a transmitter, channel and a receiver as shown in Figure 1.2. The transmitter transmits the data stream over the channel to the receiver. The receiver then processes the received signal to reliably recover the original data stream. However the original data stream cannot be perfectly reconstructed by the receiver as the channel distorts the transmitted signal by adding noise and introducing intersymbol interference (ISI) [3]. Intersymbol interference refers to the distortion caused by symbols (pulses) overlapping with one another.

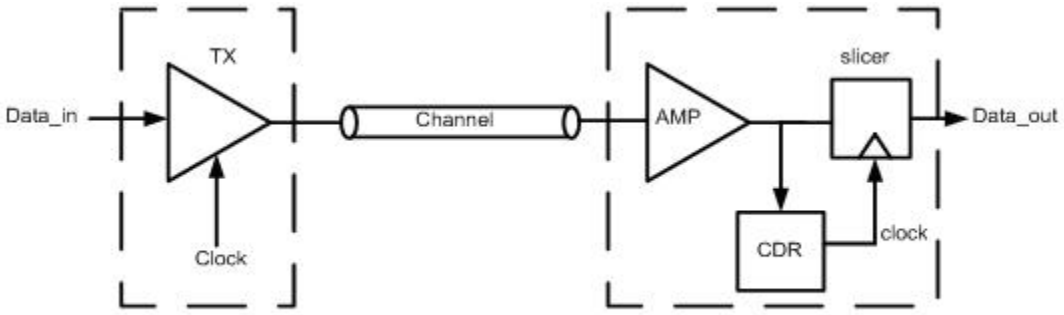

Figure 1.2: Simplified diagram of a typical high speed link.

Intersymbol interference is caused due to the bandwidth limitations of the channel while the noise present in the received signal results from the additive Gaussian noise of the channel. A typical channel has a frequency response as shown in Figure 1.3. Such a channel acts as a filter by effectively removing the high frequency components of the transmitted signal. This leads to spreading of energy in one symbol into adjacent symbols making the communication less reliable.

Synchronous sampling can be employed to overcome the distortion caused by the channel and reliably recover the transmitted data. It minimizes the probability of

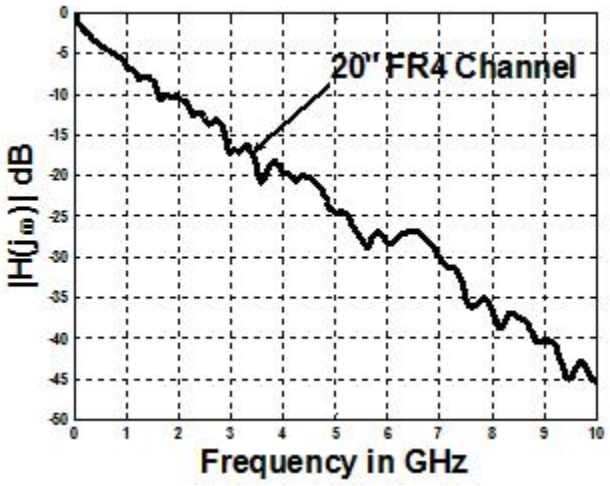

Figure 1.3: Frequency respose of a 20" FR-4 channel. Data provided by Intel Corporation.

making an error by sensing the peak value of received pulses. Synchronous sampling requires a clock signal with high spectral purity whose frequency matches the data rate of the serial link. A clock data recovery unit (CDR) typically accomplishes the above two tasks in a high speed transceiver. This thesis presents the design of a 25 GHz voltage controlled oscillator (VCO) in 65-nm technology to be used as part of the clock data recovery unit.

1.3 Scope

Designing low power on-chip voltage controlled oscillator with high spectral purity has been a highly researched topic in recent years [4–6]. While several different architectures that achieve the above objectives have been suggested [3–6], this thesis focuses primarily on the well known tail current biased cross-coupled differential LC oscillator.

1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 gives a brief introduction to oscillator fundamentals. It reviews the small-signal linear analysis technique used to design oscillators. It also discusses the different ways of quantifying the frequency instability of an oscillator. Chapter 3 provides an in-depth analysis of a cross-coupled differential LC oscillator. It also describes the different sources of noise contributing to the frequency instability of the oscillator. Chapter 4 presents the design of the cross-coupled differential LC oscillator in 65-nm, low power IBM process. It also includes a discussion on the simulated performance of the oscillator. Chapter 5 provides a summary of the thesis.

CHAPTER 2

OSCILLATOR FUNDAMENTALS

2.1 Overview

This chapter provides a brief overview of basic oscillator fundamentals starting with a mathematical model of an harmonic oscillator. Section 2.3 discusses the linear analysis techniques used to determine the conditions of oscillation while section 2.4 provides a review of resonators. Section 2.5 discusses the effect of circuit nonlinearity on steady state operation. The last section provides an introduction to frequency instability including a review of the most commonly used methods of quantifying frequency instability like phase noise and jitter.

2.2 Mathematical Model

An ideal harmonic oscillator generates a sinusoidal signal usually in the form of voltage. The output of such an oscillator can be expressed as $V_0 cos\left[\omega_0 t + \phi_0\right]$ where V_0 represents the amplitude of oscillation, ω_0 represents the frequency of oscillation and ϕ_0 represents the initial phase of oscillation. In an ideal oscillator the quantities V_0, ω_0 and ϕ_0 are all constants. Since the output signal contains a single frequency ω_0, all the energy in the signal is contained in an infinitely small bandwidth centered at ω_0. Thus the one-sided frequency spectrum of an ideal harmonic oscillator consists of a single impulse located at the frequency of oscillation ω_0 as shown in Figure 2.1.

Figure 2.1: One-sided frequency spectrum of an ideal harmonic oscillator.

A practical oscillator however generates an output signal that can be expressed as $V_0\left[\left(1+A\left(t\right)\right)\right]cos\left[\omega_0 t+\phi\left(t\right)\right]$ where $A\left(t\right)$ and $\phi\left(t\right)$ represent random fluctuation in amplitude and phase while V_0 represents the ideal amplitude of oscillation and ω_0 represents the ideal frequency of oscillation. Random fluctuations in amplitude and phase result in sidebands centered around the frequency of oscillation in the signal spectrum as shown in Figure 2.2. The sidebands imply that the energy in the signal is distributed over a finite bandwidth cenetred around ω_0. The above description does not take into account the presence of harmonics in the output signal to keep the analysis simple.

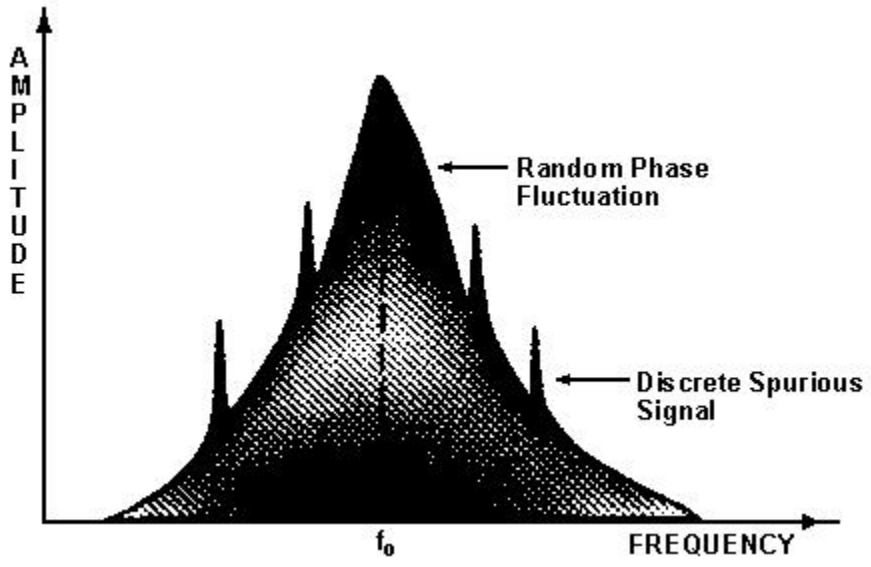

Figure 2.2: One-sided frequency spectrum of a real oscillator.

2.3 Linear Analysis Techniques

Oscillators are primarily nonlinear circuits. However small-signal linear analysis is often employed to analyze oscillators since they behave as linear systems with small signals at start-up. Hence linear analysis cannot predict the behavior of oscillators at steady-state though it can yield the conditions required for oscillation along with an estimate of the frequency of oscillation.

Linear analysis of oscillators is simplified greatly by thinking of oscillators as unstable feedback systems. An unstable feedback system experiences constructive or positive feedback which causes its output to grow indefinitely for a small initial excitation or disturbance. A block diagram of a typical feedback system is shown in Figure 2.3.

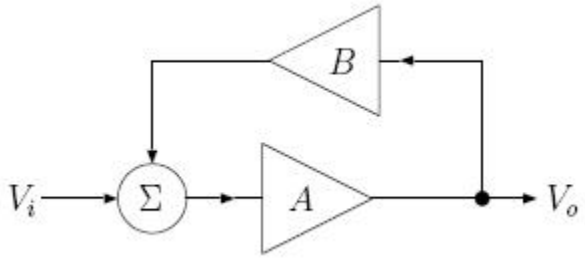

Figure 2.3: Block digram of a typical feedback system.

The voltage transfer function between the output and input of this system is given by

$$\frac{V_0(j\omega)}{V_i(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)B(j\omega)} \tag{2.1}$$

where $A(j\omega)$ represents the gain through the feed-forward path and $B(j\omega)$ represents the gain through the feedback path. The quantity $A(j\omega)B(j\omega)$ plays an important role in determining whether the oscillator oscillates and is often reffered to as the loop gain of the system. Loop gain of more complicated systems can be determined by breaking open the feedback loop and calculating the gain from the

input to the point where the feedback loop was broken. If the feedback loop of the system described above is broken at the summing junction then the loop gain is given by $V_f(j\omega)/V_i(j\omega)$ as shown in Figure 2.4.

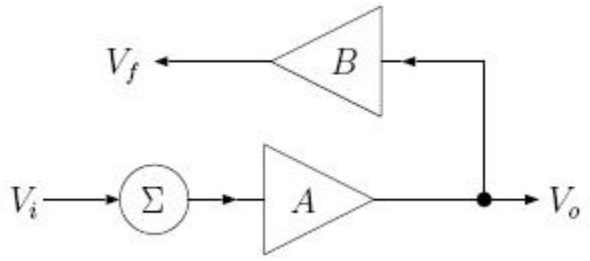

Figure 2.4: Calculating loop gain by breaking the feedback loop.

The voltage transfer function of the feedback system shown in Figure 2.3 is singular (infinite) at frequencies ω_0 where the loop gain is equal to one. Thus a sinusoidal excitation at this frequency traverses around the loop and appears back at the input with no change in phase or amplitude. However if the magnitude of loop gain is greater than one then the circuit amplifies its own noise through each pass of the loop allowing the component at ω_0 to grow with time. The loop gain in most high frequency oscillators is equal to or greater than one at exactly one frequency. Hence only one frequency component can traverse around the loop without experiencing any change in phase resulting in steady state oscillation. The two conditions required for steady state operation are called the "Barkhausen Criterion" and can be written as follows

$$mag\left[A\left(j\omega\right)B\left(j\omega\right)\right]=1 \tag{2.2}$$

$$arg\left[A\left(j\omega\right)B\left(j\omega\right)\right]=0 \tag{2.3}$$

Equation 2.2 is used to obtain as estimate of the frequency of oscillation while Equation 2.3 is used to determine the amount of gain required for oscillation to start and reach steady-state.

Negative resistance is an alternative method of analyzing oscillators where the calculation of loop gain is not feasible. The Kirchoff's current equation for the circuit shown in Figure 2.5 is given by $I\left(Z_A + Z_B\right) = 0$. Finite current I is allowed in the system if $Z_A + Z_B = 0$. Writing the impedances in terms of resistances and reactance result in the following conditions for finite current I to exist

$$\begin{aligned} Z_A + Z_B = 0 \Rightarrow (R_A + jX_A) + (R_B + jX_B) = 0 \\ \Rightarrow R_A + R_B = 0 \\ \Rightarrow X_A + X_B = 0 \end{aligned} \tag{2.4}$$

Equation 2.4 implies that the reactances and resistances of Z_A and Z_B must cancel out one another. In order for the resistances to sum to zero either Z_A or Z_B must exhibit negative resistance while reactances that sum to zero are said to satisfy the resonance condition.

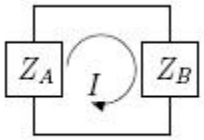

Figure 2.5: General circuit consisting of impedances $Z_A$and Z_B.

Analysis of oscillators using the negative resistance approach begins by dividing the circuit into two parts that are associated with impedances Z_A and Z_B. One part consists of all active devices while the other part consists of only passive devices. Note that the part with only passive devices has a positive resistance. The frequency of oscillation can be determined by using the resonance condition while steady-state oscillation can be guaranteed by ensuring that the part with the active devices has a large enough negative resistance.

2.4 Resonator Fundamentals

Integrated inductors and varactors available in CMOS technologies have made it possible to design oscillators based on passive resonant circuits. Figure 2.6 shows a simple parallel RLC circuit driven by an ideal current source. The transfer function between the output voltage and input current is given by

$$\frac{V_{out}(j\omega)}{I_{in}(j\omega)} = \frac{R_P}{1 + jQ_P\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)} \tag{2.5}$$

where

$$\begin{aligned} \omega_0 &= \tfrac{1}{\sqrt{LC}} \\ Q_P &= \tfrac{R_P}{\omega_0 L} = R_P\sqrt{\tfrac{C}{L}} \end{aligned} \tag{2.6}$$

ω_0 defined in Equation 2.6 represents the resonant frequency of the circuit while Q_P defined in Equation 2.6 represents its quality factor. The transfer function shown in Equation 2.5 is defined in terms of Q_P because the quality factor describes the frequency selectivity of resonant RLC circuits [7].

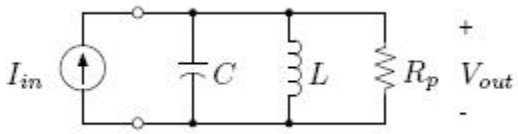

Figure 2.6: Parallel RLC resonant circuit.

Quality factor (Q) has a more general definition that can be applied to both resonant and non resonant circuits as shown below

$$\begin{aligned} Q &= 2\pi\frac{Maximum\ instantaneous\ stored\ energy}{Energy\ dissipated\ per\ cycle} \\ &= 2\pi f\frac{Maximum\ instantaneous\ stored\ energy}{Time\ average\ power\ dissipated} \end{aligned} \tag{2.7}$$

The general definition of Q described above is very useful in characterizing lossy inductors and capacitors. Modeling lossy components as a parallel combination of a reactance and resistance at some frequency further simplifies the definition of Q as shown in Figure 2.7.

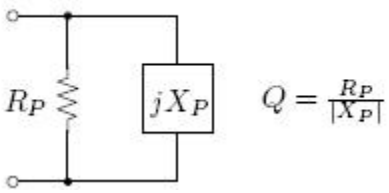

Figure 2.7: Q for a parallel combination of resistance (R_P) and reactance (X_P).

Figure 2.8 shows a typical plot of the quality factor as function of frequency for a 300 pH on-chip spiral inductor in 65-nm CMOS process. Optimal performance can be achieved by operating the inductor at or near the peak of the Q vs. frequency curve.

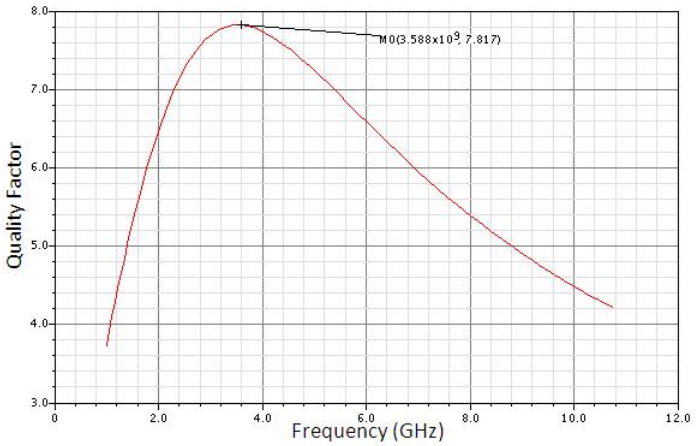

Figure 2.8: Typical variation in inductor Q with frequency.

2.5 Nonlinear Effects on Steady-State Operation

Linear analysis implies that the output of an oscillator grows indefinitely if the small-signal loop gain is greater than one. In order to reach steady-state however the amplitude of oscillation must be finite and remain constant. Hence some amplitude limiting mechanism is required to reduce the loop gain to one as the amplitude begins to grow as shown in Figure 2.9.

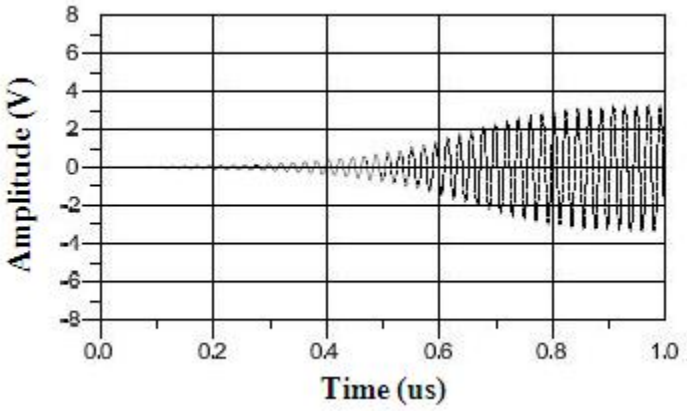

Figure 2.9: Behavior of a self limiting oscillator at start-up.

Amplitude limiting mechanisms are primarily nonlinear. In a self limiting oscillator for instance, the amplitude of oscillation keeps growing until the active devices begin to saturate. This reduces the gain of the devices which effectively reduces the loop gain of the oscillator to its steady-state value. Besides limiting the amplitude of oscillation these mechanisms also distort the output signal resulting in non sinusoidal waveform. Hence the linear analysis techniques described in section 2.3 cannot be used to analyze the steady-state behavior of oscillators.

2.6 Frequency Instability Fundamentals

Frequency stability describes the extent to which an oscillator generates the same frequency signal throughout a specified period of time. All real oscillators experience some amount of frequency instability due to the inherent noise present in them. Frequency instability can be divided into two components - long term instability and short term instability.

Long term instability refers to the variation in frequency that takes place over extended period of time like a day, month or a year. It is generally measured in a parts per million (ppm) and is mainly caused due to aging. Short term instability on the other hand refers to frequency fluctuation about a mean value that lasts less than a few seconds. Short term instability degrades the performance of the oscillator and hence the system as compared to long term instability which can be improved by utilizing high quality devices.

The mathematical model of a practical oscillator ($V_0 \left[(1 + A\left(t\right)\right] Cos \left[\omega_0 t + \phi\left(t\right)\right]$) was described in section 2.2 and is repeated here for convenience. The variation in amplitude $A\left(t\right)$ can be easily removed by the passing the output signal through a hard limiter. The variation in phase however cannot be eliminated and results in sidebands as described in section 2.2. The variations in phase can also be divided into two types - deterministic and random. The deterministic component of phase fluctuation appears as discrete signals in the frequency spectrum plot as shown in Figure 2.2. These discrete signals are called spurs and can be related to known phenomenon like power line frequency or mixer products. The random component of phase fluctuation is widely known as phase noise. The sources of phase noise in an oscillator include thermal noise, shot noise and flicker noise. Phase noise plays a critcal role in clock data recovery systems because it affects the system bit error rate.

There are many ways of quantifying phase noise. All of these methods measure the frequency or phase fluctuation of the oscillator in either time or frequency domain. Single sideband noise spectral density ($L(\triangle f)$) is the most commonly used method of describing phase noise in the frequency domain. $L(\triangle f)$ is defined as the ratio of power contained in one phase modulated sideband to the total signal power at a frequency offset $\triangle f$ away from the expected frequency of oscillation (carrier frequency, f_0) on a per hertz basis as shown in Figure 2.10.

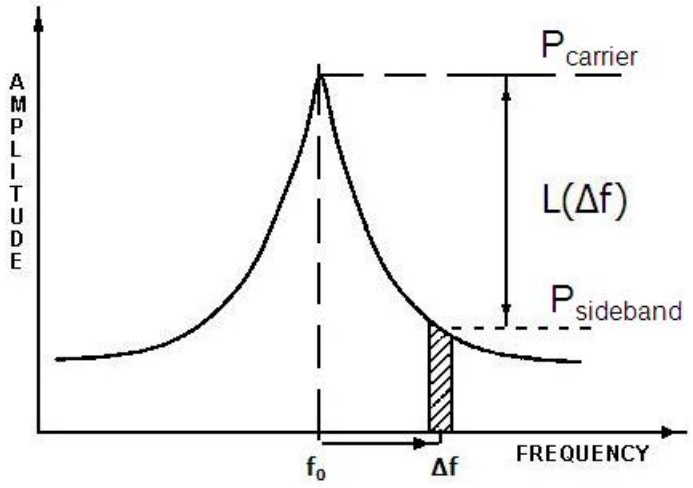

Figure 2.10: Single sideband phase noise, $L(\triangle f)$.

$L(\triangle f)$ can be directly calculated fom the frequency spectrum of the signal as shown in Figure 2.10. It has the units of decibels below the carrier per hertz (dBc/Hz) and is mathematically defined as

$$L(\triangle f) = 10Log\left[\frac{P_{sideband}(f_0 + \triangle f)}{P_{carrier}}\right] \tag{2.8}$$

Timing jitter is another commonly used technique of quantifying phase noise in the time domain. Jitter is generally defined as the short term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time as shown in Figure 2.11.

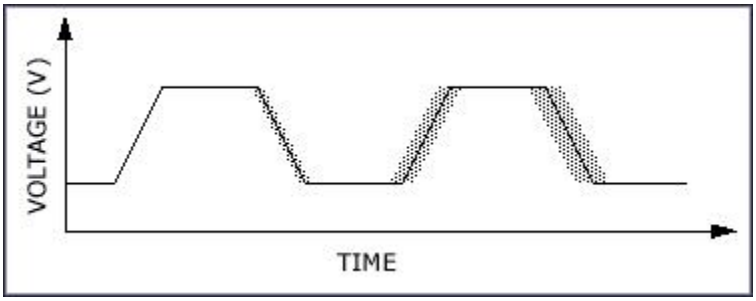

Figure 2.11: Timing jitter in a clock signal.

Timing jitter is also composed of two components, one that is deterministic and one that is random. Random jitter is the result of phase noise while deterministic jitter is caused due to known phenomenon like power line frequency or mixer products. In some applications like synchronous optical networking (SONET), jitter is specified at a particular frequency band $\triangle B$. In such cases the root mean square (rms) jitter can be directly calculated from the single sideband phase noise as follows

$$Jitter_{RMS} = \frac{1}{2\pi f_0}\sqrt{2\int_{\triangle B} 10^{\frac{L(f)}{10}} df} \tag{2.9}$$

where f_0 is the expected frequency of oscillation and $\triangle B$ is the bandwidth of interest [8].

CHAPTER 3

DIFFERENTIAL LC OSCILLATOR THEORY

3.1 Overview

One of the most commonly used on-chip voltage controlled oscillators is the cross-coupled differential LC oscillator [9,10]. Figure 3.1 shows a cross-coupled differential LC oscillator biased using a tail current source.

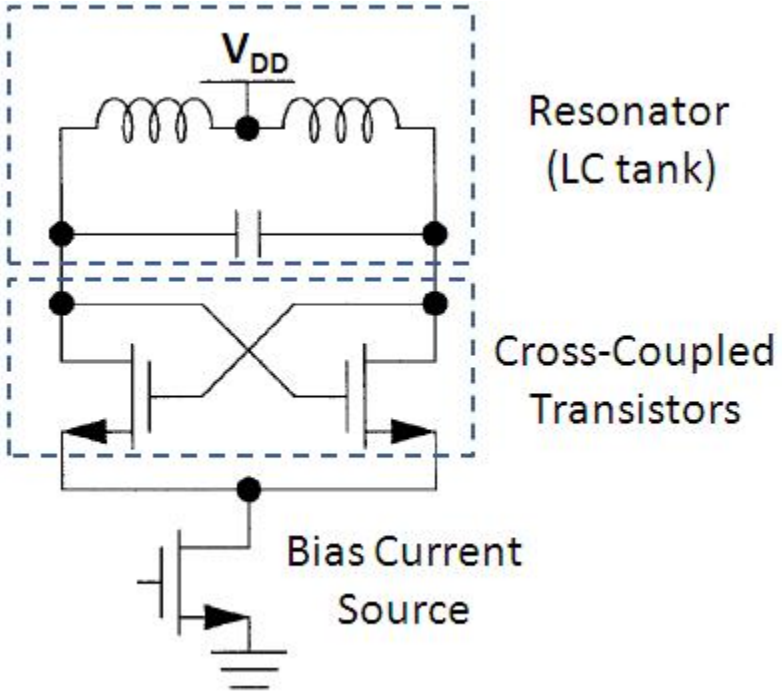

Figure 3.1: Tail current biased cross-coupled differential LC oscillator.

The resonator (LC tank) sets the frequency of oscillation while the cross-coupled transistors sustain oscillation by compensating for the loss in the tank. This oscil-

lator has become very popular in high frequency circuit design due to its ease of implementation, differential operation and good phase noise performance [9, 11].

3.2 Linear Analysis

The cross-coupled differential LC oscillator can be easily examined using the negative resistance technique introduced in section 2.3. Figure 3.2 shows the two parts of the circuits that will be used to calculate the impedances Z_A and Z_B. Note that part A consists of only passive devices (LC tank) while part B consists of the active devices (cross-coupled transistors).

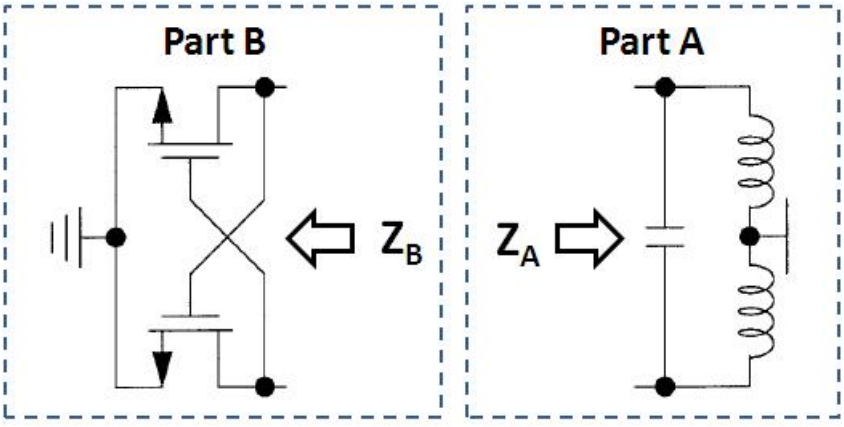

Figure 3.2: Negative resistance analysis of cross-coupled differential LC oscillator.

The impedance exhibited by part A can be easily calculated by modeling the resonator as a parallel RLC circuit as shown in Figure 2.6. The resistance R_P models the loss of the inductor as well as the varactor. R_P is related to the quality factor of the inductor and capacitor by

$$\begin{aligned} R_P &= \frac{Q_{IND}Q_{CAP}}{Q_{IND}+Q_{CAP}}\omega L \\ &= Q_{TANK}\omega L \end{aligned} \tag{3.1}$$

where ω represnts the frequency of operation, Q_{IND} and Q_{CAP} represent the quality factor of the inductor and capacitor respectively. The quality factor of the inductor and capacitor can be combined to obtain an overall quality factor of the resonator called Q_{TANK} as shown in Equation 3.1.

The impedance of the cross-coupled transistors (part B) can be evaluated by replacing the transistors with their small-signal hybrid pi model as shown in Figure 3.3.

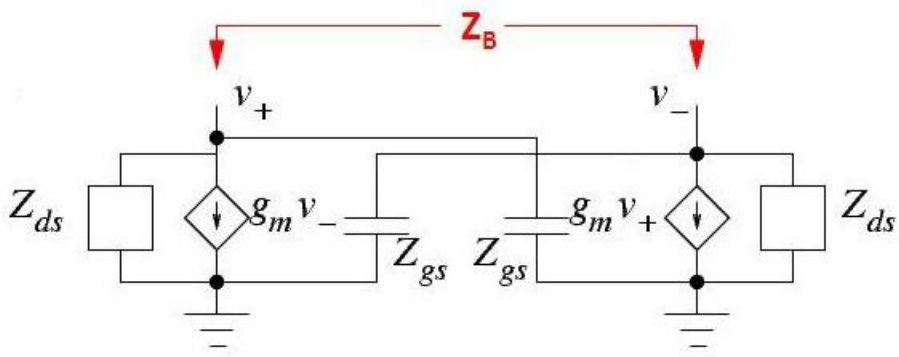

Figure 3.3: Small-signal analysis of cross-coupled transistors.

Gate to drain capacitances are not included in Figure 3.3 since they appear in parallel with the resonator and are thus included in the tank capacitance. The impedance of cross-coupled transistors obtained using Figure 3.3 is given by

$$Z_B = \frac{-2}{g_m\left(1 - j\frac{\omega}{\omega_T}\right)} \tag{3.2}$$

where it is assumed that

$$\begin{aligned} Z_{GS} &\ll Z_{DS} \\ Z_{GS} &\backsimeq \tfrac{1}{j\omega C_{GS}} \\ \omega_T &\backsimeq \tfrac{g_m}{C_{GS}} \end{aligned} \tag{3.3}$$

In the above equations g_m represents transconductance, ω represents the frequency of operation and ω_T represents the transition frequency of the transistors. Equation

3.2 shows that the impedance of the cross-coupled pair can be simplified to $-2/g_m$ if the transition frequency is much greater than the frequency of oscillation.

In order for oscillations to start and grow impedances Z_A and Z_B must satisfy Equation 2.4. The reactance part of Equation 2.4 can be satisfied at the resonance frequency of the LC tank which is given by

$$\omega_0 = \frac{1}{\sqrt{L(C + 2C_{GD})}} \tag{3.4}$$

where C_{GD} represents the gate to drain capacitance of the cross-coupled transistors. The resistance part of Equation 2.4 can be satisfied by assuming that the transition frequency is much greater than the frequency of oscillation and setting the transconductance as follows

$$g_m > \frac{2}{R_P} = \frac{2}{Q_{TANK}\omega_0 L} \tag{3.5}$$

The transconductance g_m is generally set much higher than its minimum value to ensure that oscillations start in the presence of process, voltage and temperature variations.

3.3 Steady-State Analysis

The basic current-voltage (I-V) characterestics of a differential pair is shown in Figure 3.4. In the linear region both the transistors are switched on while in the nonlinear region one of the transistors is switched off and the other the transistor carries all the bias current. Figure 3.4 shows that the differential pair becomes more nonlinear as the differential input voltage exceeds a certain limit.

The differential input voltage also happens to be the differential output voltage in the cross-coupled LC oscillator shown in Figure 3.1. As described in section 2.5

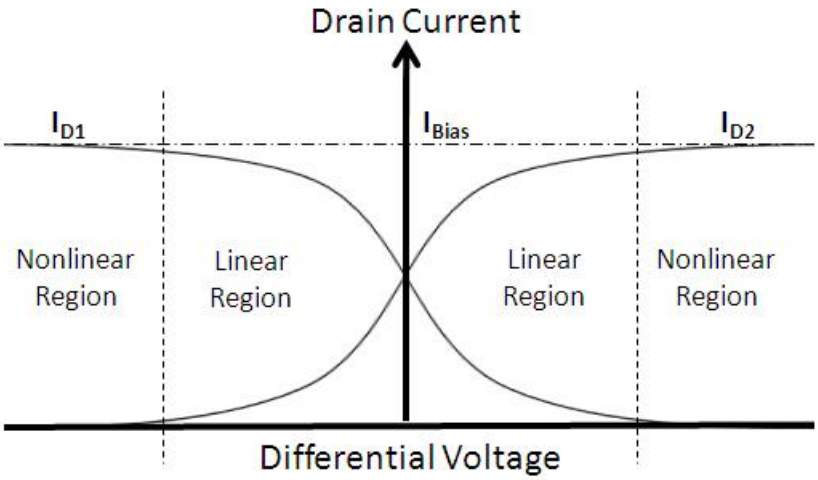

Figure 3.4: I-V characterestics of a differential pair.

the output of a properly designed cross-coupled LC oscillator keeps growing until this limit is exceeded and the loop gain of the oscillator reduces to its steady-state value of one. This causes the bias current to switch from one transistor to another in steady-state as shown in Figure 3.5.

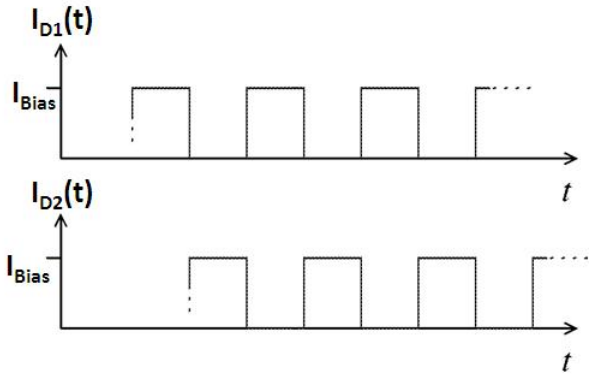

Figure 3.5: Steady-state current flow through each cross-coupled transistor.

Steady-state analysis can be further simplified by incorporating the above current waveforms into the equivalent circuit model shown in Figure 3.6. The current source found in the equivalent circuit model represents the differential current flowing into

the resonator while the parallel RLC network models the resonator as described in section 2.4.

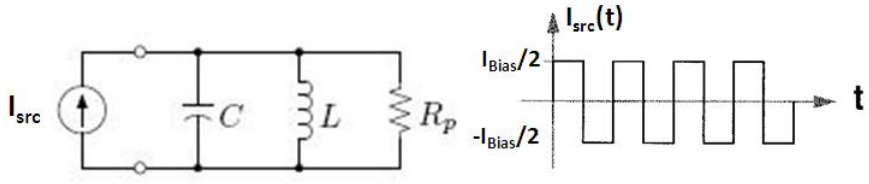

Figure 3.6: Equivalent circuit model at steady-state.

The resonator in the equivalent circuit acts a low pass filter allowing only the fundamental component of the current to pass while attenuating all other harmonics. Decomposing the current waveform using Fourier series provides the amplitude of the fundamental component which can then be used to derive the amplitude of oscillation as shown in Figure 3.7.

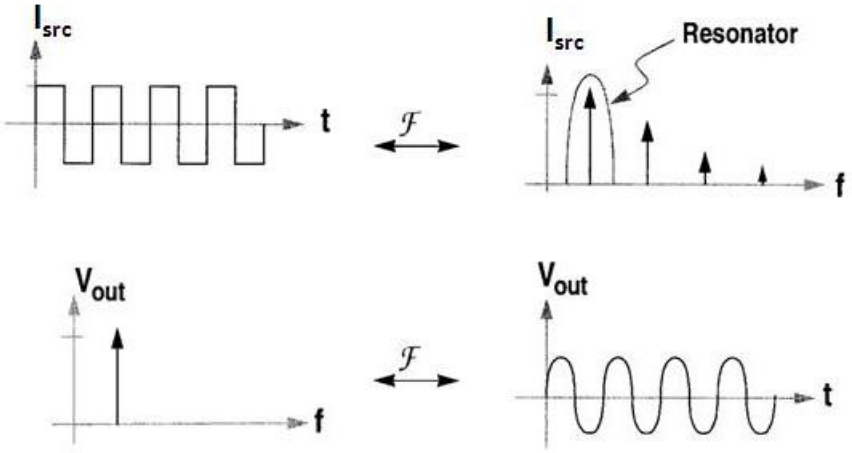

Figure 3.7: Derivation of the steady-state amplitude.

The steady-state amplitude of oscillation (single-ended) is given by

$$V_{out} = \frac{2}{\pi} R_P I_{Bias} = \frac{2}{\pi} \omega_0 L Q_{TANK} I_{Bias} \tag{3.6}$$

where Equation 3.5 is used to replace R_P in terms of the quality factor of the tank and the frequency of oscillation. Equation 3.6 suggests that the amplitude of oscillation can be increased indefinitely by increasing the bias current. However the current source transistor is driven into the triode region as the amplitude gets very large. This limits the amplitude of oscillation to $2V_{DD}$ [12]. The region of operation where the bias current limits the amplitude is called current-limited regime while the other region where supply voltage limits the amplitude is called voltage-limited regime.

3.4 Linear Noise Analysis

The effect of noise on the performance of the cross-coupled LC oscillator can be analyzed very easily by assuming that the oscillator behaves as a linear time invariant (LTI) system. This provides an invaluable insight into the operation of the oscillator while exposing the various parameters that can be used to optimize its performance. The phase noise model obtained using the above assumption is widely known as the Leeson-Cutler model and is given by [13]

$$L\left(\triangle\omega\right) = 10log\left[\frac{2kFT}{P_{out}}\left(1+\left(\frac{\omega_0}{2Q_{TANK}\triangle\omega}\right)^2\right)\left(1+\frac{\triangle\omega_{1/f^3}}{|\triangle\omega|}\right)\right] \tag{3.7}$$

where $L\left(\triangle\omega\right)$ represents the single sideband phase noise in dBc/Hz, ω_0 represents the frequency of oscillation, $\triangle\omega$ represents the frequency offset away from ω_0, Q_{TANK} represents the quality factor of the LC tank (resonator), P_{out} represents the average output power, F is an empirical fitting parameter, T is the temperature in Kelvin, K is the Boltzmann's constant and $\triangle\omega_{1/f^3}$ is defined as shown in Figure 3.8.

The Leeson-Cutler model shown in Equation 3.7 suggests that the phase noise of the oscillator can be improved by increasing the quality factor of the tank or output power of the oscillator. The output power of the oscillator however is dependent on

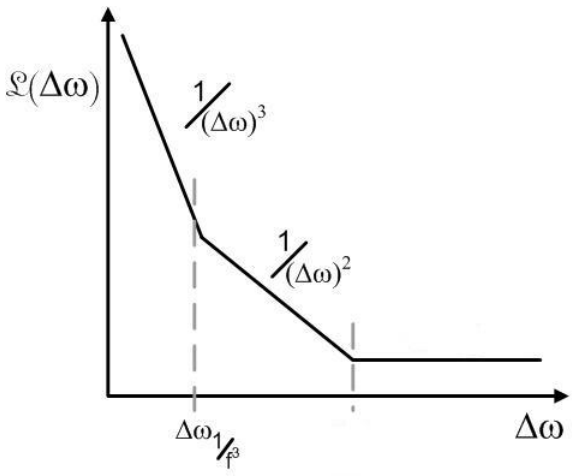

Figure 3.8: Leeson-Cutler phase noise model.

the quality factor of the resonator as shown by Equation 3.6. By combining Equation 3.6 and Equation 3.7 one can see that the phase noise is inversely proportional to cube of the quality factor. This explains the near obsession of oscillator designers to improve the quality factor of the resonator.

The Leeson-Cutler phase noise model described above does not account for frequency translation of noise which is inherently present due to the nonlinear operation of the oscillator. Various models have been suggested that take into account the different physical phenomenon resulting in phase noise [9, 14]. Though these models accurately predict the behavior of oscillators they do not provide any additional guidelines to optimize the performance of the oscillator.

3.5 Flicker Noise Analysis

The bias current source generates the majority of flicker noise in the cross-coupled LC oscillator [15]. This noise is not only composed of noise generated from the tail transistor but also the noise generated from the current mirror and its bias circuit. Any fluctuation in the bias current gives rise to a change in the frequency which in

turn results in phase noise [16]. In fact the close-in phase noise of the oscillator is dominated by the upconverted flicker noise of the current source [15].

The input-referred voltage (normalized to one Hz) at the gate of a MOSFET due to flicker noise is given by [17]

$$v_n^2 = \frac{K_F}{WLC_{OX}^2}\frac{1}{f} \tag{3.8}$$

where K_F is a process dependent parameter, C_{OX} represents the gate-oxide capacitance per unit area, W and L are the effective width and length of the transistor and f represents the frequency. Referring the noise voltage at the gate to drain current gives

$$i_n^2 = \frac{2\mu K_F I_D}{L^2 C_{OX}}\frac{1}{f} \tag{3.9}$$

where I_D represents the quiescent drain current flowing through the transistor and μ represents the effective mobility of the majority carrier. Equation 3.9 shows that the flicker noise of the tail transistor can be reduced by increasing the effective length of the transistor while keeping the drain current constant. Furthermore a capacitor can be added in parallel with the tail transistor to shape the bias current as pulses. This reduces the upconversion of flicker noise and improves the close-in phase noise [18].

CHAPTER 4

DIFFERENTIAL LC OSCILLATOR DESIGN

4.1 Overview

Typical clock data recovery circuits found in high-speed serial links require the voltage controlled oscillator to have a very low phase noise in order to minimize the jitter in the sampling clock. This ensures that the bit error rate (BER) of the system is not limited by the oscillator. Sections 4.2 to 4.7 provide a brief overview of the design of a differential cross-coupled LC oscillator operating at 25 GHz in 65-nm, low power IBM process. Section 4.8 reviews the simulated performance of the designed oscillator and discusses the trade-off that exists between power consumption and phase noise.

4.2 Resonator Design

The resonator is a fundamental part of an oscillator. It not only determines the frequency of oscillation but also governs the performance of the oscillator. The resonator chosen for the above design consists of a parallel LC tank similar to the one shown in Figure 2.6. However the capacitor in the LC tank is replaced with differentially biased PN junction varactors to vary the frequency of oscillation. Differentially biased PN junction varactors are employed to reduce the impact of noise present in the control lines on the frequency of oscillation.

The parallel LC tank is designed to maximize the quality factor of the resonator at the frequency of oscillation while maintaining a large tuning range (5%). The higher quality factor helps to reduce phase noise while the larger tuning range helps to ensure proper operation under process, voltage and temperature variations. An inductance of 300 pH is chosen as an initial estimate as it is small enough to achieve a tuning range of 5%. This corresponds to a capacitance of 135 fF as shown below

$$C = \frac{1}{\omega_0^2 L} = 135\ fF \tag{4.1}$$

The design of the inductor and differentially biased PN junction varactors based on the initial estimates found above are described in the following sections.

4.3 Inductor Design

Phase noise associated with an LC oscillator can be minimized by maximizing the quality factor of the resonator as explained in section 2.4. Equation 3.1 shows that the inductor plays a key role in determining the quality factor of the resonator. Inductors can be realized in several ways such as external inductors, bondwire inductors and on-chip inductors. External and bondwire inductors are avoided despite their high quality factor due to the large parasitic capacitance introduced by the ESD (Electrostatic Discharge) protection devices. On-chip inductors on the other hand have low quality factor due to finite resistivity of metal and finite conductivity of substrate. This is the reason why the LC tank shown in Figure 3.1 includes a differential inductor as it provides a higher quality factor as compared to single ended inductors [19].

Symmetric spiral inductor with a center tap and a low impedance ground plane is chosen in this design to maximize the highest achievable quality factor. A typical layout of the inductor is shown in Figure 4.1.

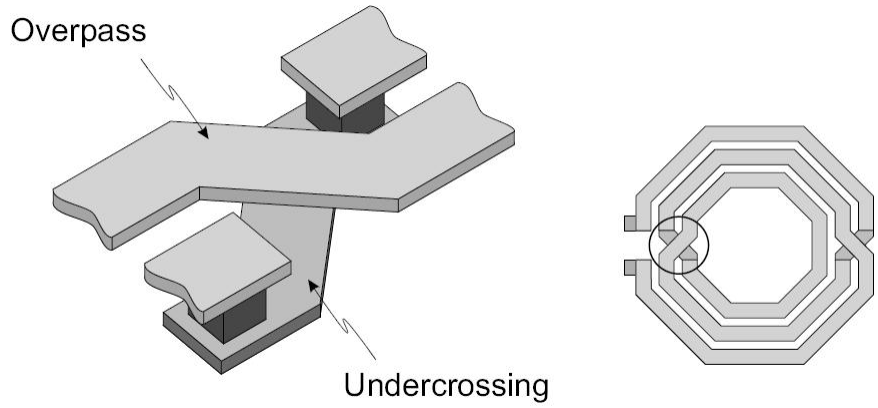

Figure 4.1: Multiple layer symmetric spiral inductor.

This structure however suffers from low self-resonant frequency due to the increased capacitance between the lowest metal layer and the ground plane. The inductor consists of multiple layers of metal connected to one another through shunt via bars. The center tap is included to allow the inductor to operate differentially. Differential operation reduces the losses in the inductor due to the presence of a virtual ground at the symmetric centre.

Self-resonant frequency and quality factor are the two major figures of merit that are used to characterize on-chip inductors. The self-resonant frequency is defined as the frequency above which the inductor starts behaving like a capacitor. Hence it describes the range of frequencies over which the inductor can be used. Quality factor has been defined previously in section 2.4. Spectre RF simulation tool was used to optimize the symmetric spiral inductor to achieve the highest possible quality factor at 25 GHz while ensuring that the self-resonant frequency is as high as possible.

Figure 4.2 shows the quality factor as a function of frequency for the optimized inductor.

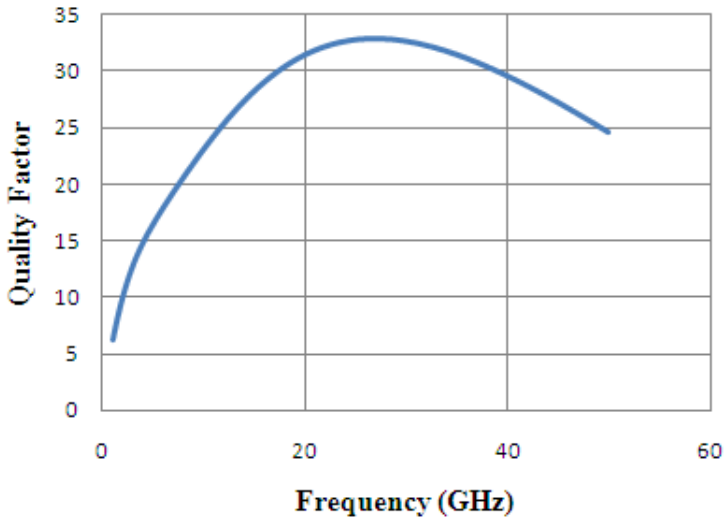

Figure 4.2: Quality factor of the optimized inductor as a function of frequency.

The optimized inductor consists of one turn with an outer diameter of 149 um. The inductor exhibits an inductance of 330 pH and a quality factor of 32 at 25 GHz while the self-resonant frequency is above 80 GHz. Figure 4.2 shows that the quality factor of the inductor peaks around 25 GHz as desired.

4.4 Varactor Design

A varactor is a tunable capacitor that is widely used in communication circuits. The most commonly used varactor is a reverse biased PN junction diode. In reverse bias, the bias voltage controls the width of the depletion region which in turn determines the junction capacitance. In general the junction capacitance can be expressed

as function of the bias voltage [20] as

$$C_j = \frac{C_{j0}}{\sqrt[m]{1 + \frac{V_R}{V_0}}} \tag{4.2}$$

where C_j is the juntion capacitance, C_{j0} is the junction capacitance obtained without bias voltage, V_0 is the built-in junction voltage, V_R is the reverse bias voltage and m is the grading coefficient. The value of grading coefficient depends on the doping concentration profile across the PN junction. Figure 4.3 shows the typical variation of junction capacitance as a function of reverse bias voltage for an abrupt PN junction diode in various technologies at 1 GHz.

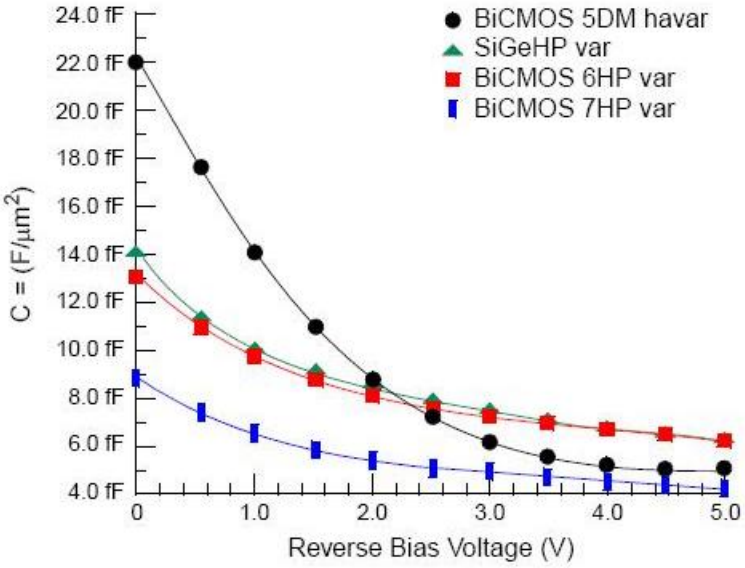

Figure 4.3: Typical variation of junction capacitance with reverse bias.

The 65-nm IBM process used in this design includes hyperabrupt junction diodes that provide an inverse square-law relation between capacitance and bias voltage as compared to the one shown in Equation 4.2. This results in a nearly linear variation of frequency with the bias voltage. The rate of change of frequency with the bias voltage is defined as gain of the oscillator, K_{VCO}.

Frequency tuning is typically implemented keeping in mind the effect of noise on the control lines. This is because any variation on the control lines results in frequency fluctuation which adds to the phase noise of the oscillator. Minimizing K_{VCO} and employing differential tuning are the two commonly used methods of lowering the effect of noise on the control lines. Differential tuning is preferred over single-ended tuning as it improves the common mode noise rejection on the control lines. Differential tuning using hyperabrupt junction diodes can be realized using the bridge structure shown in Figure 4.4 where matched resistors are used to set the common mode voltage.

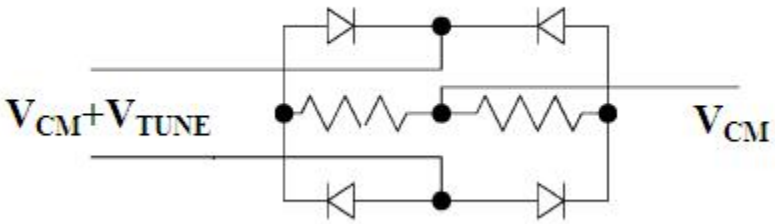

Figure 4.4: Differential tuning using a four point bridge structure.

In Figure 4.4, V_{CM} represents the common mode voltage of all the nodes while V_{TUNE} represents the differential tuning voltage. V_{CM} is set to $V_{DD}/2$ in order to maximize the differential tuning voltage that can be applied to the bridge structure without forward biasing any of the diodes. This helps to minimize K_{VCO} which improves the noise immunity of the oscillator. The optimized bridge structure consists of hyperabrupt PN junction diodes with a width of 1.15 um, length of 1.05 um and a multiplicity of 15.

Figure 4.5 shows the variation in capacitance with tuning volatge at 25 GHz in the optimized bridge structure. Note that the variation of capcitance shown in Figure 4.3

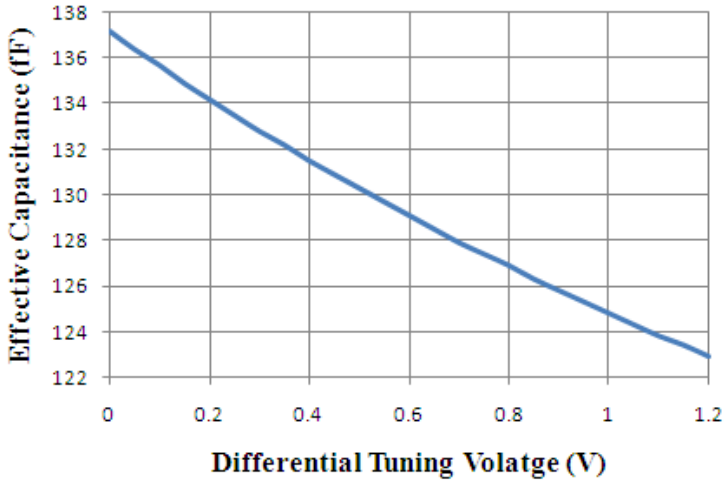

Figure 4.5: Variation of capacitance at 25 GHz in the optimized bridge structure.

and Figure 4.5 are different due to the presence of hyperabrupt PN junction diodes in the bridge structure.

4.5 LC Tank Simulation

The LC tank formed by the symmetric spiral inductor and the differentially tuned bridge varactor described above is shown in Figure 4.6.

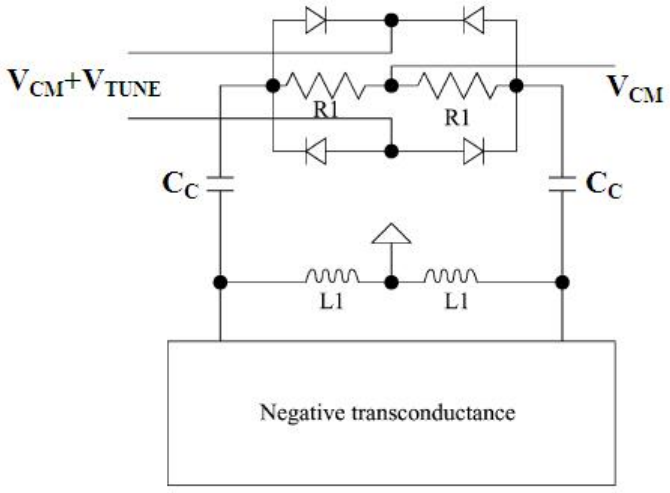

Figure 4.6: LC tank formed by symmetric spiral inductor and bridge varactor.

Coupling capacitors (C_C) are included to isolate the common mode voltage set by the spiral inductor and the bridge varactor.

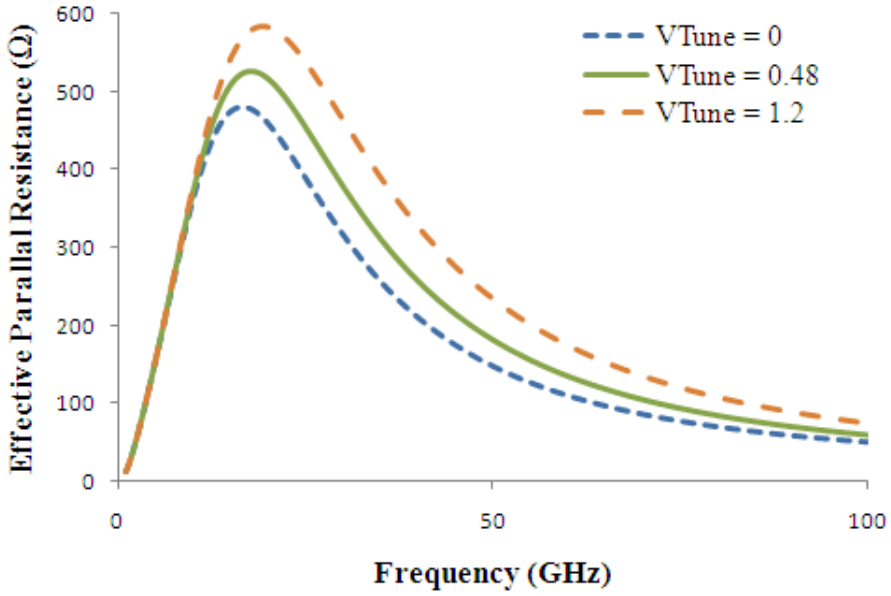

Figure 4.7: R_P as function of frequency at different values of tuning voltage.

Figure 4.7 shows the effective parallel resistance (R_P) seen looking into the LC tank. Figure 4.8 shows the variation in the resonance frequency as a function of the tuning voltage.

Note that the frequency varies almost linearly due to the presence of hyperabrupt diode in the resonator. The slope of the trace provides the gain of the voltage controlled oscillator, K_{VCO}.

4.6 Differential Pair Design

The cross-coupled differential pair shown in Figure 3.1 forms the energy restoring element in the oscillator described above. The design of the differential pair begins with Equation 3.5 where the effective parallel resistance of the resonator (R_P) is

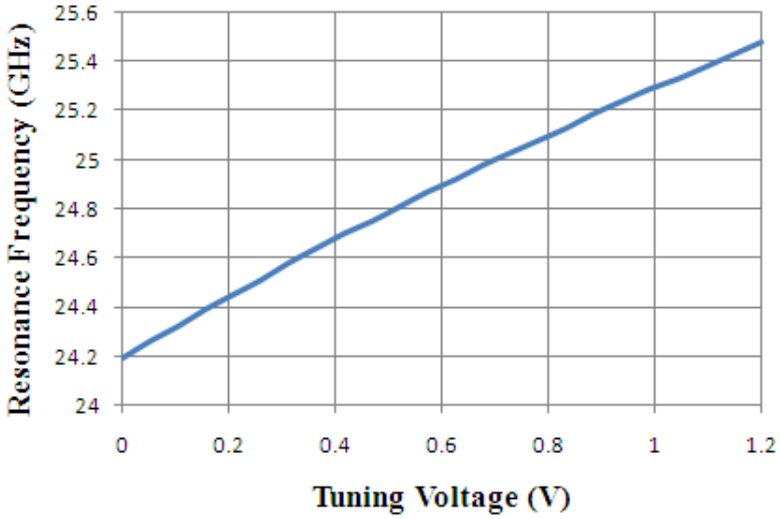

Figure 4.8: Resonance frequency as function of tuning volatge.

shown in Figure 4.7. Making use of Equation 3.5 and Figure 4.7, the transconductance can be expressed as

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} = \sqrt{2KI_DW/L} > \frac{2}{R_P} = 4\,{}^{mA}/_{V} \tag{4.3}$$

where V_{GS} represents the gate to source voltage, V_{TH} represents the threshold voltage, I_D represents the drain current, W represents the effective width, L represents the effective length and K is a process dependent parameter. Equation 4.3 suggests that g_m can be made as large as possible by choosing an appropriate aspect ratio (W/L) for a given value of drain current. However the drain current density must be chosen carefully to maximize the transition frequency of the transistor. This ensures that the cross-coupled differential pair does not significantly alter the frequency of oscillation by minimizing the reactive part of its input impedance. Table 4.1 shows the variation in the transition frequency with current density in the 65-nm, low power IBM process with 1.2 V supply volatge.

Table 4.1: Variation in transition frequency with current density.

$V_{GS}\,(V)$	$V_{TH}\,(V)$	$I_D\,(uA)$	$W\,(nm)$	$L\,(nm)$	$\frac{I_D}{W}\,(^{\mathrm{uA}}/_{\mathrm{um}})$	$F_T\,(GHz)$
0.948	0.517	265	600	60	26.5	186
0.817	0.517	203	600	60	20.3	182
0.749	0.517	143	600	60	14.3	176
0.699	0.517	115	600	60	11.5	168

Once a particular current density is chosen, the aspect ratio and the drain current of the transistors can be determined to achieve a specific value of transconductance. The transconductance of the differential pair is chosen to be at least twice as large as its minimum value to ensure that oscillation start in the presence of process, voltage and temperature variations. Table 4.2 lists the drain current and the dimensions of the transistor needed to achive a specific value of g_m for the different current densities shown in Table 4.1.

Table 4.2: Drain current and transistor dimensions to satisfy Equation.4.3

$g_m\,(^{mA}/_{V})$	$W\,(um)$	$L\,(nm)$	$I_D\,(mA)$
6	5.85	60	2.58
6	6.00	60	2.02
6	6.41	60	1.53
6	6.80	60	1.30

The length of the transistors is set to the minimum value of 60 nm in all cases to reduce the parasitic gate to drain capacitance which appears in parallel with the resonator. The optimized differential pair consists of 8 um wide transistors that attain a transition frequency of 182 GHz when biased with a drain current of 2.7 mA.

4.7 Tail Current Source Design

The tail current source is implemented using a current mirror structure. The length of the tail current transistor is set to 1 um to minimize the flicker noise as

explained in section 3.5. A 250 fF capacitor is added in parallel with the current source transistor to reduce the flicker noise upconversion in the oscillator [18].

4.8 Simulated Oscillator Performance

Figure 4.9 shows a schematic of the completed cross-coupled differential LC oscillator.

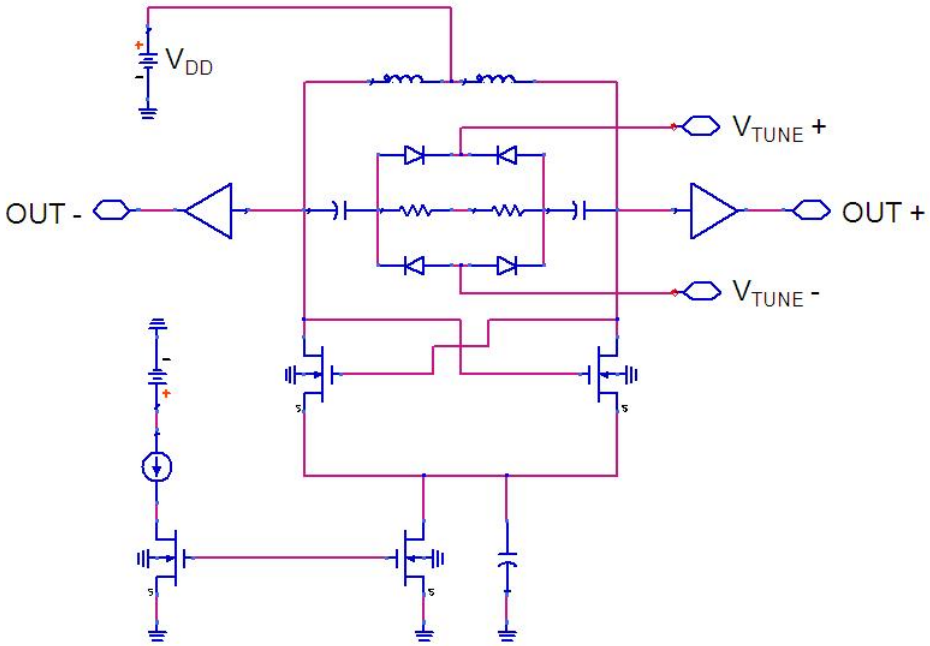

Figure 4.9: Completed schematic of the differential LC oscillator.

The oscillator consumes 5.4 mA from a 1.2V supply. Its frequency of oscillation can be tuned from 24.2 GHz to 25.4 GHz resulting in a K_{VCO} of 1000 MHz/V. Figure 4.10 shows the phase noise of the oscillator as a function of the tail current source.

The phase noise of the oscillator can be improved at the expense of power as expected. The oscillator has a simulated phase noise of -103 dBc/Hz at an offset of 1 MHz (V_{TUNE} = 0.6 V). A figure of merit (FOM) usually used to compare the oscillators is defined below

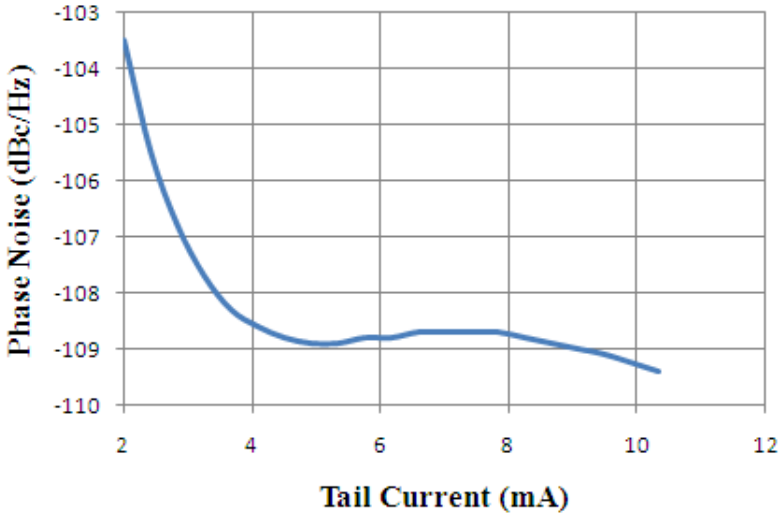

Figure 4.10: Phase noise as function on the tail current.

$$FOM = 10Log\left[\left(\frac{\omega_0}{\triangle\omega}\right)^2 \frac{1}{L\left(\triangle\omega\right)P}\right] \tag{4.4}$$

where ω_0 is the frequency of oscillation, $\triangle\omega$ is the frequency offset, $L\left(\triangle\omega\right)$ is the single sideband phase noise evaluated at a frequency offset $\triangle\omega$ away from the frequency of oscillation and P represents the power consumed by the oscillator in milliwatts. The figure of merit for the voltage controlled oscillator designed above is 183.

CHAPTER 5

CONCLUSIONS

In this thesis a fully differential LC oscillator was designed in 65-nm, low power IBM process. The simulated performance of the oscillator is comparable to the ones seen in recent literature. The small tuning range of the oscillator can be improved by employing switched capacitor banks in parallel with the bridge varactor [21]. Similarly the phase noise of the oscillator can be improved by including noise filters and shaping the tail current appropriately [18] . However the main purpose of the project was to design a voltage controlled oscillator whose power consumption can be reduced drastically at the expense of performance. Figure 4.10 shows that the oscillator designed above meets the above requirement.

CHAPTER 6

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