TRANSISTOR LEVEL X-PARAMETER SIMULATIONS OF EQUALIZATION CIRCUITS

BY

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THESIS

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ABSTRACT

As frequencies have increased in circuits used for communication electronics, signal integrity concepts have become some of the foremost challenges that circuit designers must deal with. Specifically, high-speed links have been the focus of much of the research into mitigating signal integrity issues. To combat the effects of jitter and other signal integrity problems, circuit designers have begun using increasingly more complex circuitry peripheral to the high-speed link. This presents a challenge for system level designers because of their reliance on models accurately characterizing the underlying transistor level design. Existing standards, such as IBIS-AMI, are currently used at the system level to create designs. Alternatively, X-parameters may present a more intuitive and accurate method to generate models that are detailed and that preserve intellectual property.

The open mind, the reliance on example and persuasion rather than authority—these are the heritage of the centuries in which science has altered the face of the earth.

-J. Robert Oppenheimer

ACKNOWLEDGMENTS

I would like to thank the usual suspects: friends, family and colleagues. Specifically, I would like to acknowledge José E. Schutt-Ainé, Xu Chen, Rishi Ratan, Drew Handler, Yubo Liu, and Tom Comberiate for their support at various times during the research and writing phases of this thesis. Lastly, I would like to thank Ferd and Ruby.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Signal integrity has steadily become more important in the circuit design community because of the increasing data rates found in high-speed links. The rates have increased to the point where channels are best modeled using distributed elements. In essence, the channels can be modeled using the classic transmission line approach familiar to microwave engineers. Effects such as dispersion and impedance mismatch have become relevant to the digital design community. Because digital design is often dependent on synchronous systems, any behavior that has the potential to disrupt this synchronicity is considered adversarial.

In order to engage in system level design, it is important to have a behavioral level model that is both concise and accurate. Due to the importance of the high-speed link in system design, signal integrity engineers have developed and are still developing methods for modeling their operation. The non-ideal behavior of the high-speed link has been observed, categorized and is reasonably well understood. The objective of the circuit designer is to develop high-speed links that are not only robust to this behavior but also have the ability to combat these issues. The objective for the model designer is to capture the behavioral level model of the high-speed link.

Signal integrity figures of merit are discussed in the following chapter. Chapter 2 introduces the IBIS-AMI model and describes its features and potential alternatives. Chapter 3 introduces X-Parameters and their potential role in signal integrity modeling. Agilent ADS is the primary tool used to generate X-parameters and its usage is described in chapter 4. The results and contributions of this thesis are discussed in chapter 5. Chapter 6 describes the conclusions drawn from this thesis and future work is proposed.

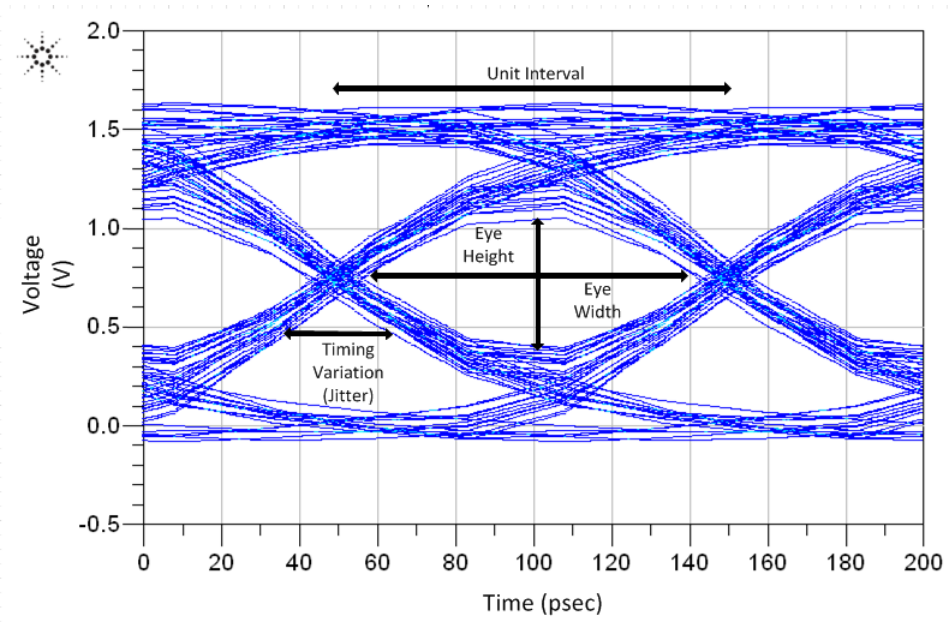

Figure 1.1: Eye diagram

1.2 Signal Integrity: Jitter and the Eye Diagram

Dispersion, impedance mismatch and other electromagnetic effects manifest themselves in digital systems in the form of jitter. Jitter is defined as the deviation of a signal timing event from its ideal position [1]. The most popular figure of merit used to capture jitter and other non-ideal behavior is the eye diagram as shown in Figure 1.1. The eye diagram is constructed by slicing a random bit stream transmitted through the link in question at regular unit intervals equal to the bit rate. The resulting bits are then superimposed and displayed on the same diagram.

The ideal eye diagram would have a rectangular opening with width equal to the bit rate and height equal to the voltage swing of the circuit. The example eye diagram in Figure 1.1 differs from this ideal behavior. The eye diagram was created using a 10 Gb/s random bit stream. The width of the eye is essentially a function of jitter and the rise and fall times of the bit stream. Because digital systems rely on the ability to reliably slice up bit streams and make decisions regarding bit values, the "eye opening" is an important design parameter to consider.

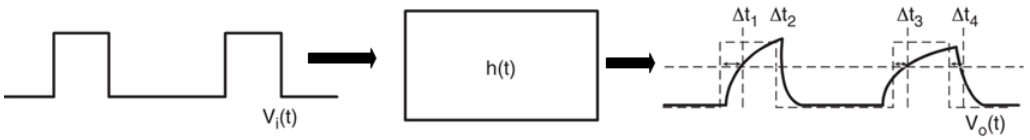

Figure 1.2: Data-dependent Jitter is caused by the limited bandwidth of the channel.

1.3 Types of Jitter

Roughly speaking, jitter can fall into two categories: random jitter or deterministic jitter. Deterministic jitter is usually data dependent [1]. Regardless of the channel used for communication, it will be band-limited. Because the channel has a limited bandwidth and bit streams have a wide bandwidth, distortion in the form of ringing and increased rise/fall time can be expected. Figure 1.2 displays what effects these properties have on bit streams. The output signal, $V_o(t)$, is the result of the familiar convolution operation $V_i(t) * h(t) = V_o(t)$.

Random jitter can be approximated as white noise using the Gaussian distribution. It is the result of a combination of noise sources [1]. Electronic noise sources include thermal noise and shot noise. It is also the result of system level noise sources such as cross-talk and supply noise. Figure 1.3 shows an example eye diagram with the distribution given for the jitter. As shown, if a more detailed model is available for the distribution, it should be used.

1.4 Circuit Designers and Jitter

The challenge for circuit designers is to develop circuits and systems that operate reliably and efficiently in the presence of jitter. To achieve this objective, circuits are designed to combat the effects of jitter and voltage level variation. This added complexity solves some signal integrity problems at the circuit level but presents greater challenges for the system level designer. System level designs are only as accurate as the models used to build the systems. With added complexity, the circuits associated with high-speed links become harder to model. In the next chapter, the commonly used IBIS-AMI model will be discussed. Several advantages and disadvantages of

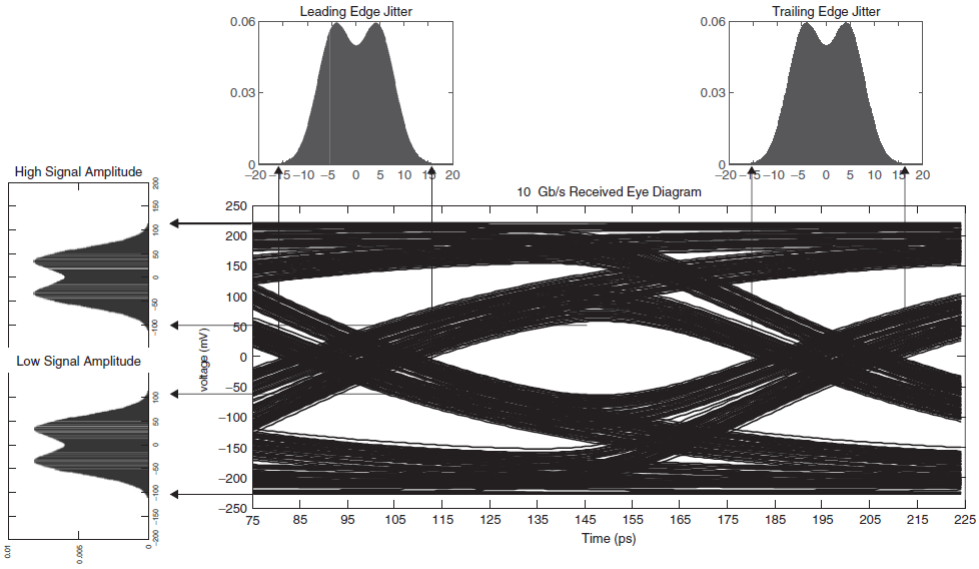

Figure 1.3: Random jitter with distribution shown [1].

this method will be analyzed. Near the end of the chapter, a new modeling paradigm using X-parameters will be introduced.

CHAPTER 2

IBIS-AMI

2.1 Basic Description and Methodology: IBIS

The Input-output Buffer Information Specification, Algorithmic Modeling Interface (IBIS-AMI) can be readily split into IBIS and AMI portions for analysis purposes. IBIS models are generated using a standardized process. Generally speaking, IBIS models are essentially look-up tables consisting of voltage versus time (V-t) and voltage versus current (V-I) tables. These tables effectively describe the switching and impedance characteristics of high-speed links. The V-t table is generated by recording the output voltage versus time as logic levels are toggled from low to high and high to low [2]. Figure 2.1 shows the basic setup. The I-V table is generated by sweeping a voltage source at the output of a buffer and recording the current for high and low logic states [2]. This basic setup is shown in Figure 2.2. The modeling technique is not limited to the circuit topology shown. These tables can be generated using any buffer circuit topology.

It is a common practice for companies to make available their IBIS models for their I/O devices. Because of the industry adoption of this standard, there are several advantages to system level design using IBIS. Most importantly, for the vendor, intellectual property is protected when using IBIS models. Another advantage is that several software design tools support the use of IBIS models. As long as a design tool has this support, IBIS models from different semiconductor vendors can be used in the same design simulation. In Figure 2.3, portions of an example IBIS model for an Actel I/O buffer can be observed.

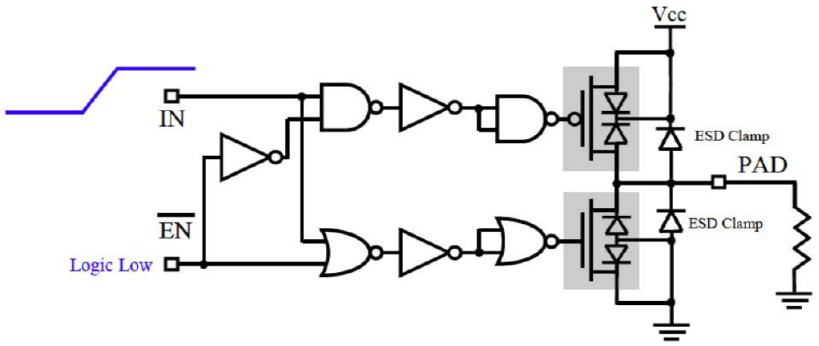

Figure 2.1: Process used to generate the switching (V-t) table [2].

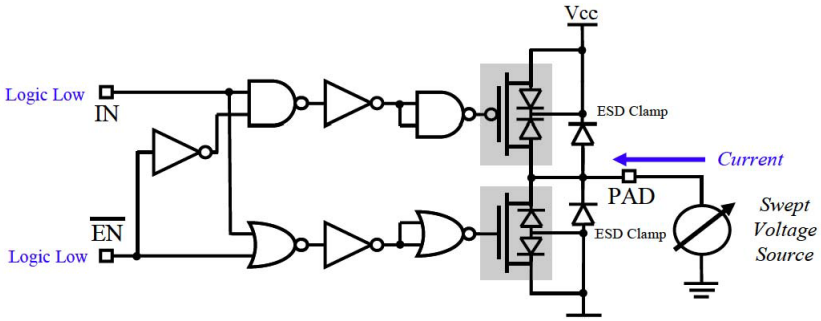

Figure 2.2: Process used to generate the impedance (I-V) table [2].

```
|
|*****************************************************************
|                          Model ttl3f1
|*****************************************************************
|
[Model]          ttl3f1
Model_type       I/O
Polarity         Non-Inverting
Enable           Active-High
Vinl =   0.8000V
Vinh =   2.0000V
Vmeas =  1.4000V
Cref =  5.0000pF
C_comp    1.036pF    0.949pF    1.123pF
|
|
[Temperature Range]       25.0000            85.0000            -40.0000
[Voltage Range]          3.3000V            3.0000V            3.6000V
[Pulldown]
| voltage     I(typ)              I(min)             I(max)
|
-3.3000         -10.9880mA         -8.4500mA         -14.4530mA
-3.1000         -10.9880mA         -8.4500mA         -14.4530mA
-2.9000         -10.9880mA         -8.4500mA         -14.4530mA
-2.7000         -10.9880mA         -8.4500mA         -14.4530mA
-2.5000         -10.9880mA         -8.4500mA         -14.4530mA
-2.3000         -10.9880mA         -8.4500mA         -14.4530mA
-2.1000         -10.9880mA         -8.4500mA         -14.4530mA
-1.9000         -10.9880mA         -8.4500mA         -14.4530mA
-1.7000         -10.9880mA         -8.4500mA         -14.4530mA
-1.5000         -10.9880mA         -8.4500mA         -14.4530mA
-1.0000         -10.9880mA         -8.4500mA         -14.4530mA
-0.9000         -10.9880mA         -8.4500mA         -14.4530mA
-0.8000         -10.9880mA         -8.4500mA         -14.4530mA
-0.7000         -10.9880mA         -8.4500mA         -14.4530mA
-0.6000         -10.9880mA         -8.4500mA         -14.4530mA
```

(a) A portion of the I-V table.

```
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.5134/1.6354e-10     0.3458/2.1713e-10     0.7314/1.0709e-10
dV/dt_f 0.6546/3.3844e-10     0.4698/4.7409e-10     0.8826/2.5300e-10
R_load = 50.0000
|
[Rising Waveform]
R_fixture = 50.000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
|
|  time          V(typ)        V(min)        V(max)
|
0.000S        5.632e-03        5.735e-03        5.357e-03
52.800pS        3.118e-03        3.549e-03        2.729e-03
118.800pS        2.541e-03        2.540e-03        2.657e-03
171.600pS        2.665e-03        2.493e-03        4.751e-03
237.600pS        3.239e-03        2.547e-03        1.381e-03
290.400pS        4.929e-03        2.433e-03        -8.344e-03
356.400pS        2.160e-03        2.693e-03        2.265e-02
369.600pS        1.278e-03        2.856e-03        5.211e-02
382.800pS        3.690e-04        3.085e-03        1.058e-01
396.000pS        -8.797e-04        3.347e-03        1.694e-01
409.200pS        -2.158e-03        3.675e-03        2.685e-01
422.400pS        -3.830e-03        4.007e-03        3.818e-01
435.600pS        -5.544e-03        4.346e-03        4.994e-01
448.800pS        -7.774e-03        4.564e-03        6.189e-01
462.000pS        -1.001e-02        4.532e-03        7.223e-01
475.200pS        -1.227e-02        4.368e-03        8.193e-01
488.400pS        -1.427e-02        3.936e-03        8.959e-01
501.600pS        -1.301e-02        3.505e-03        9.641e-01
```

(b) A portion of the V-t table.

Figure 2.3: Parts of the IBIS file for an Actel I/O buffer.

2.2 IBIS-AMI: Features

As described in the previous chapter, there exists circuitry peripheral to the buffer that is used to combat jitter and delay. The effects of this circuitry are significant in relation to the operation of modern Serial/Deserializer (SerDes) links. As discussed in Chapter 1, these added circuits and signal processing techniques make modeling SerDes devices increasingly difficult. IBIS-AMI was introduced to perform this function [3]. In addition to the IBIS model described in the previous section, an AMI model is also included in the IBIS-AMI definition. Its position in the high-speed link is shown in Figure 2.4. The usual model consists of a *.ibs, *.ami and a *.dll file. The .ami file has the potential to contain equalization filters that are nonlinear and time variant [3].

The primary purpose of the AMI is to model the analog front end (AFE), the decision feedback equalization (DFE) and clock data recovery (CDR) circuits associated with SerDes devices. The AFE generally consists of a variable gain amplifier (VGA) and a continuous-time linear equalizer (CTLE) [1]. The VGA and CTLE have varying architectures but their primary purpose is to counteract the low-pass behavior of the channel. This behavior is demonstrated in Figure 2.5. The objective of the VGA and the CTLE is to shift the corner frequency to a higher frequency. This effectively increases the bandwidth of a given channel. The VGA and the CTLE are essentially amplifiers that are designed to operate in the linear regime and whose frequency response improves the bandwidth of the channel. These assumptions of linearity may not be sound and are one of the subjects of the investigation presented in the proceeding chapters.

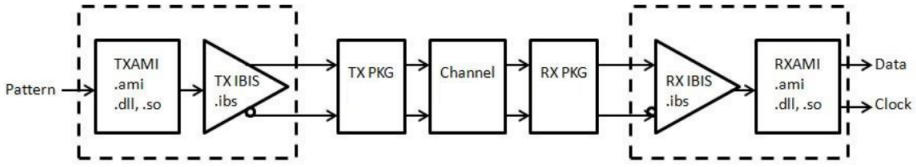

Figure 2.4: Highlighted portions of the high-speed link that are modeled by IBIS-AMI [4].

The DFE and CDR are time variant and potentially nonlinear processes. The DFE is responsible for the receiver equalization. It consists of an FIR

filter in a negative feedback loop [5]. The tapped delay line has weighted tap coefficients that are changed dynamically, based on the decision operation in the forward path. The CDR consists of a multi-phase PLL that "samples" the input data (bit stream) and the phase with the largest timing margin is selected as the clock [6]. The byte is recovered and the selection process begins with the next byte. One of the primary purposes of the AMI portion of the model is to capture this algorithmic behavior.

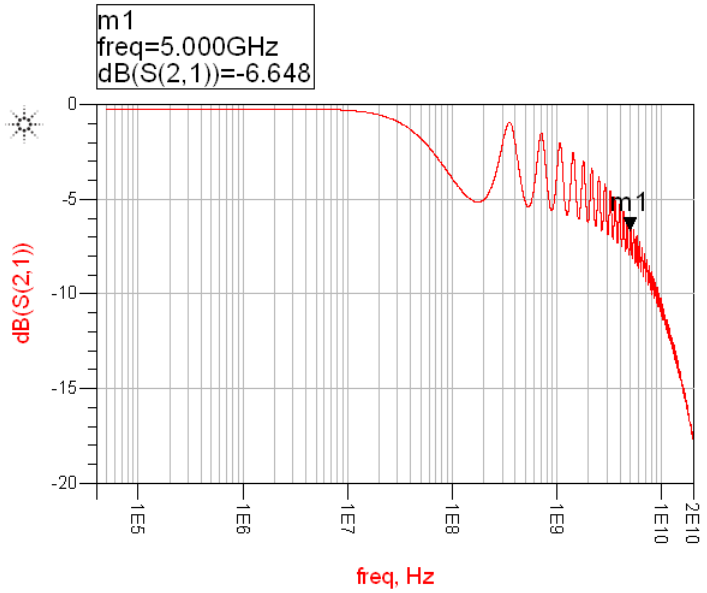

Figure 2.5: Low pass behavior of an example transmission line channel. Substrate: $\epsilon_r = 4.3, h = 31$ mil, $tan\delta = 0.02$.

2.3 IBIS-AMI: Methodology

Simulations utilizing IBIS-AMI models can only be performed using Electronic Design Automation (EDA) tools that support the standard. The first step in the simulation process is generation of the impulse response of the analog portion of the channel. The channel and the analog portions of the high speed link are approximated as linear [3]. The impulse response is generated for the through channel and the cross-talk channels. Using the approach shown in Figure 2.6, the impulse response is generated. The resulting vector is stored in an argument called the "impulse_matrix". Any filtering or equalization is defined in the "AMI_Init" argument and performed on the sampled

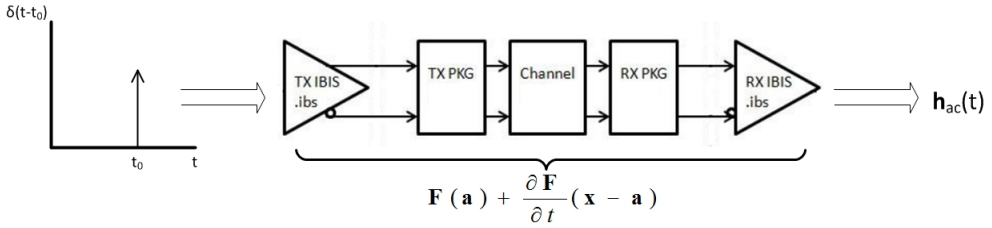

Figure 2.6: Generation of the impulse response of the analog portion of the channel.

data stored in the impulse_matrix. The transmitter and receiver may have differently defined AMI_Init arguments, depending on the model. The EDA then provides a digital stimulus to the system. The result is passed to the transmitter's "AMI_GetWave" definition and convolved (by the EDA tool) with the impulse response of the channel [3]. This result is passed to the receiver's AMI_GetWave and the resulting convolution is representative of the output of the IBIS-AMI simulation.

IBIS-AMI is the preferred method for high-speed link modeling because of its ability to characterize non-linear time variant systems. It is highly flexible and has the ability to capture the algorithmic behavior that is implemented on the circuit level. This modeling paradigm does present challenges, however. By approximating the channel and analog components of the link as linear systems, important behavior may be discarded. Additionally, due to the complexity of the standard, generation of an accurate IBIS-AMI is not a trivial task. X-parameters have the potential to replace portions of the IBIS-AMI standard with a paradigm that is more intuitive. Though X-parameters can only be used to measure time invariant systems, they can be used to more accurately model the nonlinear behavior of channels and analog front ends [7]. The X-parameter formalism is described in detail in the following chapter.

CHAPTER 3

X-PARAMETERS: THEORY AND INTUITION

3.1 S-parameter Theory

X-parameters are essentially a superset of the familiar S-parameters. In other words, it can be shown that under proper circumstances, namely small signal regimes, X-parameters can be reduced to S-parameter representations. To review, scattering parameters (S-parameters) relate power waves to ports. An example two port representation can be found in Figure 3.1. Let the voltage and current stimuli at a port be defined as:

$$v(x,t) = \mathbf{V}(x)e^{j\omega t}$$

$$i(x,t) = \mathbf{I}(x)e^{j\omega t}$$

The Telegraphers Equations in phasor form are as follows:

$$\frac{\partial \mathbf{V}(x)}{\partial x} = (R + \mathrm{j}\omega \mathrm{L})\mathbf{I}(x)$$

$$\frac{\partial \mathbf{I}(x)}{\partial x} = (G + \mathrm{j}\omega \mathrm{C})\mathbf{V}(x)$$

By taking the second derivative, the equations can be coupled [8] :

$$\frac{\partial^2 \mathbf{V}(x)}{\partial^2 x} = (R + \mathrm{j}\omega \mathrm{L})\frac{\partial \mathbf{I}(x)}{\partial x}$$

$$\frac{\partial^2 \mathbf{I}(x)}{\partial^2 x} = (G + \mathrm{j}\omega \mathrm{C})\frac{\partial \mathbf{V}(x)}{\partial x}$$

Solutions of these equations come in the form of:

$$y(x) = Ae^{\gamma x} + Be^{-\gamma x}$$

In this general solution, γ is complex, i.e. $\gamma = \alpha + j\beta$. This result implies that at a fixed distance $x = d$, the voltage and current at a given reference plane can be expressed as:

$$v(t) = \mathbf{V}(d)e^{j\omega t} = \underbrace{Ae^{\alpha d}e^{j(\omega t+\beta d)}}_{\text{forward-travelling wave}} + \underbrace{Be^{-\alpha d}e^{j(\omega t-\beta d)}}_{\text{backward-travelling wave}}$$

$$i(t) = \mathbf{I}(d)e^{j\omega t} = \frac{A}{Z_0}e^{\alpha d}e^{j(\omega t+\beta d)} - \frac{B}{Z_0}e^{-\alpha d}e^{j(\omega t-\beta d)}$$

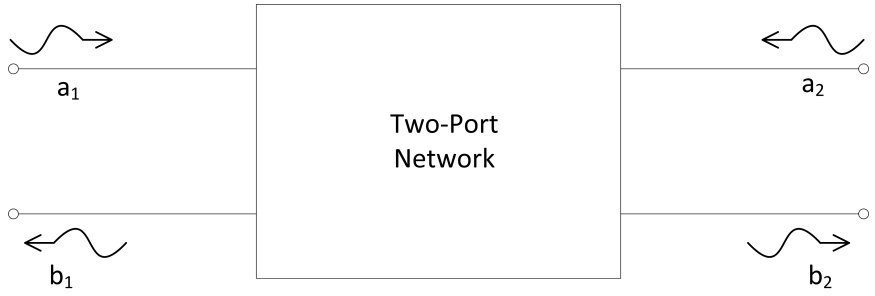

Figure 3.1: General representation of a two-port network.

In general, power waves are defined as:

$$a(t) = \frac{V^+(t)}{\sqrt{Z_0}}$$

$$b(t) = \frac{V^-(t)}{\sqrt{Z_0}}$$

where $V^+(t)$ and $V^-(t)$ are the forward and backward traveling waves that were previously defined. The forward and backward traveling power waves at the ports of a two-port system are related by the following equations:

$$b_1(t) = S_{11}(t) * a_1(t) + S_{12}(t) * a_2(t)$$

$$b_2(t) = S_{21}(t) * a_1(t) + S_{22}(t) * a_2(t)$$

From these equations it follows that [9] :

$$S_{11}(t) = \left.\frac{b_1(t)}{a_1(t)}\right|_{a_2=0}$$

$$S_{21}(t) = \left.\frac{b_2(t)}{a_1(t)}\right|_{a_2=0}$$

$$S_{22}(t) = \left.\frac{b_2(t)}{a_2(t)}\right|_{a_1=0}$$

$$S_{12}(t) = \left.\frac{b_1(t)}{a_2(t)}\right|_{a_1=0}$$

Assuming linear operation of the network of interest, the frequency dependent relationship between forward and backward traveling power waves can be expressed in a similar fashion. For a two-port system:

$$B_1(\omega) = S_{11}(\omega)A_1(\omega) + S_{12}(\omega)A_2(\omega)$$

$$B_2(\omega) = S_{21}(\omega)A_1(\omega) + S_{22}(\omega)A_2(\omega)$$

This relation implies that for a general n-port system [8] :

$$S_{ij}(\omega) = \left.\frac{B_i(\omega)}{A_j(\omega)}\right|_{\substack{A_n=0 \\ \forall n \neq j}}$$

As long as the network under test remains operating in a linear regime, the frequency content of a signal remains unaltered from input to output. As shown in Figure 3.2, the amplitudes of individual harmonics are amplified or attenuated but the harmonic content of the power waves is unchanged.

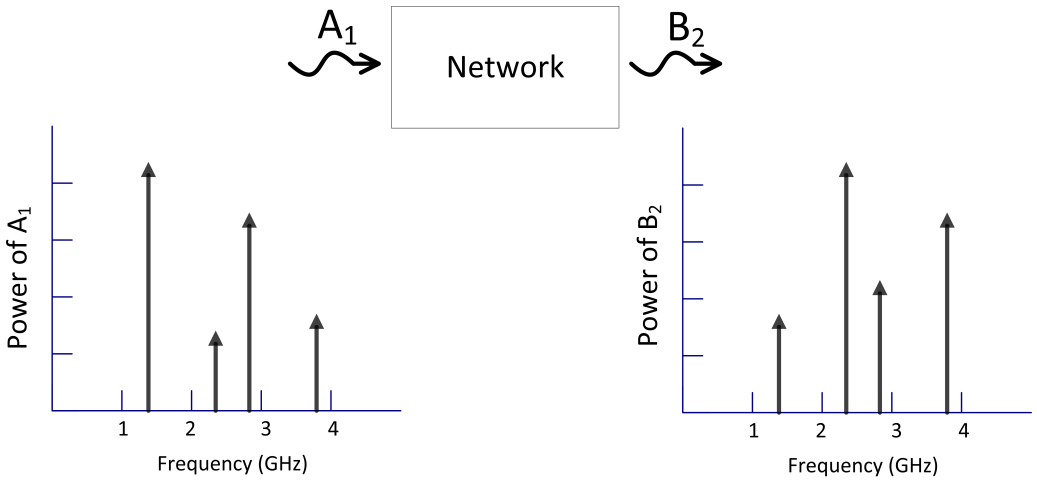

Figure 3.2: Linear frequency response of a network.

From the above analysis, it is clear that S-parameters can be used to model linear networks. Also, due to their "black box" nature, they can be used to protect intellectual property. Additionally, through a simple transformation, they can be cascaded in order to build a description for larger systems [8]. Though these properties are useful, S-parameters are limited to modeling linear systems. X-parameters are a superset of S-parameters in the sense that they have the ability to describe linear and nonlinear behavior.

3.2 X-parameter Theory

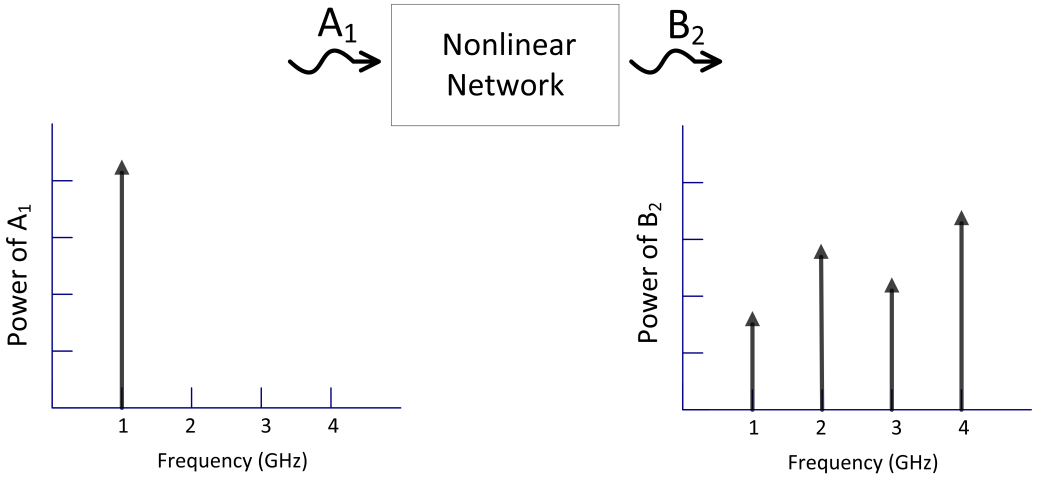

Figure 3.3: Frequency response of a nonlinear network.

S-parameters are the preferred method for linear network modeling. To model nonlinear networks, the X-parameter paradigm has been introduced. Figure 3.3 displays a typical response of a nonlinear system. It can be observed that a stimulus of a single harmonic results in a response containing several harmonics. The nonlinear mapping that governs the amplitude and phase of the output harmonics accounts for contributions from individual ports and incident harmonics. In general, the scattered waves can be expressed as [9]:

$$B_{p,k} = F_{p,k}(A_{1,1}, A_{1,2}, ..., A_{1,K}, A_{2,1}, A_{2,2}, ..., A_{2,K}, ..., A_{N,1}, A_{N,2}, ..., A_{N,K}).$$

Each $F_{p,k}()$ defines the response due to the incident phasor at every port of the N-port device under test. Additionally, the B-waves are influenced by the K harmonics of interest associated with the stimulus at each port.

This expression can be further analyzed to glean more information about the nature of the network or device being modeled. As described previously and as shown in Figure 3.3, the response of a nonlinear network to a single tone stimulus results in several harmonically related tones. Because the tones in the response are harmonically related, a cross-frequency phase can be defined. As shown in Figure 3.4, as long as the stimuli are harmonically related, an arbitrary reference can be established to define phase. This concept is referred to as a frequency grid, $f_k = kf_{fund}, k \in \mathbb{N}$, where f_{fund} is the fundamental frequency of interest [9]. The collection of tones that make up this grid are called commensurate tones. Defining the phase of our fundamental signal $A_{1,1}$ as $P = e^{j \cdot phase(A_{1,1})}$, all incident harmonics at each port can can be referenced to this phase. This means that the equation can be modified as shown in Equation 3.1. By reducing the dimensionality of the problem, further data processing becomes simpler.

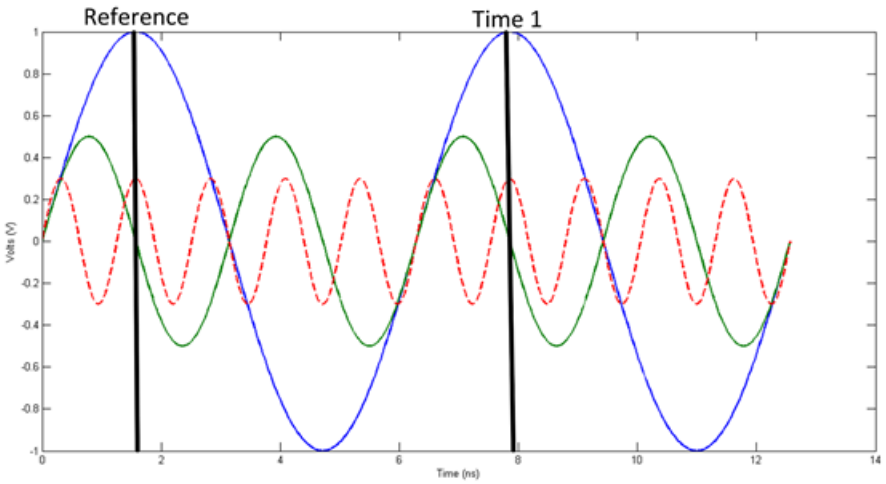

Figure 3.4: Cross-frequency phase defined for the first, second and fifth harmonic.

$$B_{p,k} = F_{p,k}\left(|A_{1,1}|, A_{1,2}P^{-2}, ..., A_{1,K}P^{-k}, A_{2,1}P^{-1}, A_{2,2}P^{-2}, \right. \\ \left. ..., A_{2,K}P^{-k}, ..., A_{N,1}P^{-1}, A_{N,2}P^{-2}, ..., A_{N,K}P^{-k}\right) P^{k} \quad (3.1)$$

The equation can be simplified further by modeling incident A waves as being composed of a large fundamental signal and smaller harmonic signals. This approach simplifies the nonlinear mapping described in Equation 3.1 and allows for harmonic superposition. The approximation is illustrated in Figure 3.5. The large signal mapping is nonlinear but the small signal contributions are calculated using harmonic superposition. The general expression is found in Equation 3.2 [10],

$$B_{p,k} = K_{p,k}\left(|A_{11}|\right) P^{k} + \sum_{q,l} G_{p,k;q,l}\left(|A_{11}|\right) P^{k} \mathrm{Re}\left\{A_{k,l}P^{-l}\right\} \\ + \sum_{q,l} H_{p,k;q,l}\left(|A_{11}|\right) P^{k} \mathrm{Im}\left\{A_{k,l}P^{-l}\right\} \quad (3.2)$$

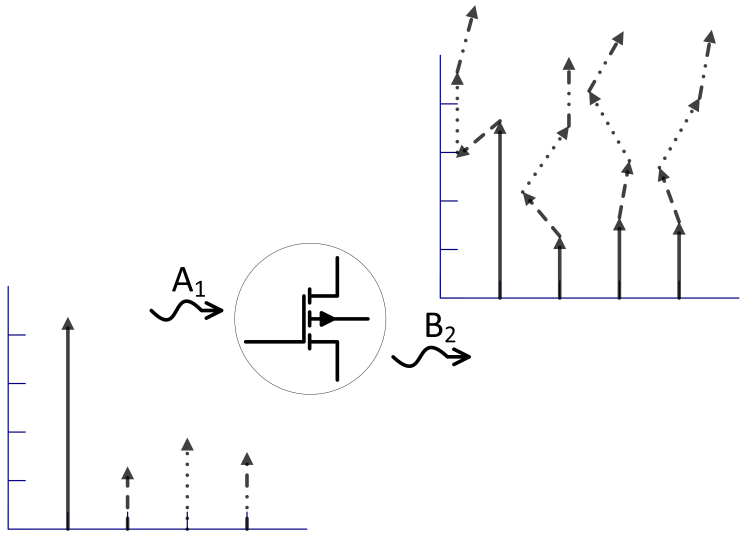

Figure 3.5: Harmonic superposition.

where each contribution is defined by [10]

$$\begin{aligned} K_{p,k}\left(|A_{11}|\right) &= F_{p,k}\left(|A_{1,1}|, 0, ...0\right) \\ G_{p,k;q,l}\left(|A_{11}|\right) &= \left.\frac{\partial F_{p,k}}{\partial \mathrm{Re}\left\{A_{k,l}P^{-l}\right\}}\right|_{|A_{1,1}|,0,...0} \qquad (3.3) \\ H_{p,k;q,l}\left(|A_{11}|\right) &= \left.\frac{\partial F_{p,k}}{\partial \mathrm{Im}\left\{A_{k,l}P^{-l}\right\}}\right|_{|A_{1,1}|,0,...0} \qquad (3.4) \end{aligned}$$

Making use of the following identities, the equation can be simplified further.

$$\begin{aligned} \mathrm{Re}\left\{A_{k,l}P^{-l}\right\} &= \frac{A_{k,l}P^{-l} + \mathrm{conj}(A_{k,l}P^{-l})}{2} \\ \mathrm{Im}\left\{A_{k,l}P^{-l}\right\} &= \frac{A_{k,l}P^{-l} - \mathrm{conj}(A_{k,l}P^{-l})}{2j} \end{aligned}$$

Substituting these identities into Equations 3.3 and 3.4 leads to the following expression [9] :

$$\begin{aligned} B_{p,k} \approx & X_{p,k}^{(FB)}\left(|A_{11}|\right) P^k \\ & + \sum_{\substack{q=1 \\ (q,l)\neq(1,1)}}^{\substack{q=N \\ l=K \\ l=1}} \left[X_{p,k;q,l}^{(S)}\left(|A_{11}|\right) A_{q,l}P^{k-l} + X_{p,k;q,l}^{(T)}\left(|A_{11}|\right) A_{q,l}^{*}P^{k+l}\right] \qquad (3.5) \end{aligned}$$

The S and T terms are defined as [9] :

$$X^{(S)}_{p,k;q,l} = \left.\frac{\partial F_{p,k}}{\partial \left(A_{k,l}P^{-l}\right)}\right|_{|A_{1,1}|,0,\ldots 0} = \left.\frac{\partial F_{p,k}}{\partial A_{k,l}}\right|_{|A_{1,1}|,0,\ldots 0} P^{l} \tag{3.6}$$

$$X^{(T)}_{p,k;q,l} = \left.\frac{\partial F_{p,k}}{\partial \left(A_{k,l}P^{-l}\right)^{*}}\right|_{|A_{1,1}|,0,\ldots 0} = \left.\frac{\partial F_{p,k}}{\partial A^{*}_{k,l}}\right|_{|A_{1,1}|,0,\ldots 0} P^{-l} \tag{3.7}$$

3.3 Analysis and Intuition

X-parameters can be understood from the perspective that they simultaneously describe the large signal and small signal responses and interactions present within the network under test. $X^{(FB)}_{p,k}$ represents the nonlinear response of the large signal at the incident port. This response reflects a scenario in which all scattering ports are matched at all harmonics. This term can produce familiar nonlinear figures of merit related to gain compression and intermodulated distortion. The onset of gain compression can be observed in the measured FB terms shown in Figure 3.6.

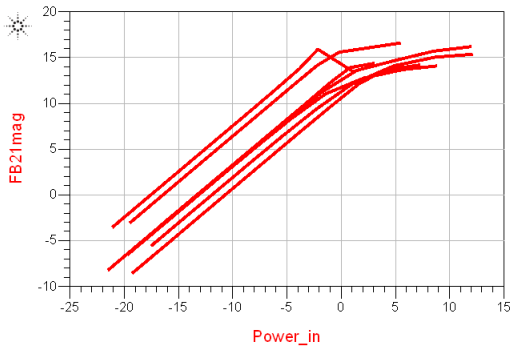

Figure 3.6: Measured FB terms for various frequencies versus RF input power. In this example, the gain compression for the amp under test can be observed.

X-parameters of type S and T come about due to the non-analytic nature of the nonlinear mapping between incident and scattered waves. Essentially, the mapping is a function of both the real and imaginary parts of a harmonic at a given port. As the input power to a network decreases, i.e. the network begins to operate in the small signal regime, the S and T terms will converge

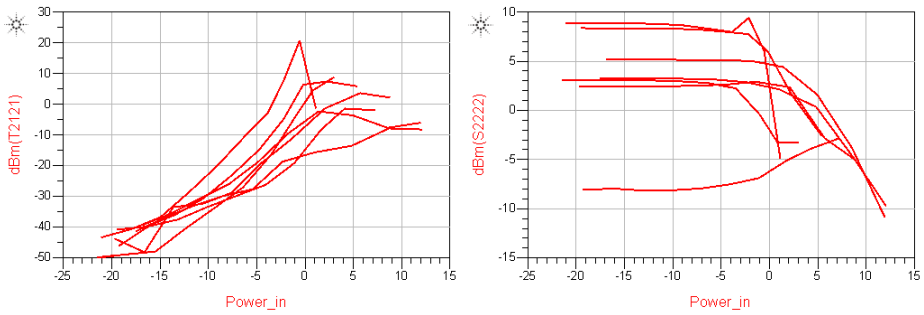

Figure 3.7: Measured X-parameters of type S and T. It can be observed that as input power increases, the S and T terms begin to diverge.

to the familiar behavior associated with S-parameters. As shown in the measured data presented in Figure 3.7, when input power increases, i.e. network behavior becomes more nonlinear, the behaviors of the S and T terms begin to diverge [9]. Alternatively, the S and T terms can be viewed as the sensitivity to mismatch at each harmonic and port.

CHAPTER 4

X-PARAMETER GENERATION AND ANALYSIS USING AGILENT ADS

4.1 Harmonic Balance

Agilent ADS uses the Harmonic Balance (HB) method to generate and analyze X-parameters. Harmonic Balance operates in a way similar to SPICE in that it performs modified nodal analysis in order to solve for circuit currents and voltages except that this analysis is performed in the frequency domain [11]. The algorithm is performed as follows:

1. At each node, linear and nonlinear devices are recognized and separately analyzed.
2. Linear currents are measured in the frequency domain and stored.
3. Nonlinear voltages are measured in the frequency domain and transformed into the time domain.
4. Nonlinear currents are solved for in the time domain and transformed back into the frequency domain.
5. The linear and nonlinear currents are compared at each node. By Kirchoff's Current Law, the currents should sum to zero.
6. If the sum falls within some prescribed error tolerance, the algorithm ends. Otherwise another iteration is performed.

This approach is used to generate X-parameters and to analyze circuits utilizing X-parameter models.

4.2 X-Parameter Model Generation

In order to generate X-parameter models in ADS, the X-parameter source, load and bias elements must be utilized. These are found in the "Simulation-X_Param" palette. The X-parameter source block specifies the port impedance at that port and any input power sweeps desired. The X-parameter load can be used to define the load impedance or any load sweeps desired. The bias block is used to bias active devices and its value can be swept. After performing an X-parameter simulation, a *.ds file will be generated in the directory where the simulation was performed. This file contains the X-parameter model of the DUT. This data file can be used in conjunction with the "data item" block in ADS to perform simulations using this model. An example data item is shown in Figure 4.1. Alternatively, a *.xnp file generated using measured data can be substituted for the simulated model. This file can be generated by measuring a device of interest using a Nonlinear Vector Network Analyzer (NVNA). The simulation process is identical for models generated using simulated or measured data [12].

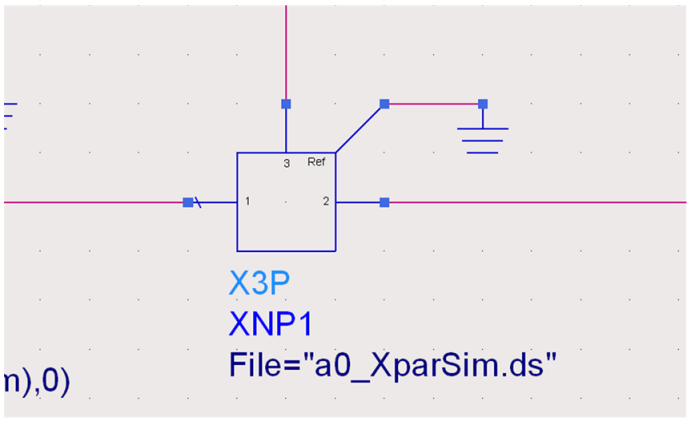

Figure 4.1: Data item in an ADS schematic displaying the directory of X-parameter data set of interest.

Harmonic Balance, as discussed in the previous section, is the simulation environment used to generate X-parameters. In this simulation environment, frequency sweeps, mixing order and harmonic order can be specified. If multiple sources are present and multiple harmonics are generated in the DUT, the mixing order truncates the number of mixing products that are considered in the solution. The harmonic order refers to the number of harmonics of the fundamental frequency under consideration. This number should be

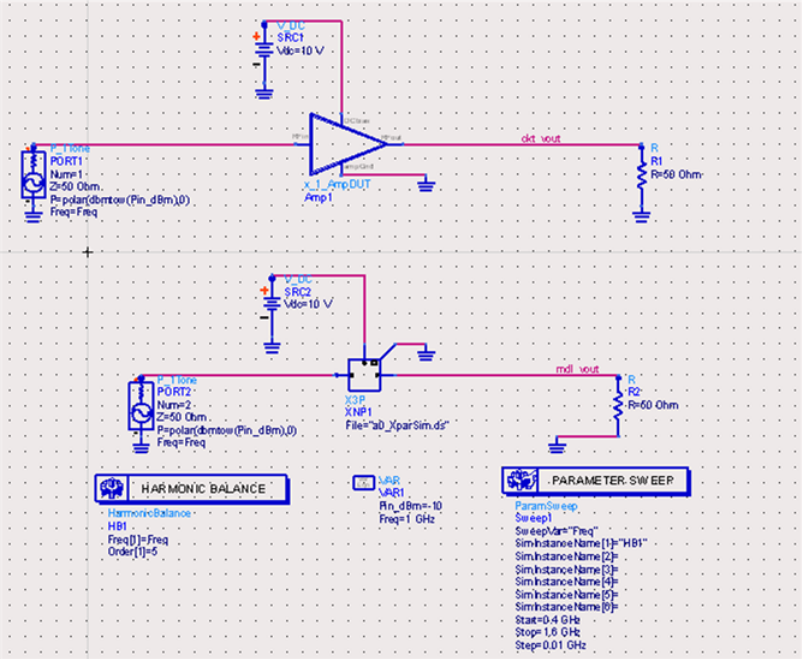

Figure 4.2: ADS schematic showing the X-parameter sources and loads used in the Harmonic Balance simulation environment.

sufficiently large in order to ensure convergence of the HB simulation [11]. For demonstration purposes, an HB simulation of a transistor level circuit was compared to its X-parameter model as shown in Figure 4.2. The magnitude and phase of the first harmonic at the output were compared. As Figure 4.3 shows, the responses are very similar over the frequency range of interest. Deviations in the data begin at 0.5 and 1.5 GHz because the X-parameter model was generated using a smaller frequency range than the example simulation given.

4.3 Figures of Merit

Though X-parameters describe nonlinear behavior from a perspective not traditionally explored, it is still useful to generate standard figures of merit for linearity. This is still possible using X-parameter models. The third order intercept (TOI) of a device can be found using the X-parameter model and the circuit envelope simulation environment. The TOI measurement is a well known method used calculate to what degree a device follows the superposition property of linearity. The circuit envelope method works by

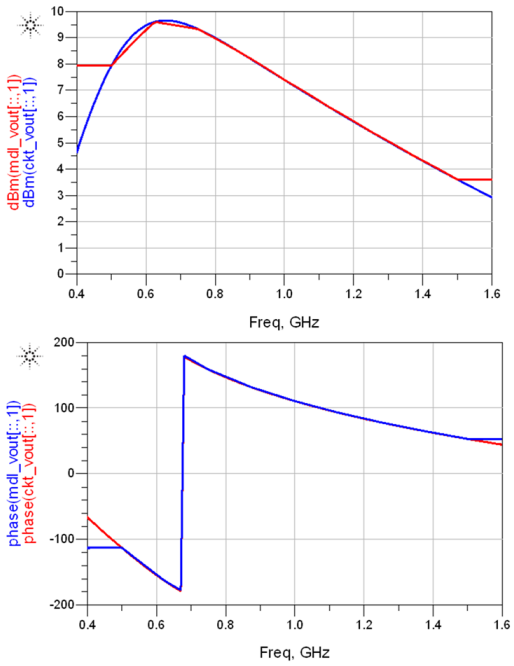

Figure 4.3: Comparison of the first harmonic of a transistor level simulation versus an X-parameter simulation.

sampling the envelope of a modulated RF signal and performing harmonic balance on a given circuit at each time step. Each harmonic is tracked versus time and a fast Fourier transform is performed to give the frequency spectrum of the output of the device [12]. From the resulting frequency spectrum, the TOI can be calculated. As an example, the X-parameters of an amplifier were obtained through measurement using an NVNA. Using the data item described in the Harmonic Balance section of this chapter, the *.xnp file was imported into an ADS schematic. The "message" and "carrier" signals in this case are two tones that are closely spaced in frequency. Similar to the HB simulation, order and mixing order can be specified. The ADS schematic can be viewed in Figure 4.4. The resulting spectrum is found in Figure 4.5. The third order intercept can be calculated using the power of the fundamentals and the intermodulation products [12].

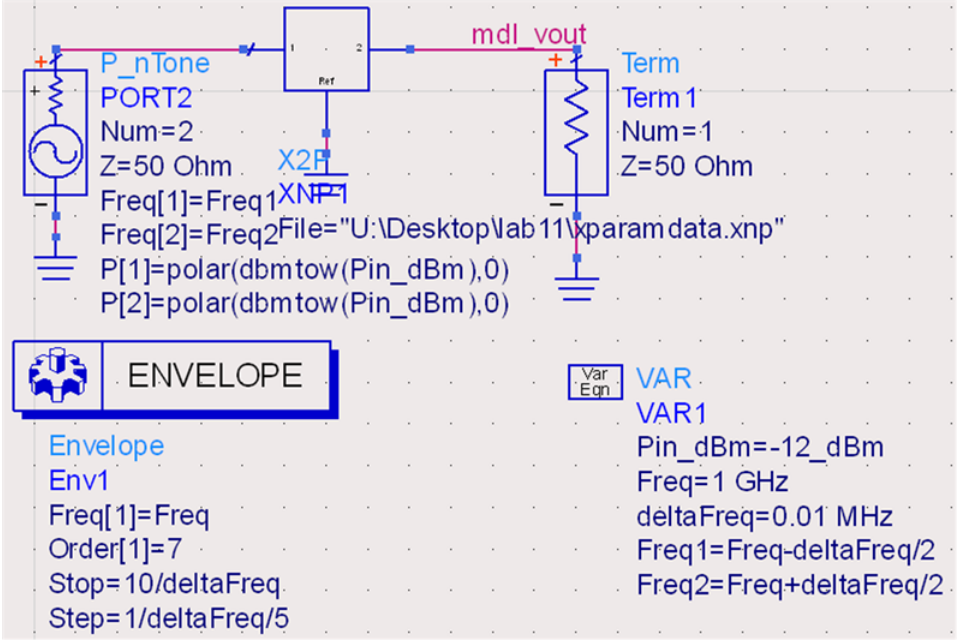

Figure 4.4: The circuit envelope simulation environment used to generate TOI data.

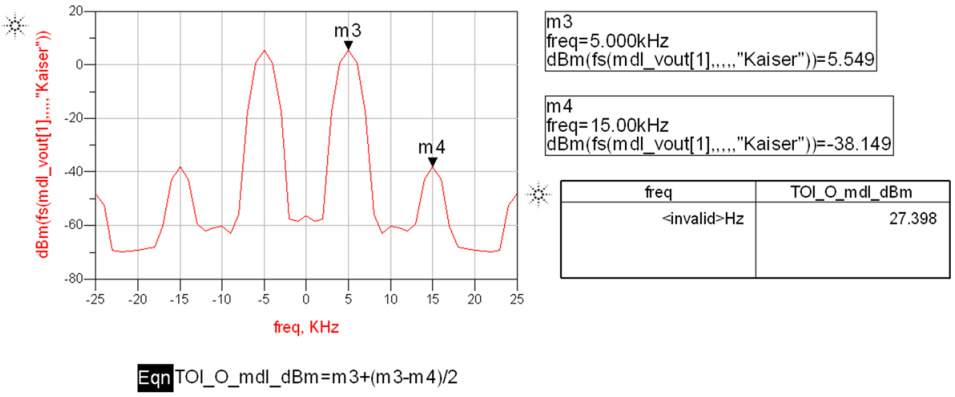

Figure 4.5: Spectrum generated using circuit envelope method to determine TOI.

Another common figure of merit that X-parameters are capable of producing is the 1-dB compression point. This measurement reveals to what degree a device follows the homogeneity principle of linearity. This is most readily produced by plotting the X-parameter of type FB versus input power. The X_{21}^{FB} terms represent the nonlinear mapping at port 2 of the first harmonic of the large signal input with all other ports matched at all harmonics [9]. From Figure 4.6, the onset of gain compression can be observed. This plot is

capable of approximating the 1-dB compression point commonly used when quantifying nonlinear behavior. Figure 4.7 displays the ADS schematic used to produce the FB terms of interest. Depending on the order of the simulation used, other harmonics besides the fundamental can by analyzed and their compression characteristics can be determined.

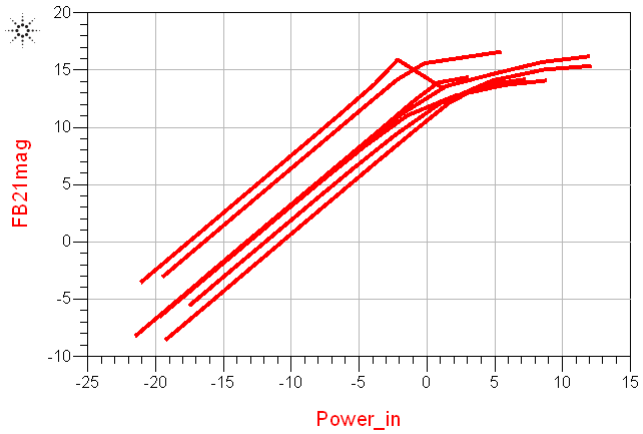

Figure 4.6: Measurement of 1-dB compression for multiple frequencies.

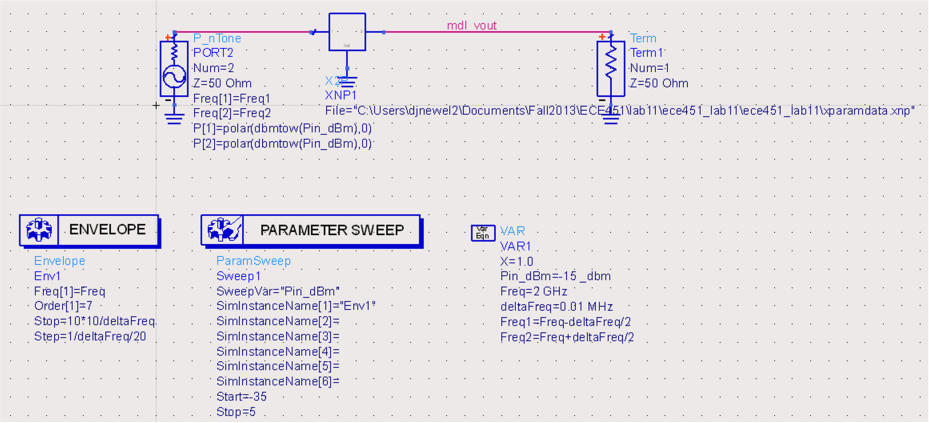

Figure 4.7: ADS Schematic use to plot FB, S and T type X-parameters.

4.4 Cascading X-Parameters

Much of the value of S-parameter models lies in the fact that they can be cascaded together. In this way, system level designers can design accurate models for complex systems while the intellectual property of the circuit level designs is protected. This is made possible by the fact that S-parameters are

used to model linear behavior. By performing the well known S-to-T transformation, cascaded chains can be formed and the internal node associated with two networks in cascade can be absorbed [8].

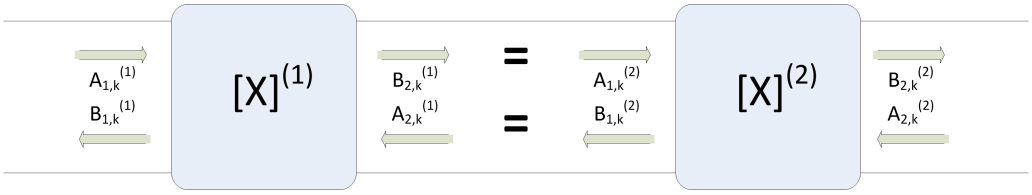

Figure 4.8: Depiction of the X-parameter cascading process. The equality of the scattered and incident waves must be satisfied for all harmonics at the internal node.

Cascading of X-parameters cannot performed in this straightforward fashion. This is due to the input power dependence of X-parameter models. X-parameter blocks can be cascaded in ADS but the internal node, as depicted in Figure 4.8, is maintained and the equations in this internal node are iteratively satisfied [11]. This approach can be observed in the following example. A simple model for a high-speed link consisting of a transmit buffer, microstrip line and receive buffer is used to demonstrate X-parameter cascading. The X-parameters for the buffers were generated using the setup shown in Figure 4.9. Once the X-parameter models were available, the cascaded response of the buffers and the channel was generated using the schematic shown in Figure 4.10. For the purposes of comparison, an X-parameter model was generated for the entire link. This process is displayed in Figure 4.11. As shown in Figure 4.12, the cascaded model behaves similarly to the model generated from the transistor level circuit.

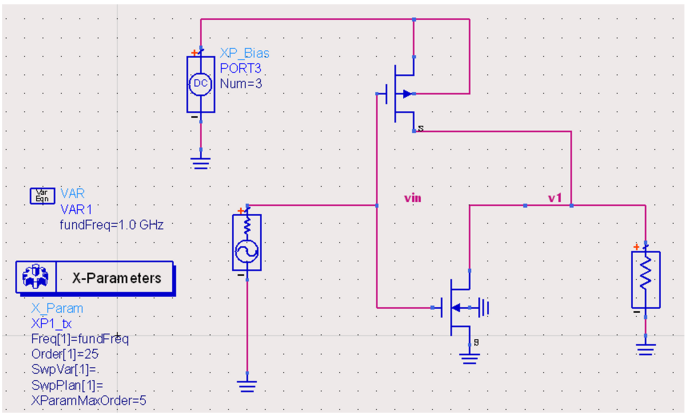

Figure 4.9: X-parameter model generation of the inverter used in the high-speed link.

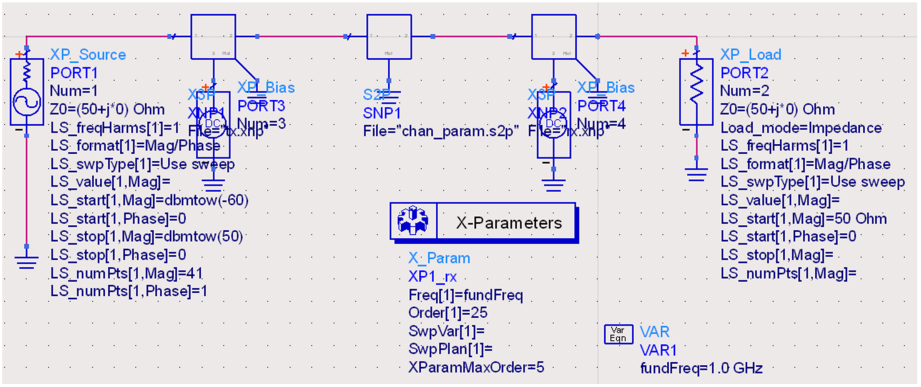

Figure 4.10: Generation of high-speed link model by cascading X-parameter models for the buffers and an S-parameter model for the channel.

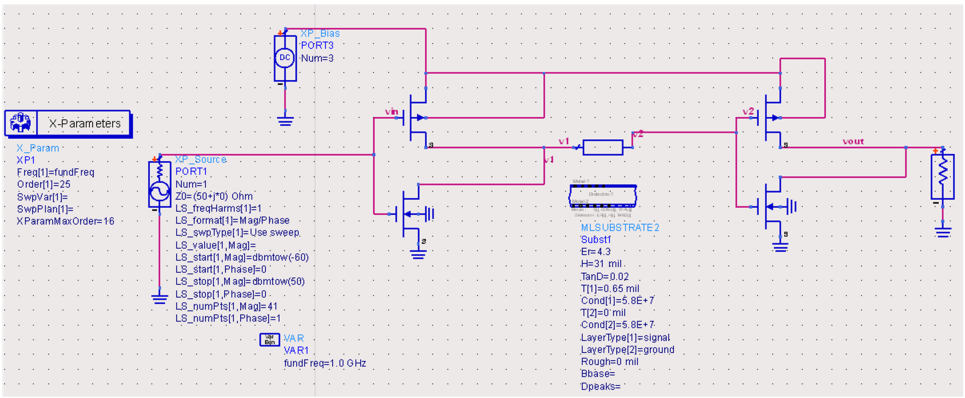

Figure 4.11: Generation of X-parameters for the full, transistor level circuit.

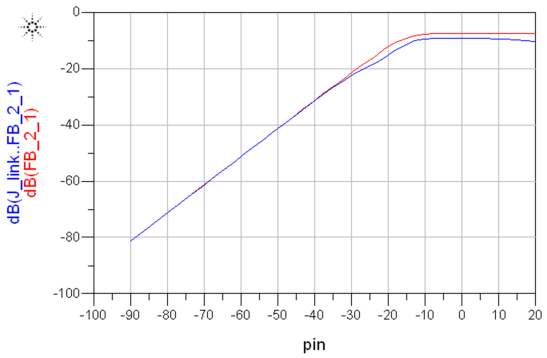

Figure 4.12: Comparison of the response of cascaded X-parameters and direct X-parameter generation of a transistor level circuit. Plotted is the power of the first harmonic at the output versus input power.

CHAPTER 5

TRANSISTOR LEVEL SIMULATION RESULTS

5.1 Equalization Circuits

To counteract the low pass characteristics of channels used in high-speed links, equalization circuits are utilized. An example channel response for a microstrip is presented in Figure 5.1. In most cases, links use both variable gain amplifiers (VGA) and continuous time linear equalizers (CTLE) to shift the corner frequency of the low pass behavior [5]. The ultimate objective of these circuits is to increase the bandwidth of the channel. The VGA is usually used at the transmitter side of a high-speed link. A system level diagram is shown in Figure 5.2. The VGA acts as a pre-emphasis amplifier for the link. A supplied control voltage sets the amplification. The circuit used for this discussion is shown in Figure 5.3 [13]. A PMOS current mirror is used to set the NMOS current source that biases the differential amplifier. Gain is set using an adjustable emitter degeneration [14]. The emitter degeneration resistance is tuned by a parallel arrangement of a fixed resistance and a transistor. The resistance of this arrangement is adjusted by changing the V_{GS} associated with the transistor.

The CTLE circuit analyzed in this chapter can be roughly described as a peaking amp. The frequency response of the circuit is such that a gain peak occurs near the corner frequency of the channel response. The circuit topology can be found in Figure 5.4. The frequency response of the circuit can be approximated by the transfer function [13]:

$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_s C_s}}{\left(s + \frac{1+g_m R_s/2}{R_s C_s}\right)\left(s + \frac{1}{R_D C_p}\right)}$$

In this transfer function, R_S and C_S form the emitter degeneration network, R_D represents the drain resistance and C_P represents the load capacitance.

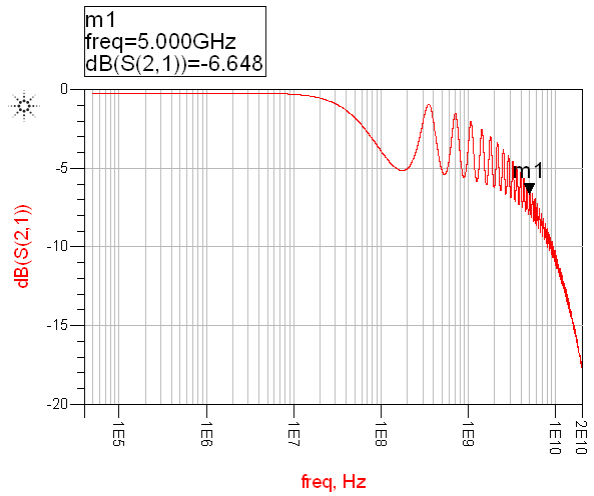

Figure 5.1: Low pass behavior of an example transmission line channel. Substrate: $\epsilon_r = 4.3, h = 31$ mil, $tan\delta = 0.02$.

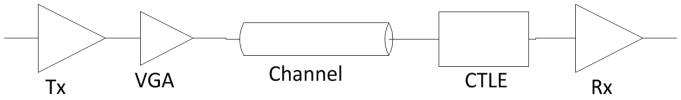

Figure 5.2: Cascading of the VGA, channel and CTLE.

Using this relationship between frequency response and component values, the poles and zeros of the transfer function can be placed where desired. In practice, this equation is only an approximation of the frequency response. Circuit simulation and optimization are the primary methods used to develop these circuits. The design equations do, however, provide a starting point for component selection.

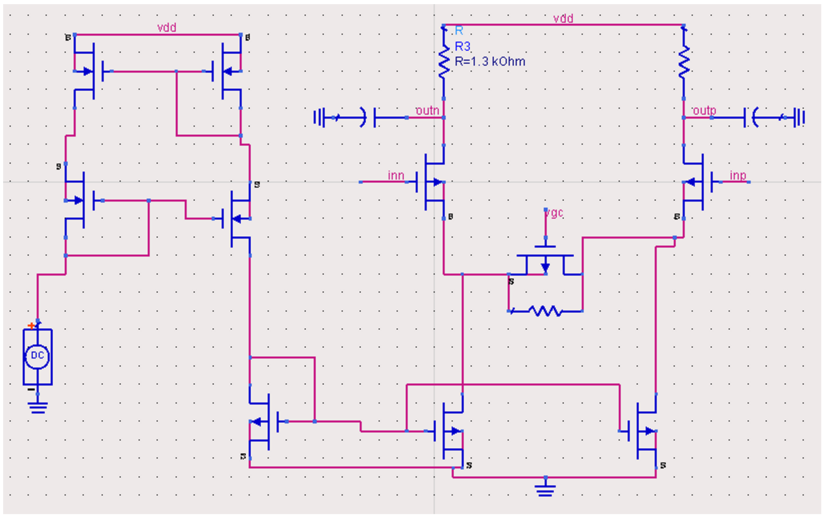

Figure 5.3: Topology of VGA used for modeling.

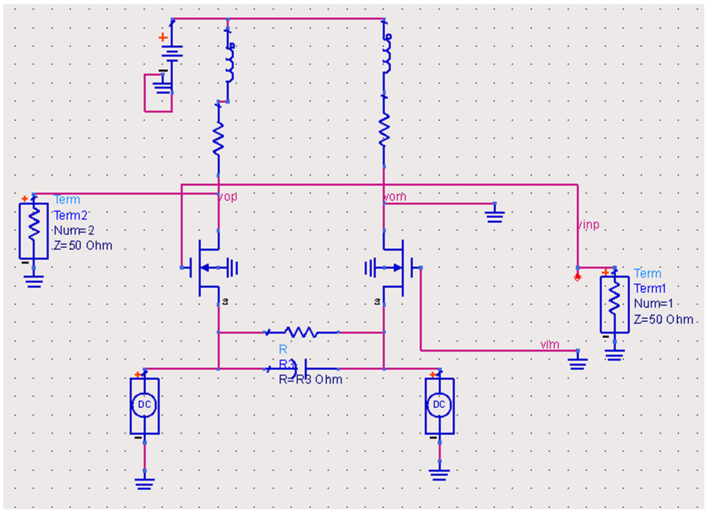

Figure 5.4: Example CTLE (peaking amp) analyzed.

5.2 Circuit Simulation

The VGA X-parameter simulation was performed using a SPICE defined model of 250μm CMOS technology. SPICE transistor models can be imported into ADS using the "Import" feature in the file menu of the schematic view. In the following dialog box, "Netlist" must be specified under the file type. ADS will populate the standard ADS CMOS model with the values specified in the netlist. For the X-parameter simulations of the VGA, both

frequency and input power were swept. Input power was swept from -100 to 25 dBm and frequency was swept from 1 MHz to 1 GHz.

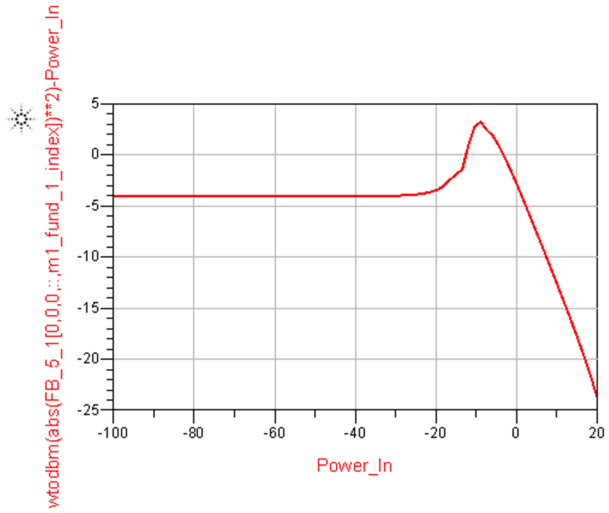

Figure 5.5: Approximate gain profile of VGA using $X_{5,1}^{FB}$ plotted versus input power.

The first parameter analyzed was $X_{5,1}^{FB}$: the power due to the first harmonic at port 5. In this simulation, port 5 can be considered the output port of the amplifier. Figure 5.5 displays a plot of this parameter normalized by the input power versus the input power. As expected, gain compression can be observed as input power increases.

Next, the X-parameters of type S and T were plotted. These parameters were plotted versus frequency for the input power swing stated previously. As shown in chapter 3 of this thesis, S and T parameters diverge in behavior as input power increases. Equivalently, as the network under test begins to operate in a nonlinear fashion, S and T parameters will diverge in behavior. This trend is observable in Figure 5.6 and Figure 5.7.

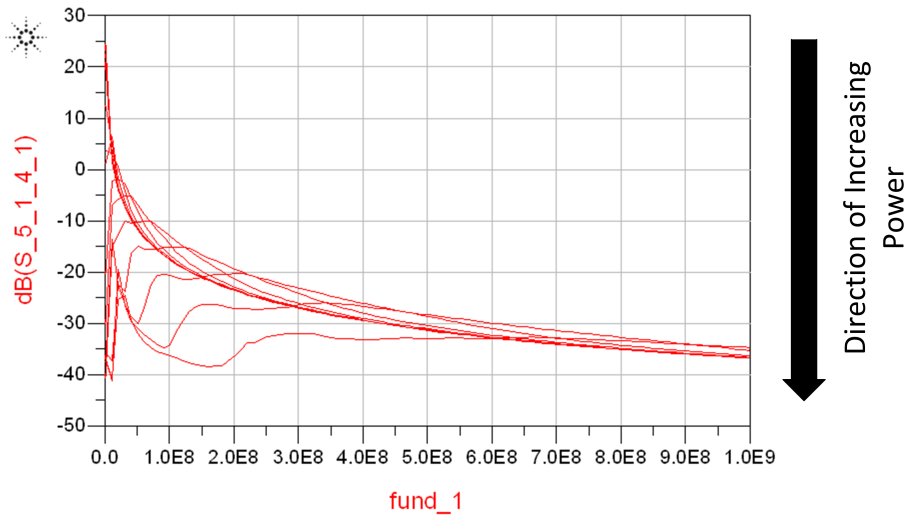

Figure 5.6: X-parameter of type S plotted for various input power levels versus input frequency. The general trend associated with increasing input power is indicated.

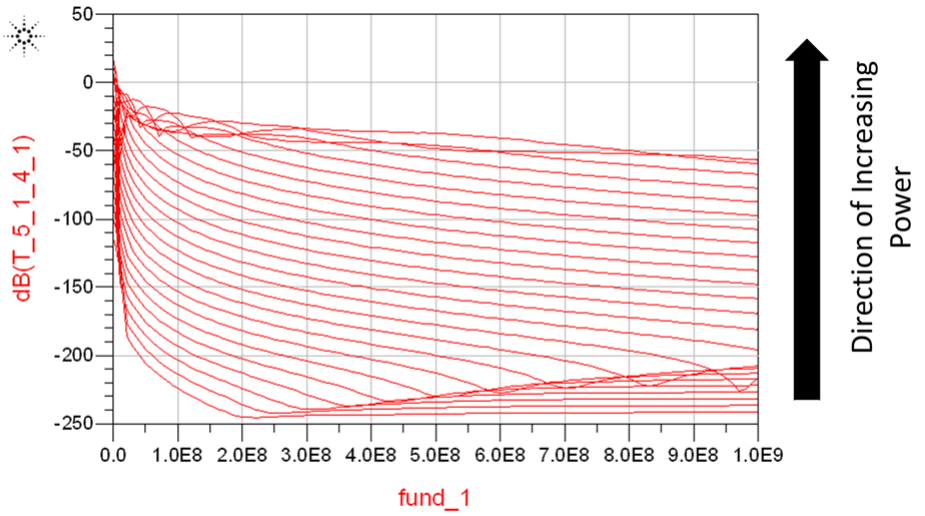

Figure 5.7: X-parameter of type T plotted for various input power levels versus input frequency. The general trend associated with increasing input power is indicated.

The CTLE was analyzed next. The S-parameters for the CTLE were obtain initially to verify operation of the circuit. The transfer coefficient of the cascaded channel and CTLE is displayed in Figure 5.8. The CTLE effectively shifts the corner frequency of the channel from 1 GHz to approximately 4.1 GHz. For the X-parameter simulation, input power was swept from -20 to 40 dBm and the frequency was swept from 500 kHz to 40 GHz.

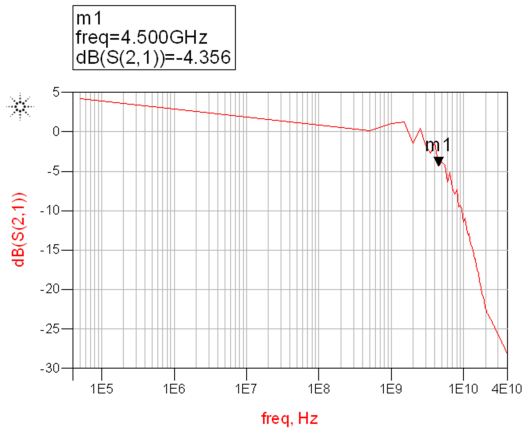

Figure 5.8: Response of cascaded channel and CTLE.

Shown in Figure 5.9, $X^{(S)}_{1,1;4,1}$ is plotted versus the power and frequencies defined previously. In this case, the plot essentially shows how the transmission coefficient of the first harmonic defined between the input and output ports changes with input power and frequency. Shown in Figure 5.10, $X^{(T)}_{1,1;4,1}$ is plotted versus the power and frequencies defined previously. This plot showcases similar information but it is the plot of the transmission coefficient associated with the conjugate of the first harmonic. As expected, as input power increases, the S and T parameters diverge.

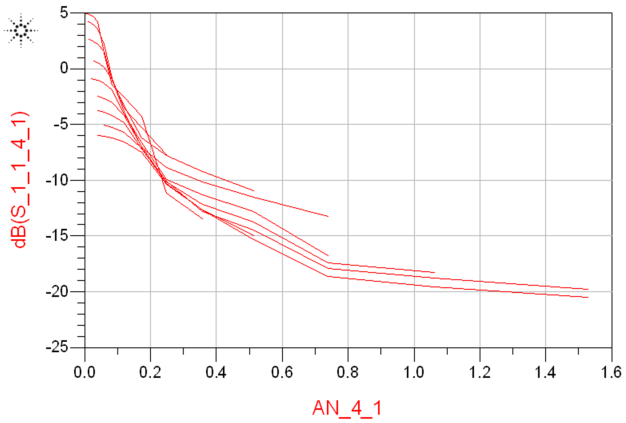

Figure 5.9: $X^{(S)}_{1,1;4,1}$ plotted against input power for various frequencies.

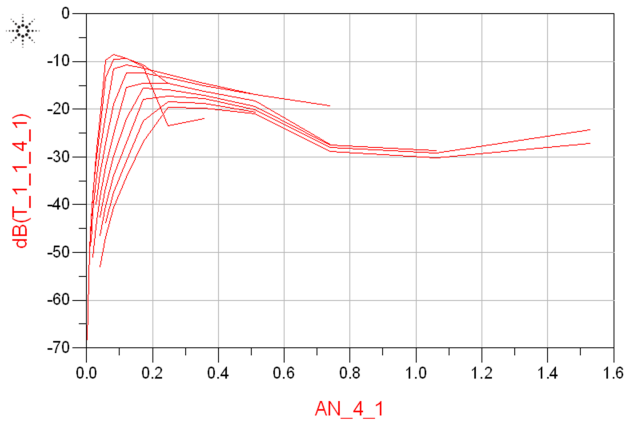

Figure 5.10: $X^{(T)}_{1,1;4,1}$ plotted against input power for various frequencies.

CHAPTER 6

CONCLUSION

6.1 Review

The primary purpose of this thesis was to explore the viability of using X-parameter models to replace well established signal integrity standards. In chapter 1, the basic signal integrity figure of merit called the eye diagram was explored. Its relation to system level properties and electromagnetic effects were discussed. IBIS-AMI was discussed in chapter 2. In this chapter, the basic features of this established standard were discussed and a proposal for an alternative paradigm was made. X-parameters were introduced in chapter 3 and basic theory was presented. In chapter 4, it was demonstrated that Agilent ADS provided convenient tools for X-parameter extraction and analysis. Finally, in chapter 5, X-parameter models were extracted from transistor level equalization circuits commonly used in high-speed links.

6.2 Future Work

X-parameters are native to the frequency domain. As shown in this thesis, X-parameters have the potential to accurately model circuits associated with high-speed links in the frequency domain. The next steps for this analysis are to generate X-parameter models for several other key circuits that make up a high-speed link and perform a full simulation of the cascaded models. A comparison of this model with a frequency domain simulation of a full transistor level high-speed link should validate the accuracy of X-parameters in modeling linear and nonlinear behavior.

Another concept that could be addressed is time domain analysis. Many figures of merit associated with signal integrity are described in the time do-

main. If the S-parameters are known for a circuit, a simple inverse Fourier transform can describe the time domain behavior of a circuit. This is possible because S-parameters are used to model linear behavior. Because X-parameters model nonlinear behavior, this straightforward approach is not possible. Potential avenues for investigation include using Volterra series representations of signals and multidimensional inverse Fourier transformations.

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