MNA STAMPING FOR TRANSIENT CIRCUIT SIMULATION USING SPICE

BY

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THESIS

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ABSTRACT

Simulation is an essential step in the circuit design procedure, helping to verify the behavior of a designed circuit and dramatically reducing the time and effort required for debugging a given design. However, to analyze this behavior, we require an interface between the circuit design and the computer's computational capabilities. This translation can be done in various ways depending on what aspect of the circuit is desired to be modeled (steady-state, transient, etc.). In this thesis, we explore two of these (steady-state MNA formulation and State-Space formulation) as a first step towards transient analysis.

To my family, for their love and support.

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LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor
CCCS	Current-Controlled Current Source
CCVS	Current-Controlled Voltage Source
JFET	Junction-gate Field-Effect Transistor
LIM	Latency Insertion Method
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MNA	Modified Nodal Analysis
SPICE	Simulation Program with Integrated Circuit Emphasis
VCCS	Voltage-Controlled Current Source
VCVS	Voltage-Controlled Voltage Source

CHAPTER 1

INTRODUCTION

1.1 Motivation

Circuit simulation allows a designer to model the behavior of a designed circuit to verify behavior of the design. This is critical to designers to ensure that a designed circuit will behave as intended before being fabricated or built. In order to perform these simulations, we need a way to describe the circuit elements and model their behavior. The circuit can be described using a SPICE netlist, which is a textual way to describe the components of the circuit and their interconnections. This can then be translated (stamped) into a matrix form that describes the behavior of the circuit described. One such formulation is Modified Nodal Analysis (MNA) formulation. The behavior of the circuit can then be modeled based on these matrices. In order for this process to be efficient, however, we need to be able to automatically generate the stamps from the circuit description[1]. This process is discussed in depth in this thesis.

1.2 Outline

- Chapter 1 introduces the motivation behind this thesis.
- Chapter 2 describes the SPICE program and how to use netlists to describe a given circuit.
- Chapter 3 explains the MNA formulation, focusing on the steady-state analysis.
- Chapter 4 explains the State-Space formulation.

[1]Please contact the author for the Python code at visheshverma22@gmail.com

- Chapter 5 discusses the implementation of parsing the netlist and collecting basic circuit information.
- Chapter 6 describes the generation of the stamp of the steady-state MNA formulation.
- Chapter 7 describes the generation of the stamp of the State-Space formulation.
- Chapter 8 concludes the thesis with a summary
- Chapter 9 discusses future extensions on the described work.

CHAPTER 2

WHAT IS SPICE?

2.1 The SPICE Program

The Simulation Program with Integrated Circuit Emphasis, more commonly referred to as by its abbreviation "SPICE," is a circuit simulation program commonly used in both academia and industry to model behavior of a circuit. All circuits, however, can only include certain circuit elements that are supported: resistors, inductors, capacitors, independent voltage sources, independent current sources, voltage-controlled voltage sources, voltage-controlled current sources, current-controlled voltage sources, current-controlled current sources, transmission lines, switches, diodes, MOSFETs, BJTs, JFETs, and MESFETs. Any additional elements that a user wants to implement must be modeled using the other existing circuit elements. Because of its widespread adoption, many companies have also produced an external SPICE tool including models of their products, such as LTspice, Pspice, and HSPICE. SPICE also currently supports three types of analyses: DC, AC, and transient.

2.2 SPICE Netlists

A netlist is a textual description of a circuit. It describes the circuit by listing each component and which nodes it is connected to along with any additional information needed to describe the behavior of the circuit element. Each type of component listed previously has a specific code associated with it to identify it. The descriptions of each of the types of circuit components of a SPICE netlist are given below in addition to a few additional relevant instructions to this study. The full netlist is a combination of the elements

described below. The lines should include all elements in the circuit and their connections in order to be a complete netlist [1], [2].

2.2.1 Resistors

The general SPICE netlist representation of a resistor appears as below, followed by an example resistor in Figure 2.1[1] named R1 with resistance 10 kΩ connected between nodes a and b along with the corresponding SPICE netlist line for resistor R1.

Rxxxxxxx Node1 Node2 Resistance

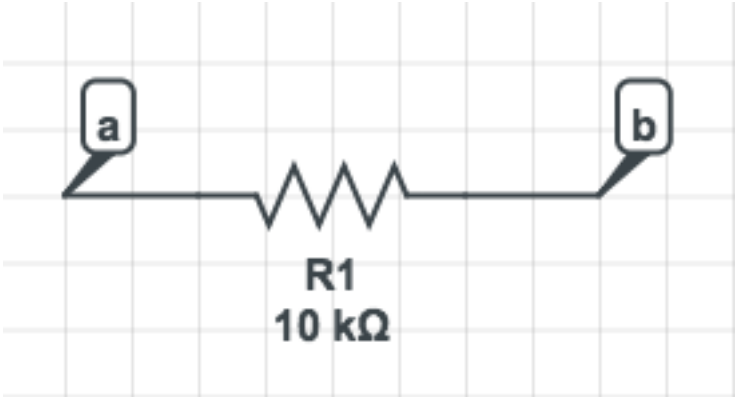

Figure 2.1: Resistor Schematic

R1 a b 10k

The node listed first of the two (Node1) is considered the positive terminal of the resistor and the second listed node (Node2) is considered the negative terminal. The units of the resistance are assumed to be ohms.

2.2.2 Inductors

The general SPICE netlist representation of an inductor appears as below, followed by an example inductor in Figure 2.2 named L5 with inductance 45 nH connected between nodes 1 and 2 along with the corresponding SPICE netlist line for inductor L5.

[1] All schematics in this thesis were generated using CircuitLab

Lxxxxxxx Node1 Node2 Inductance

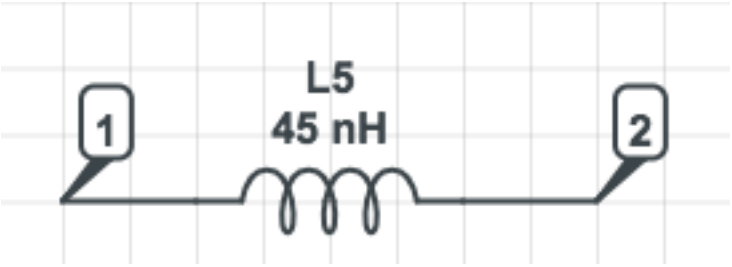

Figure 2.2: Inductor Schematic
L5 1 2 45n

The node listed first of the two (Node1) is considered the positive terminal of the inductor and the second listed node (Node2) is considered the negative terminal. The current through the inductor is defined to go from Node1 to Node2. The units of the inductance are assumed to be henries.

2.2.3 Capacitor

The general SPICE netlist representation of a capacitor appears as below, followed by an example capacitor in Figure 2.3 named C_filter with capacitance 22 pF connected between nodes ckt_out and filt_out along with the corresponding SPICE netlist line for capacitor C_filter.

Cxxxxxxx Node1 Node2 Capacitance

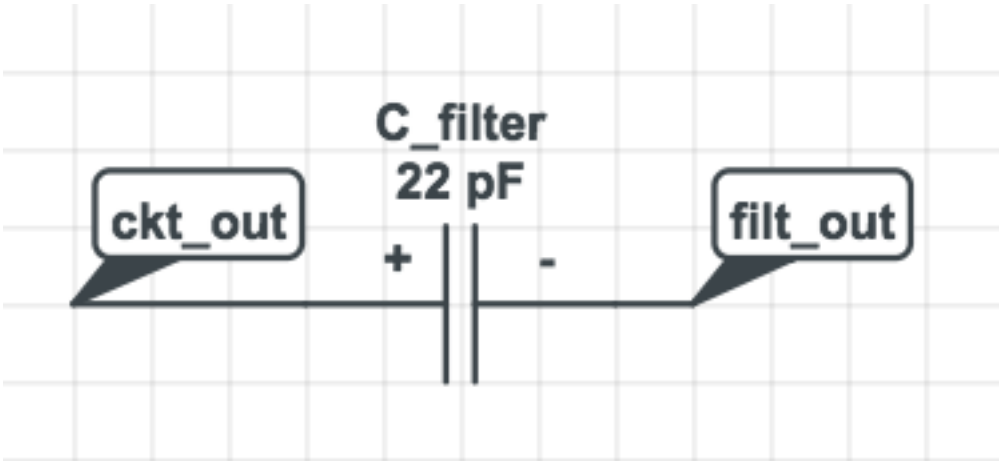

Figure 2.3: Capacitor Schematic
C_filter ckt_out filt_out 22p

The node listed first of the two (Node1) is considered the positive terminal of the capacitor and the second listed node (Node2) is considered the negative terminal. The units of the capacitance are assumed to be farads.

2.2.4 Independent Voltage Source

The general SPICE netlist representation of an independent voltage source appears as below, followed by an example voltage source in Figure 2.4 named Vbias with voltage 5 V connected between nodes VDC and GND along with the corresponding SPICE netlist line for voltage source Vbias.

Vxxxxxxx Node1 Node2 DC_Voltage

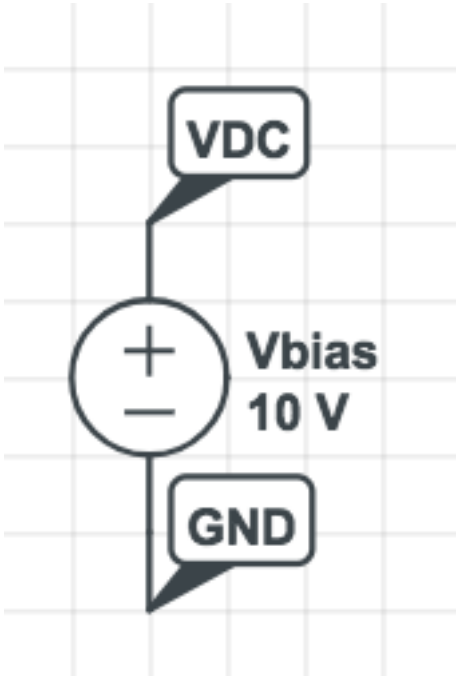

Figure 2.4: Independent Voltage Source Schematic
Vbias VDC GND 10

The node listed first of the two (Node1) is considered the positive terminal of the voltage source and the second listed node (Node2) is considered the negative terminal. The units of the voltage across the source are assumed to be volts.

2.2.5 Independent Current Source

The general SPICE netlist representation of an independent current source appears as below, followed by an example current source in Figure 2.5 named Isource with current 10 mA connected between nodes input and ground along with the corresponding SPICE netlist line for current source Isrc.

Ixxxxxxx Node1 Node2 DC_Current

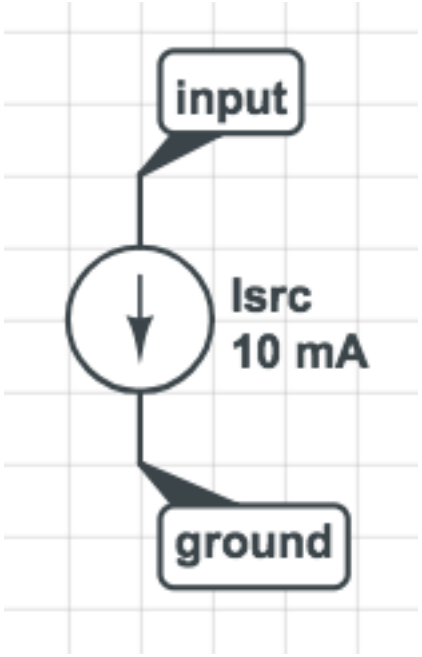

Figure 2.5: Independent Current Source Schematic
Isrc input ground 10m

The node listed first of the two (Node1) is considered the positive terminal of the voltage source and the second listed node (Node2) is considered the negative terminal. The units of the voltage across the source are assumed to be volts.

2.2.6 Current-Controlled Current Source

The general SPICE netlist representation of a current-controlled current source appears as below, followed by an example current-controlled current source in Figure 2.6 named FCCCS connected between nodes iout and iref that provides gain 2 from the current through the independent voltage

source imeas along with the corresponding SPICE netlist line for the current-controlled current source FCCCS.

Fxxxxxxx Node1 Node2 VSource0 Gain

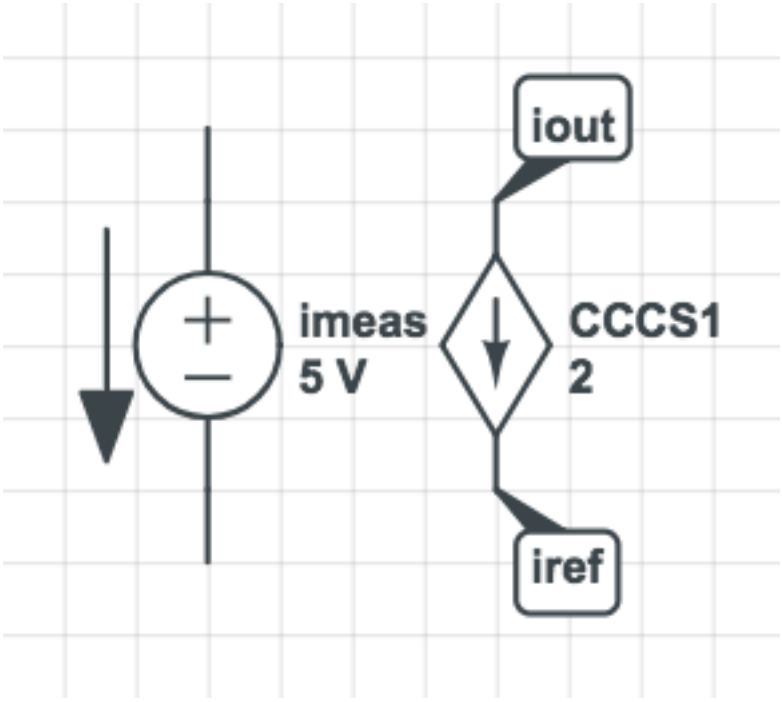

Figure 2.6: CCCS Schematic
FCCCS iout iref imeas 2

The first listed node (Node1) is considered the positive terminal of the dependent current source and the second listed node (Node2) is considered the negative terminal. Therefore, current flows from Node2 to Node1. VSource0 is a voltage source in the place where the current reference is measured. If there is not a voltage source at this location in the circuit already, it is easy to add a 0 V voltage source in series in the location where the current is to be measured and use that as the reference without affecting the behavior of the rest of the circuit.

2.2.7 Voltage-Controlled Current Source

The general SPICE netlist representation of a voltage-controlled current source appears as below, followed by an example voltage-controlled current source in Figure 2.7 named GVCCS connected between nodes Ipos and Ineg

that provides gain 5 mA/V from the voltage between nodes Vneg and Vpos along with the corresponding SPICE netlist line for the voltage-controlled current source GVCCS.

Gxxxxxxx Node1 Node2 Node3 Node4 Gain

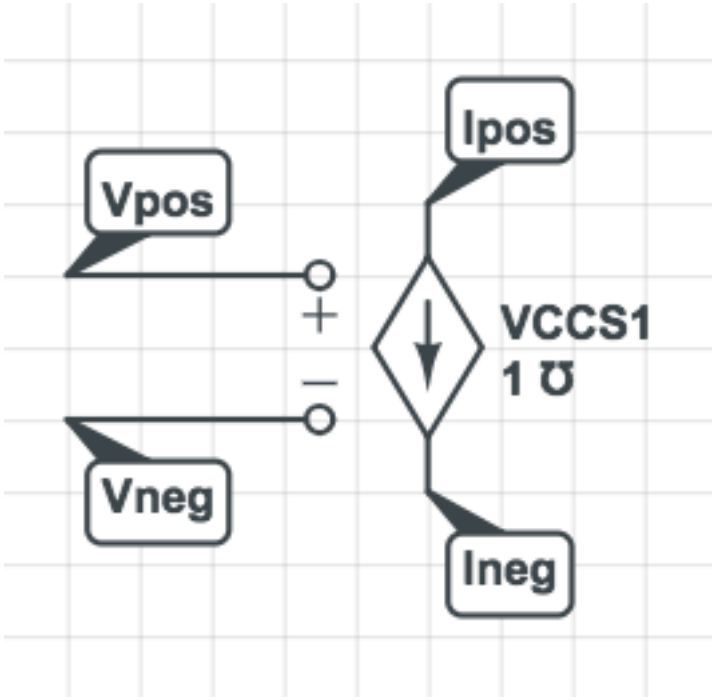

Figure 2.7: VCCS Schematic
GVCCS Vpos Vneg Ipos Ineg 5m

The first listed node (Node1) is considered the positive terminal of the measured voltage and the second listed node (Node2) is considered the negative terminal. The current flows from the third node (Node3) to the fourth node (Node4). The units of the gain across the source are assumed to be amps/volt.

2.2.8 Current-Controlled Voltage Source

The general SPICE netlist representation of a current-controlled voltage source appears as below, followed by an example current-controlled voltage source in Figure 2.8 named HCCVS connected between nodes Vout and Vref that provides gain $2x10^6$ from the current through the independent voltage

source imeas along with the corresponding SPICE netlist line for the current-controlled voltage source HCCVS.

Hxxxxxxx Node1 Node2 VSource0 Gain

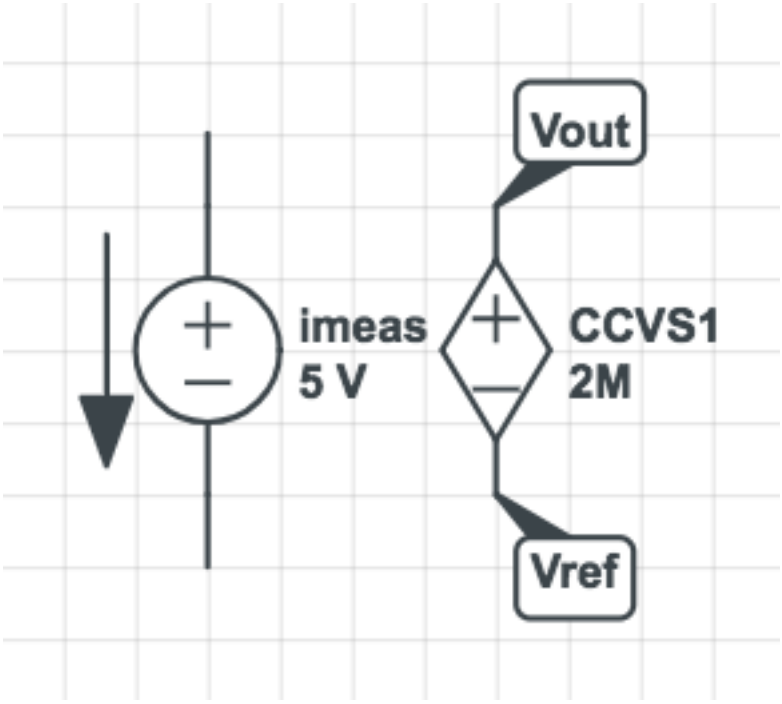

Figure 2.8: CCVS Schematic
HCCVS Vout Vref imeas 2M

The first listed node (Node1) is considered the positive terminal of the dependent voltage source and the second listed node (Node2) is considered the negative terminal. VSource0 is a voltage source in the place where the current reference is measured. If there is not a voltage source at this location in the circuit already, it is easy to add a 0 V voltage source in series in the location where the current is to be measured and use that as the reference without affecting the behavior of the rest of the circuit. The units of the gain across the source are assumed to be volts/amp.

2.2.9 Voltage-Controlled Voltage Source

The general SPICE netlist representation of a voltage-controlled voltage source appears as below, followed by an example voltage-controlled current

source in Figure 2.9 named EVCVS connected between nodes Vref+ and Vref- that provides gain 2 V/V from the voltage between nodes Vneg and Vpos along with the corresponding SPICE netlist line for the voltage-controlled voltage source EVCVS.

Exxxxxxx Node1 Node2 Node3 Node4 Gain

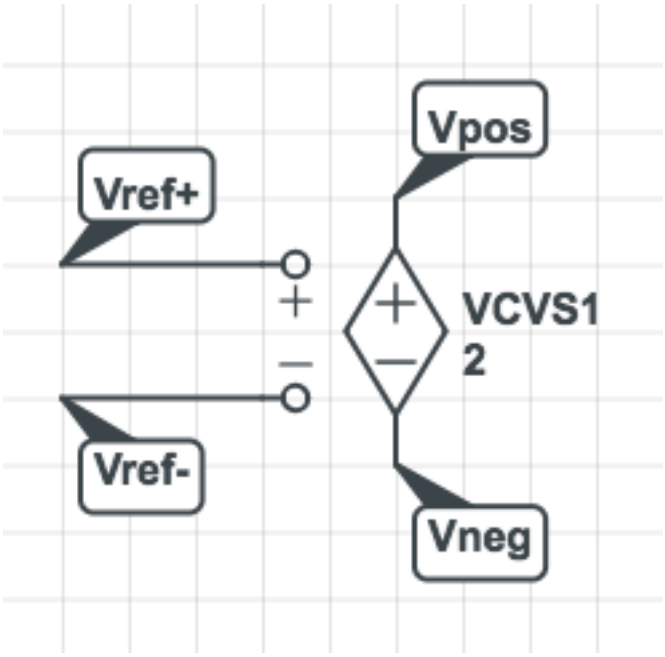

Figure 2.9: VCVS Schematic
EVCVS Vpos Vneg Vref+ Vref- 2

The first listed node (Node1) is considered the positive terminal of the measured voltage and the second listed node (Node2) is considered the negative terminal. The output dependent voltage source has a positive terminal at the third node (Node3) and negative terminal at the fourth node (Node4). The units of the gain across the source are assumed to be volts/volt.

2.2.10 Subcircuit

The SPICE netlist representation of a subcircuit requires two parts: the subcircuit definition and the invocation of the subcircuit. The subcircuit definition starts with the command .subckt, followed by the name of the subcircuit (sub_name) and a list of all the nodes to connect to the rest of the

circuit. The number of externally connected nodes can be arbitrarily long. This line is then followed by any collection of the previously listed circuit elements that form the internal components of the subcircuit. The subcircuit definition is considered terminated at the line .ends followed by the name of the subcircuit sub_name. The subcircuit definition follows the format below:

.subckt sub_name node1 node2 . . . nodeN ⋮.ends sub_name

To invoke the previously defined subcircuit, the following netlist line is used:

Xxxxxxxx node1 node2 . . . nodeN sub_name

The list of nodes describes the nodes in the circuit that connect to the corresponding subcircuit node listed previously. The last element is the subcircuit name sub_name that refers to which subcircuit definition this instance of a subcircuit should follow. Below is an example subcircuit definition and invocation for a low pass filter subcircuit.

```
.subckt lowpass input vref output
Rin input N1 50
Cshunt N1 vref 15p
Lseries N1 output 8.2n
.ends lowpass
XLPF Port1 GND Port2 lowpass
```

2.2.11 End of Netlist

The Ends line, as the name implies, signifies the end of a section. It can be used as described previously to end a subcircuit definition. It is also used to end a netlist. In this second case, any lines that come after the Ends line is ignored entirely. This can be in either lowercase or capital letters, as below.

```
.ends
.ENDS
```

2.2.12 Comments

Comments are lines in the netlist that are only included in the file for readability of the netlist. They are not part of the circuit implementation, though they typically help anyone who has to read the netlist to understand something that may not be intuitive just reading the netlist alone.

CHAPTER 3

MNA FORMULATION

Modified Nodal Analysis (MNA) formulation is a way of expressing the equations governing the behavior of a given circuit. Specifically, the MNA formulation describes the circuit according to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL). These equations are expressed in the form of a matrix to allow for easier and more efficient computation, usually by a computer. The MNA formulation follows the form shown in Equation 3.1:

$$[\mathbf{A}] \cdot [\mathbf{x}] = [\mathbf{z}] \tag{3.1}$$

For this analysis, we will focus on just the most commonly used components: resistors, inductors, capacitors, independent current sources, and independent voltage sources. Here we will describe which components affect which parts of Equation 3.1, and we will describe the exact details in Chapter 6, where the implementation is detailed.

The vector $\mathbf{x}$ is the list of our unknown parameters (voltages and currents) in the circuit. We describe $\mathbf{x}$ in terms of two vectors $\mathbf{v}_x$ and $\mathbf{i}_x$ as in Equation 3.2:

$$[\mathbf{x}] = \begin{bmatrix} \mathbf{v}_x \\ \mathbf{i}_x \end{bmatrix} \tag{3.2}$$

The vector $\mathbf{v}_x$ lists all the node voltages in the circuit with the exception of whichever node is defined as the Ground node. The Ground node does not appear in the MNA formulation matrices. The vector $\mathbf{i}_x$ lists all the currents through voltage sources and inductors. These two concatenate to form the vector $\mathbf{x}$.

The matrix $\mathbf{A}$ describes the relationships between the node voltages and currents in the circuit. We can divide this matrix into four sub-matrices that we call $\mathbf{G}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{L}$ according to Equation 3.3:

$$[\mathbf{A}] = \begin{bmatrix} \mathbf{G} & \mathbf{B} \\ \mathbf{C} & \mathbf{L} \end{bmatrix} \tag{3.3}$$

Matrix **G** is a square matrix with size equal to the number of node voltages in the circuit. Circuit elements that have a conductance will have this value described here. The exact details of how these conductances are calculated and placed in the matrix are described in Chapter 6.

Matrix **B** contains information about voltage sources including independent sources, dependent sources, and inductors. Each component adds only ones, zeros, or negative ones to the elements in the matrix. The implementation is described in Chapter 6.

Matrix **C** also contains information about voltage sources including independent sources, dependent sources, and inductors. It is simply the transpose of the **B** matrix.

Matrix **L** contains information about currents. This includes information about both inductors and some dependent sources. Since dependent sources were not implemented for this part of the project, non-zero values only appear in this matrix when we have an inductor in the circuit.

The vector **z** lists all the known currents and voltages in the circuit. Similarly to the **x** vector, this can be divided into $\mathbf{i}_z$ and $\mathbf{v}_z$ vectors, as shown below in Equation 3.4. Vector $\mathbf{i}_z$ contains the currents in and out of nodes due to an independent current source, and vector $\mathbf{v}_z$ contains the voltages created by the independent voltage sources. These primarily come from independent current and voltage sources, whereas most other components do not affect this vector [3]. The implementation is described in Chapter 6.

$$[\mathbf{z}] = \begin{bmatrix} \mathbf{v}_z \\ \mathbf{i}_z \end{bmatrix} \tag{3.4}$$

CHAPTER 4

STATE-SPACE FORMULATION

The State-Space formulation describes the time-domain behavior of a circuit in the form of a first-order ordinary differential equation. The general expression for the State-Space formulation follows Equations 4.1 and 4.2 as follows:

$$\mathbf{C} \cdot \mathbf{x}'_n = -\mathbf{G} \cdot \mathbf{x}_n + \mathbf{B} \cdot \mathbf{u} \tag{4.1}$$

$$\mathbf{y} = \mathbf{L}^T \cdot \mathbf{x}_n \tag{4.2}$$

The vector $\mathbf{x}_n$ is the list of our unknown parameters (voltages and currents) in the circuit. We describe $\mathbf{x}_n$ in terms of two vectors $\mathbf{v}$ and $\mathbf{i}$ as in Equation 4.3:

$$\mathbf{x}_n = \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} \tag{4.3}$$

The vector $\mathbf{v}$ lists all the node voltages in the circuit with the exception of whichever node is defined as the Ground node. The Ground node does not appear in the Steady-State formulation matrices. The vector $\mathbf{i}$ lists all the currents through voltage sources and inductors. These two concatenate to form the vector $\mathbf{x}_n$. $\mathbf{x}'_n$ is the derivative of $\mathbf{x}_n$.

The $\mathbf{C}$ matrix contains elements where the unknown currents and voltages are related to the derivatives of the node voltages and currents respectively.

The $\mathbf{G}$ matrix contains element relationships between the node voltages and currents in the circuit that are directly related to each other. This is very similar to the $\mathbf{A}$ matrix from the Steady-State MNA formulation.

The $\mathbf{B}$ matrix combined with the $\mathbf{u}$ vector is to include known current and voltage sources. The $\mathbf{u}$ vector contains the values of independent voltage and current sources, and the $\mathbf{B}$ matrix notates which nodes in the independent

voltage or current source are the positive and negative terminals.

Similar to the combination of **L** matrix and **u** vector, the **L** matrix and **y** vector combine to describe the unknown current and voltage sources. The **y** vector contains the unknown currents and voltages through the independent sources, while the **L** matrix notates which nodes in the independent voltage or current source are the positive and negative terminals.

From the matrices defined above, we can also generate a matrix **A** as described in Equation 4.4:

$$\mathbf{A} = -\mathbf{G}^{-1} \cdot \mathbf{C} \tag{4.4}$$

The inverses of the eigenvalues of matrix **A** provide the poles of the admittance function [4] defined in Equation 4.5:

$$\mathbf{Y(s)} = \mathbf{L}^T \cdot (\mathbf{G} + s\mathbf{C})^{-1} \cdot \mathbf{B} \tag{4.5}$$

For this analysis, we will expand the base of components that we consider in order to include additional common circuit elements: resistors, inductors, capacitors, independent current sources, independent voltage sources, current-controlled current sources (CCCS), current-controlled voltage sources (CCVS), voltage-controlled current sources (VCCS), and voltage-controlled voltage sources (VCVS). The implementations of these are discussed in Chapter 7.

CHAPTER 5

NETLIST PARSING IMPLEMENTATION

No matter which method we plan to use to analyze the behavior of a given circuit, the starting point for programmatically representing the solution in matrices is the same: interpreting the netlist. For the purpose of simplicity, the netlist parsing was divided into two passes: the first pass collects information about the circuit as a whole to be able to generate matrices, and the second pass fills in these matrices to reflect the properties of the circuit.

5.1 First Pass

The goal of the first pass is to determine basic information about the circuit so that the appropriate matrices can be created. First it is determined whether or not the line contains relevant information to the circuit. Any blank lines, comments (denoted by lines starting in ; or *), or lines that come after a .ends command can be ignored as they are not part of the circuit.

Once it has been determined that the line contains a valid circuit component, we then determine what component this might be. Based on the component, we also collect additional information about the circuit that can be determined from this, such as the nodes in the circuit to which the component is connected. Each of the components and its relevant properties is described below.

5.1.1 Resistor

The SPICE representation of a resistor appears as:

Rxxxxxxx Node1 Node2 Resistance

In the first pass for both Steady-State MNA and State-Space analysis, we only need to collect the names of the nodes and add them to our list of nodes in the circuit if it is not already included.

5.1.2 Inductor

The SPICE representation of an inductor appears as:

Lxxxxxxx Node1 Node2 Inductance

In the first pass for both Steady-State MNA and State-Space analysis, we collect the names of the nodes and add them to our list of nodes in the circuit if it is not already included. In the Steady-State MNA representation, we also keep track of the number of inductors in the circuit. In the State-Space analysis, we add an additional unknown current to the $\mathbf{x}$ vector for the current through the inductor.

5.1.3 Capacitor

The SPICE representation of a capacitor appears as:

Cxxxxxxx Node1 Node2 Capacitance

In the first pass for both Steady-State MNA and State-Space analysis, we only need to collect the names of the nodes and add them to our list of nodes in the circuit if it is not already included.

5.1.4 Independent Voltage Source

The SPICE representation of an independent voltage source appears as:

Vxxxxxxx Node1 Node2 DC_Voltage

In the first pass for both Steady-State MNA and State-Space analysis, we collect the names of the nodes and add them to our list of nodes in the circuit

if it is not already included. In the Steady-State MNA representation, we also need to increment the voltage source counter and add the known voltage to the $\mathbf{z}$ vector. In the State-Space analysis, we also keep track of the number of sources encountered in addition to adding the unknown current through the source to both vectors $\mathbf{x}_i$ and $\mathbf{y}$ and adding the source to a dictionary of voltage sources. This dictionary is necessary later for any potential dependent sources we come across later.

5.1.5 Independent Current Source

The SPICE representation of an independent current source appears as:

Ixxxxxxx Node1 Node2 DC_Current

In the first pass for both Steady-State MNA and State-Space analysis, we collect the names of the nodes and add them to our list of nodes in the circuit if it is not already included. In the Steady-State MNA representation, we also add the known currents into node Node2 and out of node Node1 both to the $\mathbf{z}$ vector. In the State-Space analysis, we also note the current through the source as a part of the $\mathbf{x}_i$vector and the unknown voltage across the current source to the $\mathbf{y}$ vector. Finally, the source counter needs to be incremented.

5.1.6 Current-Controlled Current Source

The SPICE representation of a current-controlled current source (CCCS) appears as:

Fxxxxxxx Node1 Node2 VSource0 Gain

In the first pass for State-Space analysis, we collect the names of the nodes and add them to our list of nodes in the circuit if it is not already included. In addition, we add two unknown currents due to the dependent source: one on the input side and one on the output side. Because of this, we increase our source counter by two. The Steady-State MNA analysis implementation did not include current-controlled current sources but could easily be added

if desired.

5.1.7 Voltage-Controlled Current Source

The SPICE representation of a voltage-controlled current source (VCCS) appears as:

Gxxxxxxx Node1 Node2 Node3 Node4 Gain

In the first pass for State-Space analysis, we collect the names of each of the four nodes and add them to our list of nodes in the circuit if it is not already included. Since it is a source, we also increment our source counter and add the output (current source) side as a new unknown current to the vector $\mathbf{x}_i$. The Steady-State MNA analysis implementation did not include voltage-controlled current sources but could easily be added if desired.

5.1.8 Current-Controlled Voltage Source

The SPICE representation of a current-controlled voltage source (CCVS) appears as:

Hxxxxxxx Node1 Node2 VSource0 Gain

In the first pass for State-Space analysis, we collect the names of the nodes and add them to our list of nodes in the circuit if it is not already included. In addition, we add an unknown current due to the output current source. We do not need to add the input reference voltage source as this is already included from other aspects of the analysis. Because of this, we increase our source counter by only one. The Steady-State MNA analysis implementation did not include current-controlled voltage sources but could easily be added if desired.

5.1.9 Voltage-Controlled Voltage Source

The SPICE representation of a voltage-controlled voltage source (VCVS) appears as:

Exxxxxxx Node1 Node2 Node3 Node4 Gain

In the first pass for State-Space analysis, we collect the names of each of the four nodes and add them to our list of nodes in the circuit if it is not already included. Since it is a source, we also increment our source counter and add the output (voltage source) side as a new unknown current to the vector $\mathbf{x}_i$. The Steady-State MNA analysis implementation did not include voltage-controlled voltage sources but could easily be added if desired.

5.1.10 Subcircuit

The SPICE representation of a subcircuit element appears as:

Xxxxxxxx node1 node2 ... nodeN sub_name

This must also be paired with a subcircuit definition which would appear as follows:

.subckt sub_name node1 node2 ... nodeN ⋮.ends sub_name

This has not yet been implemented in the current code. However, it would contain the same relevant information of a set of nodes that need to be added to our list of nodes in the circuit if not already included [1], [2]. This would then be followed up by parsing all the components included in the subcircuit in the same ways as described in the earlier parts of this Chapter

5.2 Second Pass

In preparation for the second pass, the information gathered from the first pass gives sufficient information to determine the necessary sizes of the ma-

trices for each different stamping method. This allows us to create static matrices (typically initialized to zeros) without having to consider dynamically allocating more memory.

For the Steady-State MNA formulation, the size of the square matrix $\mathbf{A}$ becomes the sum of the number of nodes in the circuit (minus one for the ground node, which is not included in the matrix) and unknown currents (including both independent voltage sources and inductors) in each dimension. The vectors $\mathbf{x}$ and $\mathbf{z}$ have the same height as the matrix $\mathbf{A}$, but width of one.

For the State-Space formulation, we have many more matrices that must be created between the two passes. The size of the vector $\mathbf{x}$ is the combined size of $\mathbf{x}_v$ (node voltages) and $\mathbf{x}_i$ (unknown currents). Matrix $\mathbf{C}$ is a square matrix with each dimension the same length as the size of vector $\mathbf{x}$. Matrix $\mathbf{G}$ is also a square matrix with the same dimensions as matrix $\mathbf{C}$. Matrix $\mathbf{B}$ is a rectangular matrix with width equal to the number of voltage and current sources in the circuit, and height equal to the size of vector $\mathbf{x}$. Matrix $\mathbf{L}$ has the same dimensions as the transpose of matrix $\mathbf{B}$. Finally, vector $\mathbf{u}$ has length equal to the number of voltage and current sources in the circuit.

As can be seen, the majority of components have some sort of value attached to them, such as a resistance, capacitance, gain, voltage, etc. When these values are either very large or very small, it is typical to use a metric prefix to the units to describe a power of ten, such as using "10k" in place of writing out "10000" or using "5p" in place of "0.000000000005". This improves readability of the netlist. Both programs allow the use of this as well for metric prefixes from "T" for "Tera-" as 10^{12} down to "f" for "femto-" as 10^{-15} in intervals of 10^3. The program also includes a few select additional metric prefixes "d" and "c" for "deci-" and "centi-" respectively.

The final step of the second pass is to update each of the matrices for the appropriate stamp based on the formulation method chosen. This process is described in Chapters 6 and 7 for Steady-State MNA and State-Space analyses respectively.

CHAPTER 6

STEADY-STATE MNA FORMULATION IMPLEMENTATION

As described in Chapter 3, the MNA formulation follows the form shown in Equation 6.1. The matrix $\mathbf{A}$ can be broken up into submatrices $\mathbf{G}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{L}$ as shown below in Equation 6.2

$$\mathbf{z} = \mathbf{A} \cdot \mathbf{x} \tag{6.1}$$

$$[\mathbf{x}] = \begin{bmatrix} \mathbf{G} & \mathbf{B} \\ \mathbf{C} & \mathbf{L} \end{bmatrix} \tag{6.2}$$

6.1 Implementation

The implementation of the steady-state MNA formulation was built as a stepping stone towards transient analysis, so only the most common and simple circuit elements were implemented. These components included resistors, inductors, capacitors, independent current sources, and independent voltage sources. The procedure we followed to generate this formulation was to break down the analysis into two passes. The purpose of the first pass is to gather information about the circuit in order to determine the sizes of the three matrices in Equation 6.1. This was described in depth previously in Chapter 4, so in this section we will focus on the second pass.

6.1.1 Resistor

The behavior of a resistor is described by its resistance. This can be equivalently described as a conductance. This can be included in the conductance matrix $\mathbf{G}$ which is the upper left quadrant of the $\mathbf{A}$ matrix. The conductance matrix has one row and column for each node in the circuit, so we can relate

the nodes based on the conductance of the resistor and Ohm's law, as shown in Figure 6.1 for the example resistor.

$$V = I \cdot R \rightarrow (V_{pos} - V_{neg}) \cdot (1/R) = I \tag{6.3}$$

Figure 6.1: Resistor for MNA Formulation

$$\begin{bmatrix} \frac{1}{R} & \cdots & -\frac{1}{R} \\ \vdots & & \vdots \\ -\frac{1}{R} & \cdots & \frac{1}{R} \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \end{bmatrix} = \begin{bmatrix} \\ \\ \\ \end{bmatrix} \tag{6.4}$$

If the resistor has resistance 0 Ω, this model is ineffective as the conductance of the resistor goes to infinity. Since a 0 Ω resistor is simply a wire, we can replace this with a more usable model of a 0 V independent DC voltage source. The general implementation of a voltage source is described later in this section.

6.1.2 Capacitor

The behavior of a capacitor is described by its capacitance. Its impedance can be described as $\frac{1}{j\omega C}$, or equivalently by its admittance $j\omega C$. This can be included in the conductance matrix **G** which is the upper left quadrant of the **A** matrix. The conductance matrix has one row and column for each node in the circuit, so we can relate the nodes based on the admittance of the capacitor and Ohm's law, as shown in Figure 6.2 for the example capacitor.

$$V = I \cdot Z \rightarrow (V_{pos} - V_{neg}) \cdot (j\omega C) = I \tag{6.5}$$

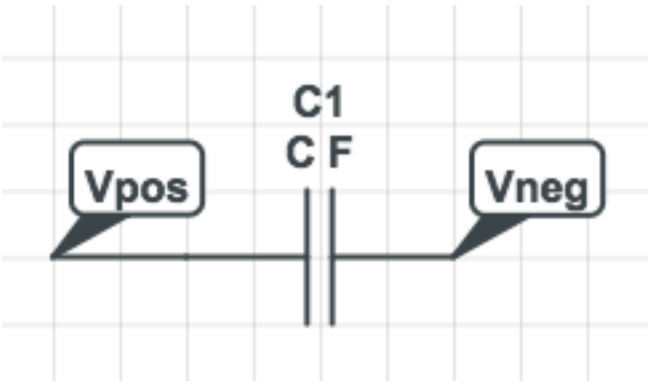

Figure 6.2: Capacitor for MNA Formulation

$$\begin{bmatrix} j\omega C & \dots & -j\omega C \\ \vdots & & \vdots \\ -j\omega C & \dots & j\omega C \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \end{bmatrix} = \begin{bmatrix} \ \end{bmatrix} \tag{6.6}$$

6.1.3 Inductor

The behavior of an inductor is described by its inductance. Inductors can be described by Equation 6.7. This translates to affecting the **A** matrix in the submatrices **B**, **C**, and **L**. This is shown in Figure 6.3 for the example inductor.

$$V_{pos} - V_{neg} - j\omega L = 0 \tag{6.7}$$

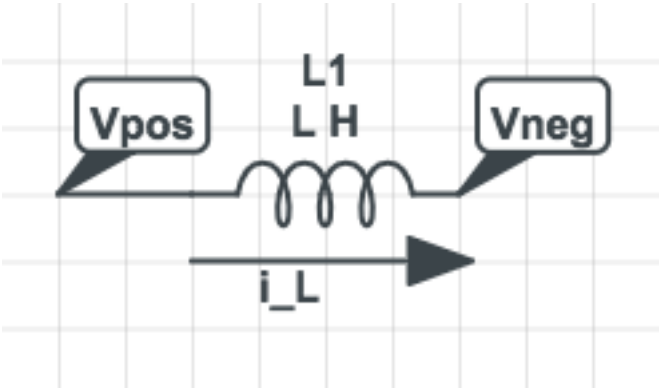

Figure 6.3: Inductor for MNA Formulation

$$\begin{bmatrix} & & & & 1 \\ & & & & \vdots \\ & & & & -1 \\ & & & & \vdots \\ 1 & \dots & -1 & \dots & -j\omega L \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ i_L \end{bmatrix} = \begin{bmatrix} \\ \\ \\ \\ \\ \end{bmatrix} \tag{6.8}$$

6.1.4 Independent Voltage Source

The behavior of an independent voltage source is defined by the voltage it provides. There is a current through the independent voltage source that moves from node N_{pos} to node N_{neg}, and there is an increase in voltage by V volts from node N_{neg} to node N_{pos} as shown in Figure 6.4. This results in adding two currents to the KCL expression, and one added to the KVL expression (shown in Equation 6.9).

$$V_{Npos} - V_{Nneg} = V \tag{6.9}$$

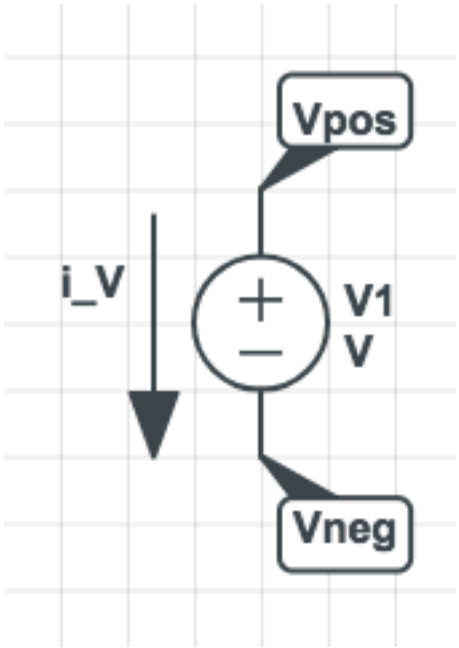

Figure 6.4: Independent Voltage Source for MNA Formulation

$$\begin{bmatrix} & & & 1 \\ & & & \vdots \\ & & & -1 \\ & & & \vdots \\ 1 & \dots & -1 & \dots \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ i_V \end{bmatrix} = \begin{bmatrix} \\ \vdots \\ \\ V \end{bmatrix} \tag{6.10}$$

6.1.5 Independent Current Source

The behavior of an independent current source is a simple current injection. The outputs of the KCL expressions are decreased at node Node1 and increased at node Node2 as shown in Figure 6.5. This can simply be represented by increasing/decreasing the current at the appropriate nodes in the output vector **z**.

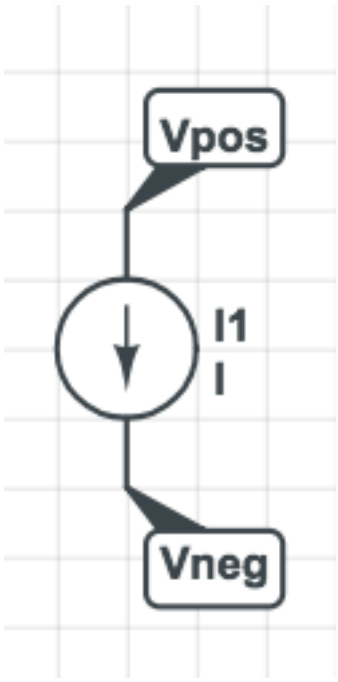

Figure 6.5: Independent Current Source for MNA Formulation

$$\begin{bmatrix} & \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \end{bmatrix} = \begin{bmatrix} I \\ \\ -I \end{bmatrix} \tag{6.11}$$

6.1.6 End of Netlist

Any line that comes after the Ends line is ignored entirely. This can be in either lowercase or capital letters.

6.1.7 Comments

Comments are lines in the netlist that are ignored. They are not part of the circuit implementation, nor do they affect the generation of the stamp for the circuit.

The matrices are smaller by one because the ground node is not included in the steady-state MNA stamp. The row and column associated with the ground node are removed, as are any values in those locations in the matrices. The ground node in the existing code was determined to simply be the last node named in the netlist, but can be prioritized to choose a node as ground if it is named "gnd", "GND", or "0", since these are the typical names for the ground node [3], [5].

6.2 Sample Circuits and Stamps

6.2.1 Example 1

The circuit in Figure 6.6 was the first test used to verify the functionality of the code for voltage sources and resistors. As the first test, it also ensures that the code can correctly identify and separate different nodes and other components of the netlist.

V1 1 3 5
R1 1 3 200
R2 1 2 100
R3 2 3 100

$$\mathbf{A} \cdot \mathbf{x}_n = \mathbf{z} : \begin{bmatrix} 0.015 & -0.005 & 1 \\ -0.005 & 0.015 & -1 \\ -1 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_3 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 5 \end{bmatrix} \tag{6.12}$$

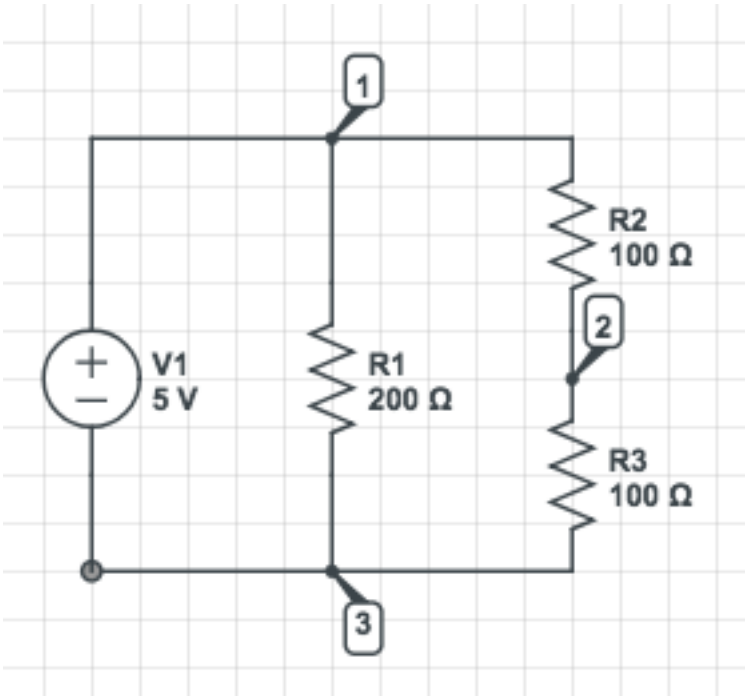

Figure 6.6: Sample Circuit Containing Voltage Sources and Resistors

6.2.2 Example 2

The circuit in Figure 6.7 was the second test used to verify the functionality of the code for current sources after other voltage sources and resistors were shown to work in the previous test. This was also used to ensure that nodes not named numerically could be handled by the code.

I1 a b 1.1
V1 c d 10
R1 b e 1
R2 e a 2
R3 a d 3
R4 e d 4
R5 e c 5

$$\mathbf{A} \cdot \mathbf{x}_n = \mathbf{z} : \begin{bmatrix} 0.83333 & 0 & 0 & -0.3333 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0.2 & 0 & 0 \\ -0.3333 & 0 & 0 & 0.58333 & -1 \\ 0 & 0 & 1 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ I_{V1} \end{bmatrix} = \begin{bmatrix} -1.1 \\ 1.1 \\ 0 \\ 0 \\ 10 \end{bmatrix} \quad (6.13)$$

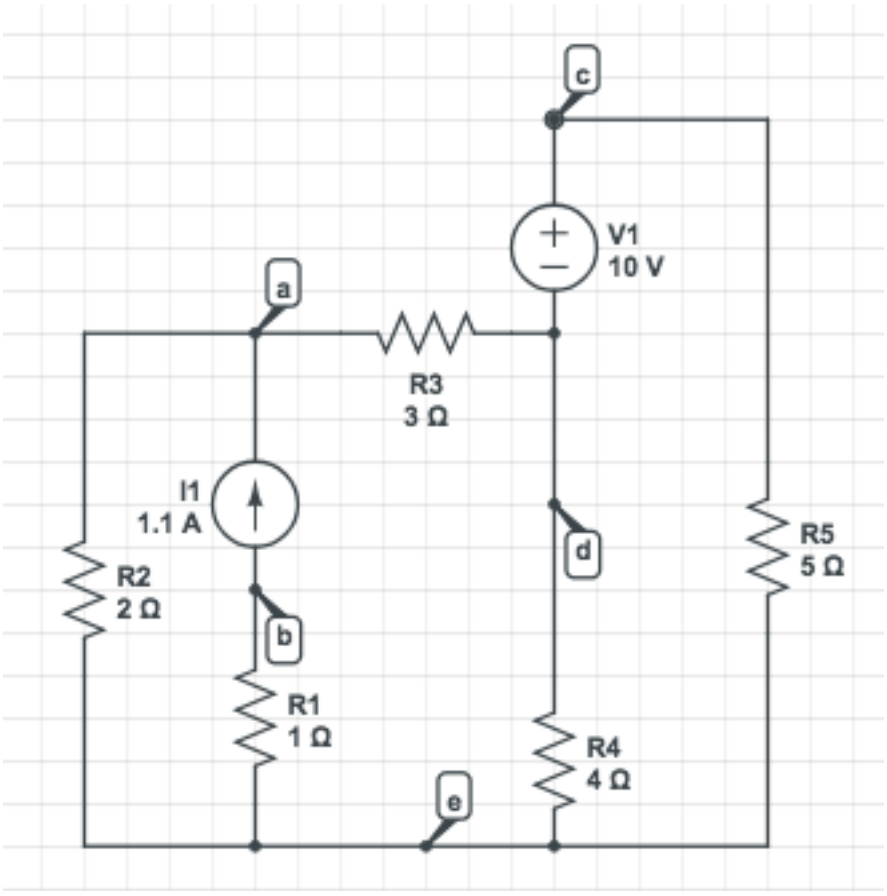

Figure 6.7: Sample Circuit Containing Voltage Sources, Current Sources, and Resistors for Testing the Steady-State MNA Formulation

6.2.3 Example 3

The circuit in Figure 6.8 was the third test used to verify the functionality of the code for capacitors as well as testing if the program can handle exponential notation in the component value.

C2 1 2 1e-3

V1 1 3 5

C1 1 3 2e-3

C3 2 3 1e-3

$$\mathbf{A} \cdot \mathbf{x}_n = \mathbf{z} : \begin{bmatrix} 3000000j & -1000000j & 1 \\ -1000000j & 2000000j & 0 \\ 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ I_{V1} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 5 \end{bmatrix} \tag{6.14}$$

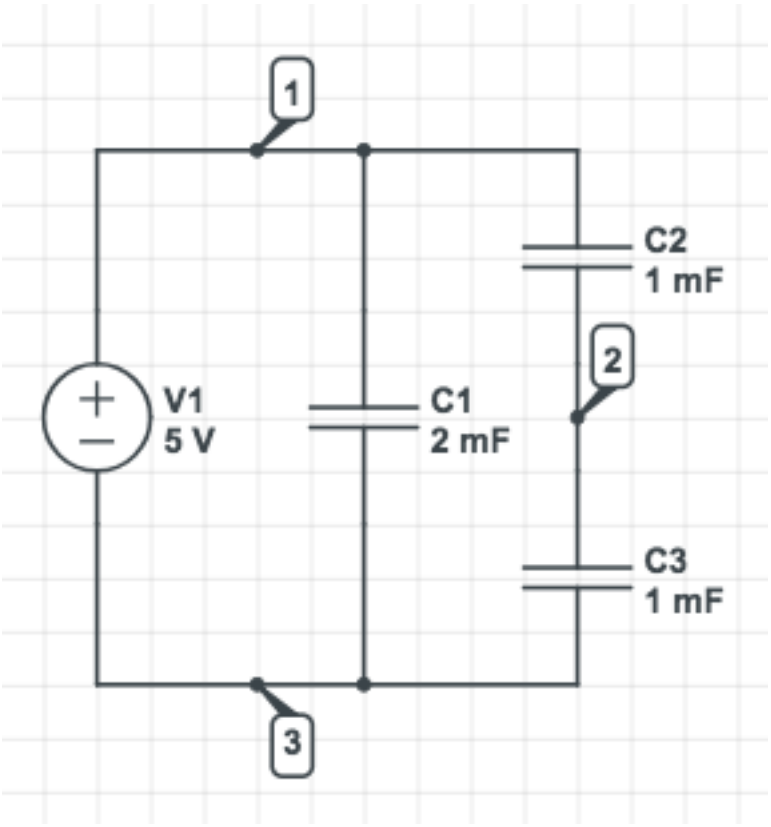

Figure 6.8: Sample Circuit Containing Voltage Sources and Capacitors for Testing the Steady-State MNA Formulation

6.2.4 Example 4

The circuit in Figure 6.9 was used to test and verify the functionality of the code for inductors as well as testing if the program can correctly process prefixes in the component value.

I1 a b 1.1u
L1 c d 10n
R1 b e 1m
R2 e a 2
R3 a d 3
R4 e d 4
R5 e c 5

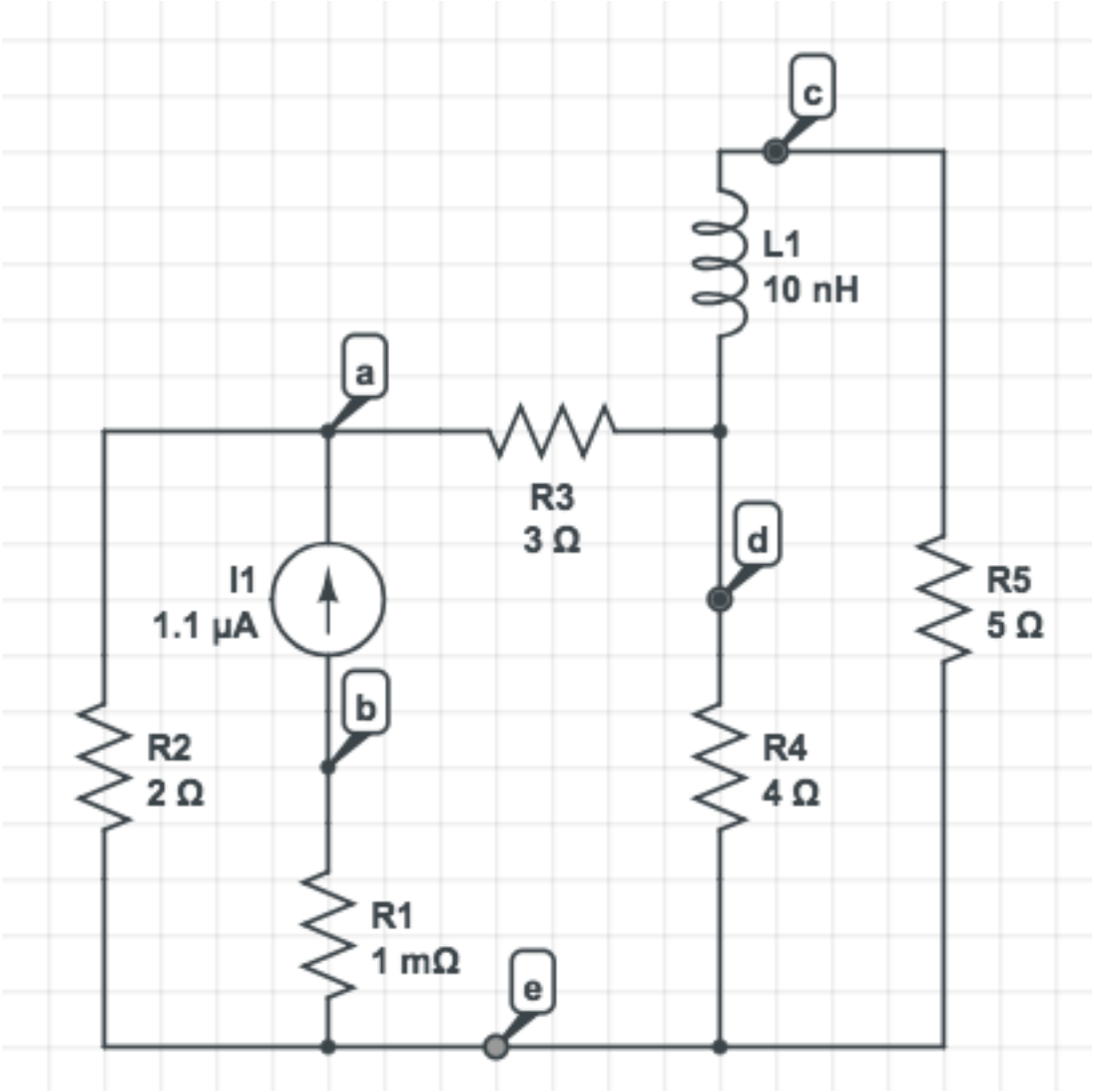

Figure 6.9: Sample Circuit Containing Current Sources and Inductors for Testing the Steady-State MNA Formulation

$$\mathbf{A}\cdot\mathbf{x}_n = \mathbf{z}: \begin{bmatrix} 0.833333 & 0 & 0 & -0.333333 & 0 \\ 0 & 1000.0 & 0 & 0 & 0 \\ 0 & 0 & 0.2 & 0 & 1 \\ -0.333333 & 0 & 0 & 0.583333 & -1 \\ 0 & 0 & 1 & -1 & -10j \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ I_{L1} \end{bmatrix} = \begin{bmatrix} -1.1e-06 \\ 1.1e-06 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.15}$$

6.2.5 Example 5

The circuit in Figure 6.10 was an outside example [5] used to externally validate the solution to be correct.

R4 1 3 4
R2 2 3 2
IS 4 1 1
VS 1 3 5
R1 1 4 1
R3 3 4 3
C1 1 4 1e-3
C2 2 4 2e-3

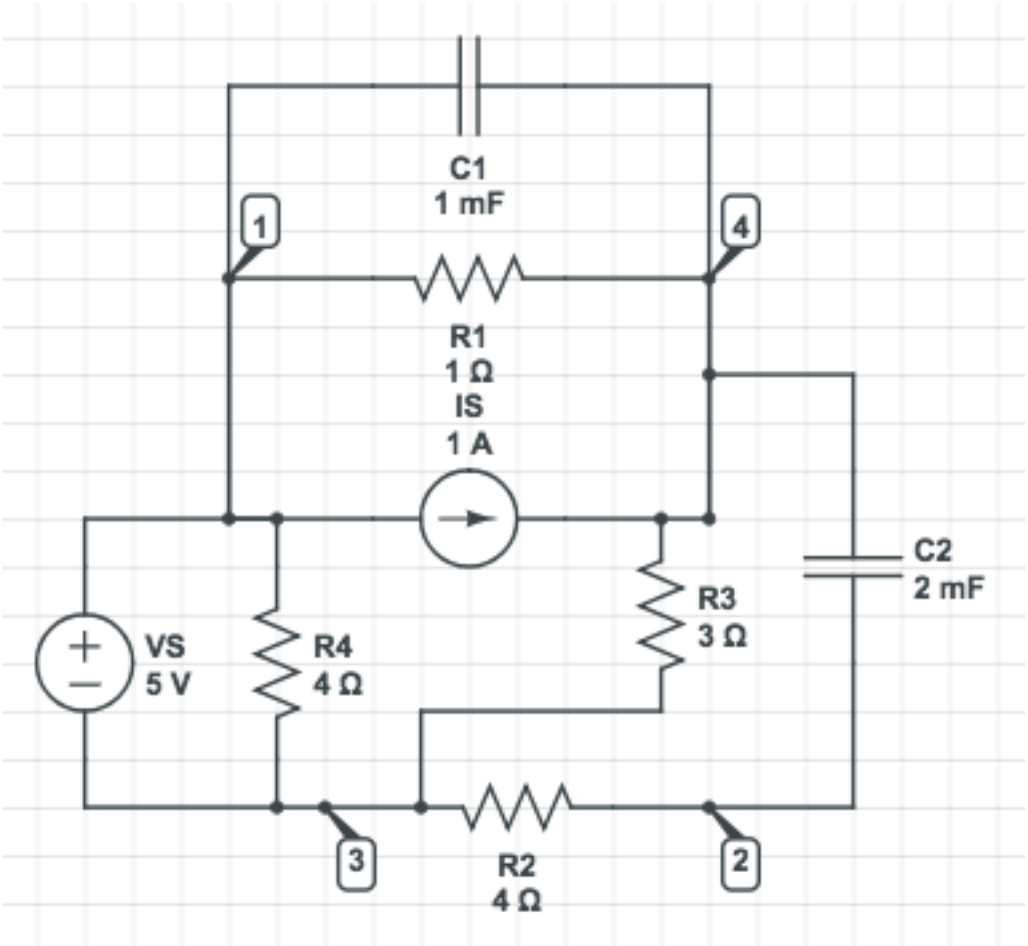

Figure 6.10: Example Circuit [5] for Testing the Steady-State MNA Formulation

$$\mathbf{A}\cdot\mathbf{x}_n = \mathbf{z}: \begin{bmatrix} (1.25+1000000j) & -0.25 & 0 & 1 \\ -0.25 & 1.083333 & -0.5 & -1 \\ 0 & -0.5 & (0.5+2000000j) & 0 \\ 1 & -1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_3 \\ V_2 \\ I_{VS} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 5 \end{bmatrix} \tag{6.16}$$

CHAPTER 7

STATE-SPACE FORMULATION IMPLEMENTATION

As described in Chapter 4, the State-Space formulation follows the form shown in Equations 7.1 and 7.2.

$$\mathbf{C} \cdot \mathbf{x}'_n = -\mathbf{G} \cdot \mathbf{x}_n + \mathbf{B} \cdot \mathbf{u} \tag{7.1}$$

$$\mathbf{y} = \mathbf{L} \cdot \mathbf{x}_n \tag{7.2}$$

7.1 Implementation

The implementation of the State-Space formulation was built as the second step towards transient analysis, so more components were implemented than in the steady-state MNA stamping described previously. The components in the stamp implementation for the State-Space solution include resistors, inductors, capacitors, independent current sources, independent voltage sources, voltage-controlled voltage sources, voltage-controlled current sources, current-controlled voltage sources, and current-controlled current sources. The procedure we followed to generate this formulation was to break down the analysis into two passes. The purpose of the first pass is to gather information about the circuit in order to determine the sizes of the three matrices in Equation 7.2. This was described in depth in Chapter 5, so in this section we will focus on the second pass.

7.1.1 Resistor

The behavior of a resistor is described by its resistance. This can be equivalently described as a conductance, which can be included in the conductance matrix $\mathbf{G}$. The conductance matrix has one row and column for each node

in the circuit, so we can relate the nodes based on the conductance of the resistor and Ohm's law, as shown in Figure 7.1 for the example resistor.

$$V = IR \rightarrow (V_{pos} - V_{neg}) \cdot (\frac{1}{R}) = I \rightarrow \frac{1}{R}V_{pos} + \frac{1}{R}V_{neg} = I \tag{7.3}$$

Figure 7.1: Resistor for State-Space Formulation

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} \frac{1}{R} & \dots & -\frac{1}{R} \\ \vdots & & \vdots \\ -\frac{1}{R} & \dots & \frac{1}{R} \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \end{bmatrix} \tag{7.4}$$

If the resistor has resistance 0 Ω, this model is ineffective as the conductance of the resistor goes to infinity. Since a 0 Ω resistor is simply a wire, we recommend replacing this with a more easily implemented model of a 0 V independent DC voltage source. The general implementation of a voltage source is described later in this section.

7.1.2 Capacitor

The behavior of a capacitor is described by its capacitance. This can be described as shown in Equation 7.5, and can be represented in the **C** matrix as shown in the example in Figure 7.2.

$$I = C\frac{dv}{dt} \tag{7.5}$$

$$\mathbf{C} \cdot \mathbf{x}'_n = \begin{bmatrix} C & \dots & -C \\ \vdots & & \vdots \\ -C & \dots & C \end{bmatrix} \cdot \begin{bmatrix} V'_{pos} \\ \vdots \\ V'_{neg} \end{bmatrix} \tag{7.6}$$

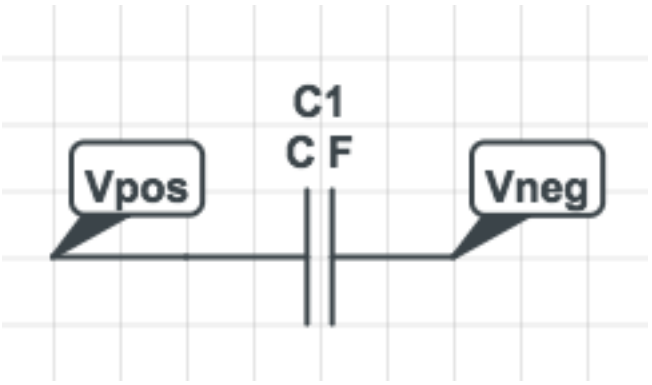

Figure 7.2: Capacitor for State-Space Formulation

7.1.3 Inductor

The behavior of an inductor is described by its inductance. Inductors can be described by equation 7.7. This can be represented in the **G** and **C** matrices as shown in the example in Figure 7.3.

$$L\frac{di}{dt} = V_{pos} - V_{neg} \tag{7.7}$$

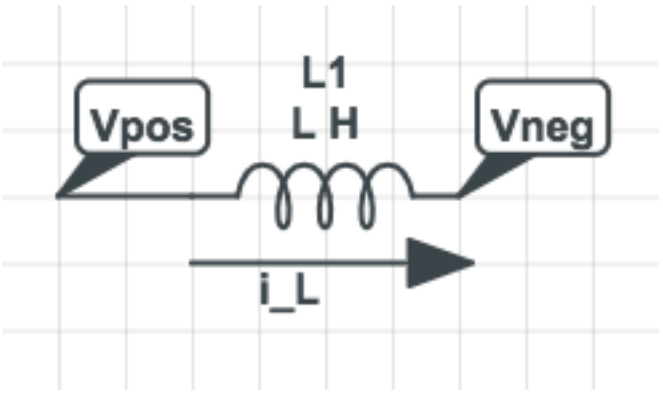

Figure 7.3: Inductor for State-Space Formulation

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} & & 1 \\ & & \vdots \\ & & -1 \\ & & \\ 1 & \dots & -1 \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ i_L \end{bmatrix} \tag{7.8}$$

$$\mathbf{C} \cdot \mathbf{x}'_n = \begin{bmatrix} & & \\ & & \\ & & \\ & & L \end{bmatrix} \cdot \begin{bmatrix} V'_{pos} \\ \vdots \\ V'_{neg} \\ \vdots \\ i'_L \end{bmatrix} \tag{7.9}$$

7.1.4 Independent Voltage Source

The behavior of an independent voltage source is defined by the voltage it provides. There is a current through the independent voltage source that moves from node Npos to node Nneg, and there is an increase in voltage by V volts from node Nneg to node Npos as shown in Figure 7.4. This is represented by Equation 7.10.

$$V_{Npos} - V_{Nneg} = V \tag{7.10}$$

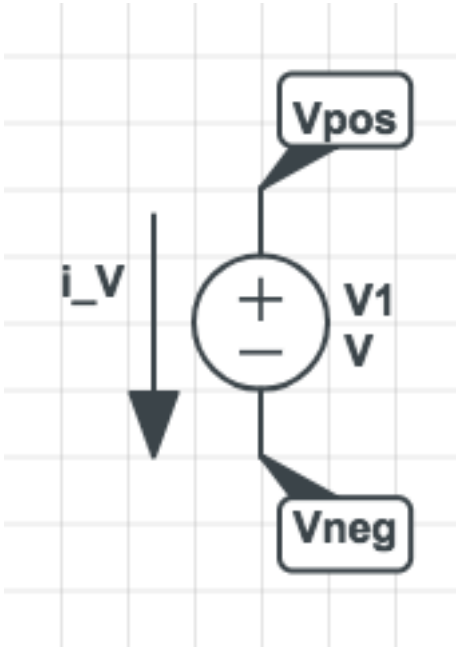

Figure 7.4: Independent Voltage Source for State-Space Formulation

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} & & 1 \\ & & \vdots \\ & & -1 \\ & & \\ 1 & \dots & -1 \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ i_{v_s} \end{bmatrix} \tag{7.11}$$

$$\mathbf{B} \cdot \mathbf{u} = \begin{bmatrix} & \vdots & \\ & & \\ \dots & -1 & \dots \\ & & \\ & & \end{bmatrix} \cdot \begin{bmatrix} \\ \vdots \\ V \\ \vdots \end{bmatrix}, \mathbf{L} = \mathbf{B}^T \tag{7.12}$$

7.1.5 Independent Current Source

The behavior of an independent current source is defined by the current it provides. There is a voltage across the independent current source from node Nneg to node Npos and a current from node V_{Npos} to V_{Nneg} as shown in Figure 7.5. This is represented by Equation 7.13.

$$I_{Npos} - I_{Nneg} = I \tag{7.13}$$

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} & & 1 \\ & & \vdots \\ & & -1 \\ & & \vdots \\ & \dots & -1 \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ i_{i_s} \end{bmatrix} \tag{7.14}$$

$$\mathbf{B} \cdot \mathbf{u} = \begin{bmatrix} & \vdots & \\ & & \\ \dots & -1 & \dots \\ & & \\ & & \end{bmatrix} \cdot \begin{bmatrix} \\ \vdots \\ I \\ \vdots \end{bmatrix} \tag{7.15}$$

$$\mathbf{L} \cdot \mathbf{x} = \begin{bmatrix} & -1 & \\ & \vdots & \\ \dots & 1 & \dots \\ & & \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ i_{i_s} \end{bmatrix} \tag{7.16}$$

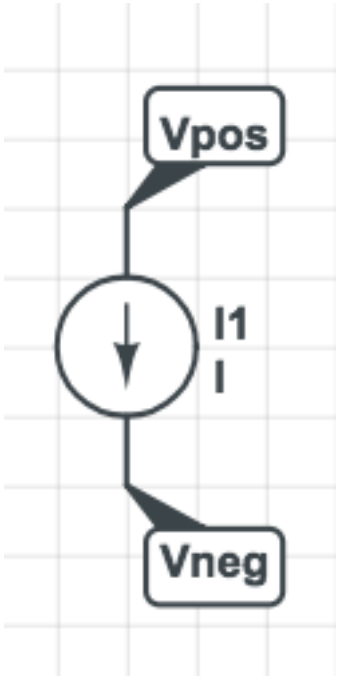

Figure 7.5: Independent Current Source for State-Space Formulation

7.1.6 Voltage-Controlled Voltage Source

A voltage-controlled voltage source provides a voltage based on a measured voltage elsewhere in the circuit. The reference input voltage difference between two determined nodes is measured and a dependent voltage source outputs a voltage that is larger than the measurement by a factor of Av as shown in Figure 7.6. This is represented by Equation 7.17.

$$(V_{ref+} - V_{ref-}) * Av = (V_{out+} - V_{out-}) \tag{7.17}$$

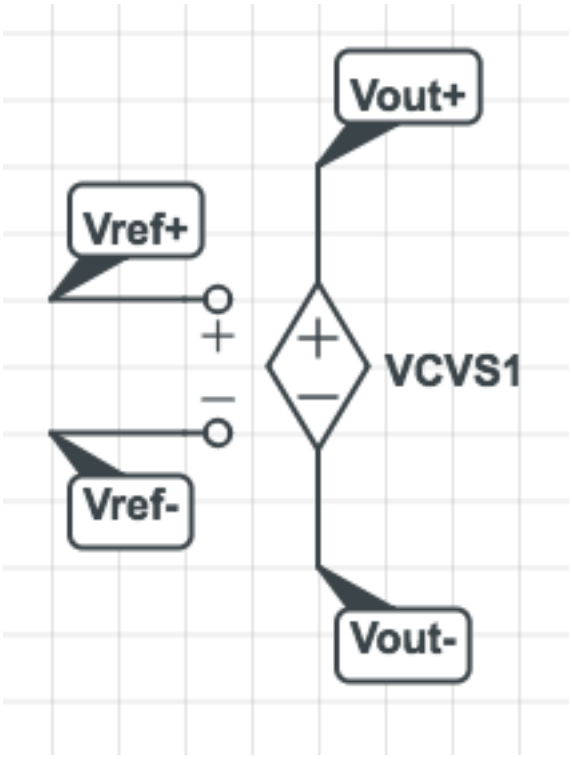

Figure 7.6: VCVS for State-Space Formulation

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} & & & & & & & -1 \\ & & & & & & & \vdots \\ & & & & & & & 1 \\ & & & & & & & \vdots \\ & & & & & & & \\ & & & & & & & \\ & & & & & & & \\ & & & & & & & \\ -1 & \dots & 1 & \dots & A_v & \dots & -A_v & \dots \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ V_{ref+} \\ \vdots \\ V_{ref-} \\ \vdots \\ i_{v_s} \end{bmatrix} \tag{7.18}$$

7.1.7 Voltage-Controlled Current Source

A voltage-controlled current source provides a current based on a measured voltage elsewhere in the circuit. The reference input voltage difference between two determined nodes is measured and a dependent current source

outputs a current that is larger than the measurement by a factor of g_m from node *Ineg* to *Ipos* as shown in Figure 7.7. This is represented by Equation 7.19:

$$(V_{ref+} - V_{ref-}) * g_m = I_{out} \tag{7.19}$$

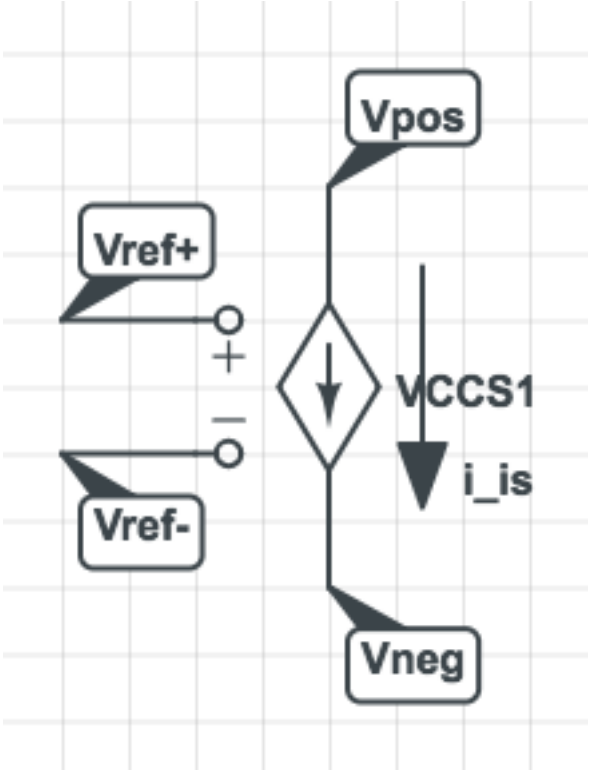

Figure 7.7: VCCS for State-Space Formulation

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} & & & & & & 1 \\ & & & & & & \vdots \\ & & & & & & -1 \\ & & & & & & \vdots \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ . & \dots & . & 1 & \dots & -1 & \dots & \frac{1}{g_m} \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ V_{ref+} \\ \vdots \\ V_{ref-} \\ \vdots \\ i_{i_s} \end{bmatrix} \tag{7.20}$$

7.1.8 Current-Controlled Voltage Source

A current-controlled voltage source provides a voltage based on a measured current elsewhere in the circuit. The reference current through a given independent voltage source is measured, and a dependent voltage source outputs a voltage that is larger than the measurement by a factor of gain as shown in Figure 7.8. This is represented by Equation 7.21:

$$I_{ref} * gain = (V_{out+} - V_{out-}) \tag{7.21}$$

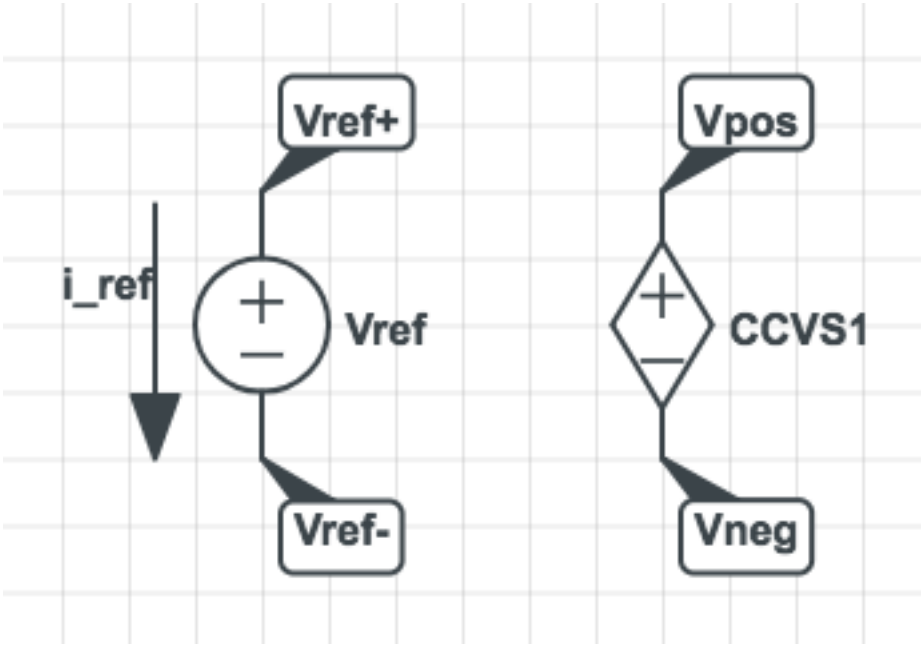

Figure 7.8: CCVS for State-Space Formulation

$$\mathbf{G} \cdot \mathbf{x}_n = \begin{bmatrix} & & & & & & & 1 & \\ & & & & & & & \vdots & \\ & & & & & & & -1 & \\ & & & & & & & \vdots & \\ & & & & & & & \frac{1}{gain} & \\ & & & & & & & \vdots & \\ & & & & & & & -\frac{1}{gain} & \\ & & & & & & & \vdots & \\ . & \dots & . & 1 & \dots & -1 & \dots & & \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ V_{ref+} \\ \vdots \\ V_{ref-} \\ \vdots \\ i_{out} \end{bmatrix} \tag{7.22}$$

7.1.9 Current-Controlled Current Source

A current-controlled current source provides a current based on a measured current elsewhere in the circuit. The reference current through a given independent voltage source is measured and a dependent current source outputs a current that is larger than the measurement by a factor of gain from node Ineg to Ipos as shown in Figure 7.9. This is represented by Equation 7.23:

$$I_{ref} * gain = I_{out} \tag{7.23}$$

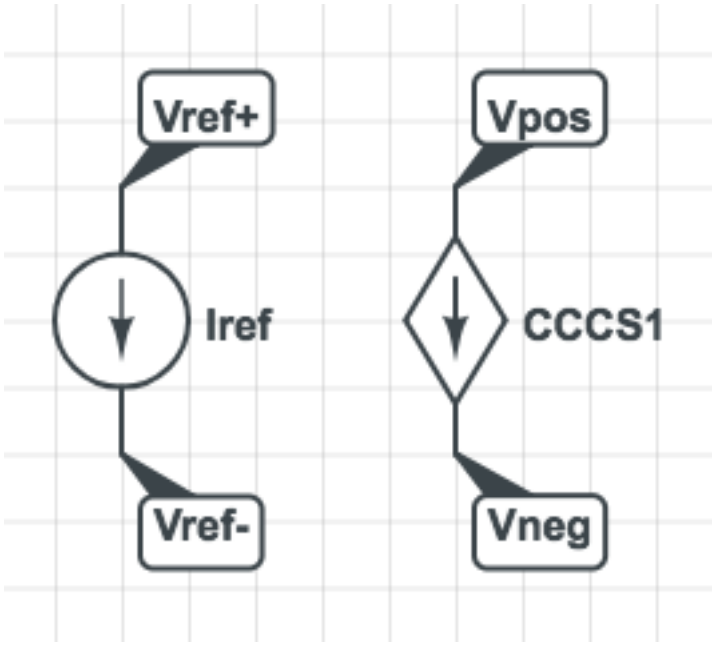

Figure 7.9: CCCS for State-Space Formulation

$$\mathbf{G}\cdot\mathbf{x}_n = \begin{bmatrix} & & & & & & & & -1 \\ & & & & & & & & \vdots \\ & & & & & & & & 1 \\ & & & & & & & & \vdots \\ & & & & & & 1 & & \\ & & & & & & \vdots & \cdots & \\ & & & & & & -1 & & \\ & & & & & & \vdots & & \\ 1 & \cdots & -1 & & & \cdots & -gain & & \\ & & & & & \vdots & & & \\ & & & \cdots & 1 & \cdots & -1 & & \end{bmatrix} \cdot \begin{bmatrix} V_{pos} \\ \vdots \\ V_{neg} \\ \vdots \\ V_{ref+} \\ \vdots \\ V_{ref-} \\ \vdots \\ i_{in} \\ \vdots \\ i_{out} \end{bmatrix} \tag{7.24}$$

7.1.10 End of Netlist

Any line that come after the Ends line is ignored entirely. This can be in either lowercase or capital letters.

7.1.11 Comments

Comments are lines in the netlist that are ignored. They are not part of the circuit implementation, nor do they affect the generation of the stamp for the circuit [4].

7.2 Sample Circuits and Stamps

7.2.1 Example 1

The circuit in Figure 7.10 was the first test used to verify the functionality of the code for voltage sources and resistors. As the first test, it also ensures that the code can correctly identify and separate different nodes and other components of the netlist.

V1 1 3 5

R1 1 3 200

R2 1 2 100

R3 2 3 100

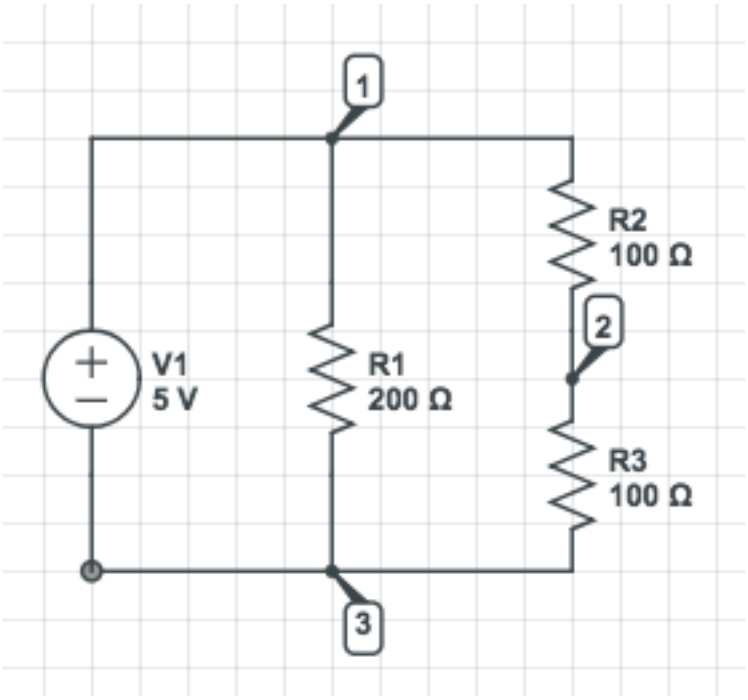

Figure 7.10: Sample Circuit Containing Voltage Sources and Resistors for Testing the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \mathbf{G}: \begin{bmatrix} 0.015 & -0.005 & 1.0 \\ -0.005 & 0.015 & -1.0 \\ -1.0 & 1.0 & 0.0 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0.0 \\ 0.0 \\ -1.0 \end{bmatrix}, \mathbf{L}: \begin{bmatrix} 0.0 & 0.0 & -1.0 \end{bmatrix} \tag{7.25}$$

7.2.2 Example 2

The circuit in Figure 7.11 was the second test used to verify the functionality of the code for current sources after other voltage sources and resistors were shown to work in the previous test. This was also used to ensure that nodes not named numerically could be handled by the code.

I1 a b 1.1

V1 c d 10

R1 b e 1

R2 e a 2

R3 a d 3

R4 e d 4

R5 e c 5

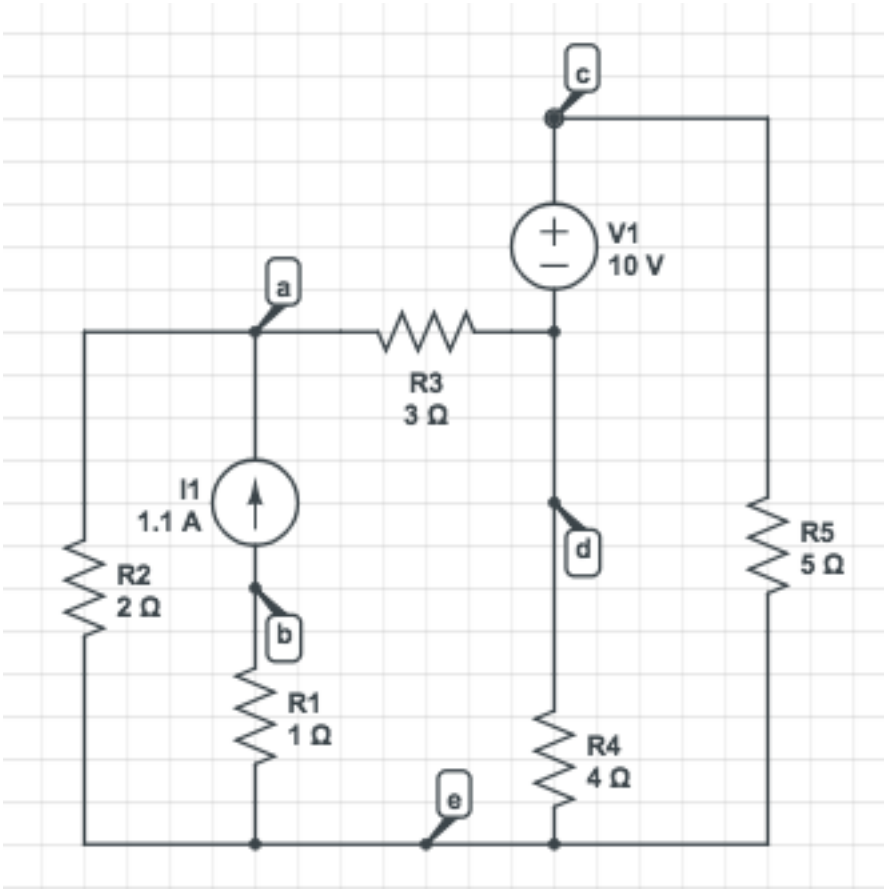

Figure 7.11: Sample Circuit Containing Voltage Sources, Current Sources, and Resistors for Testing the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{G}: \begin{bmatrix} 0.833333 & 0 & 0 & -0.33333 & 1 & 0 \\ 0 & 1.0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0.2 & 0 & 0 & 1 \\ -0.333333 & 0 & 0 & 0.5833333 & 0 & -1 \\ 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 \end{bmatrix} \tag{7.26}$$

$$\mathbf{B}: \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & -1 \end{bmatrix}, \mathbf{L}: \begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix} \tag{7.27}$$

7.2.3 Example 3

The circuit in Figure 7.12 was the third test used to verify the functionality of the code for capacitors as well as whether the program can handle exponential notation in the component value.

C2 1 2 1e-3

V1 1 3 5

C1 1 3 2e-3

C3 2 3 1e-3

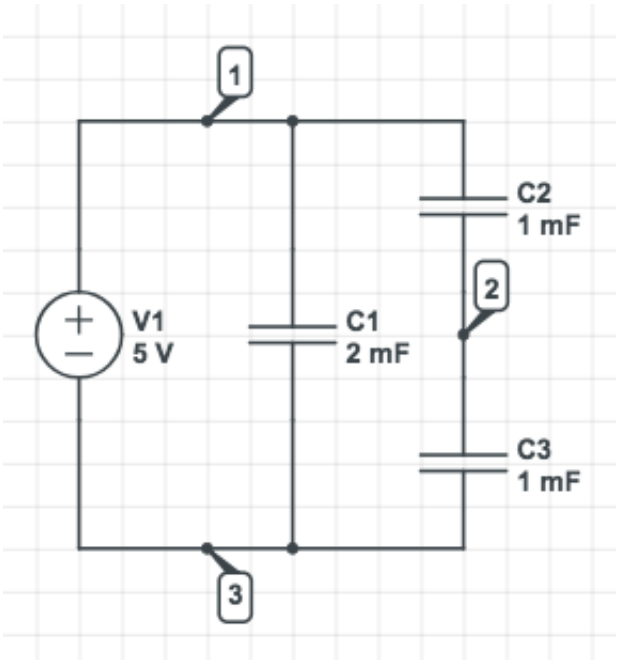

Figure 7.12: Sample Circuit Containing Voltage Sources and Capacitors for Testing the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 0.003 & -0.001 & 0 \\ -0.001 & 0.002 & 0 \\ 0 & 0 & 0 \end{bmatrix} \mathbf{G}: \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ -1 & 0 & 0 \end{bmatrix} \mathbf{B}: \begin{bmatrix} 0 \\ 0 \\ -1 \end{bmatrix} \mathbf{L}: \begin{bmatrix} 0 & 0 & -1 \end{bmatrix} \tag{7.28}$$

7.2.4 Example 4

The circuit in Figure 7.13 was used to test and verify the functionality of the code for inductors as well as whether the program can correctly process prefixes in the component value.

I1 a b 1.1u
L1 c d 10n
R1 b e 1m
R2 e a 2
R3 a d 3
R4 e d 4
R5 e c 5

$$\mathbf{C}: \begin{bmatrix} 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1e-08 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0.0 \\ 0.0 \\ 0.0 \\ 0.0 \\ -1.0 \\ 0.0 \end{bmatrix} \tag{7.29}$$

$$\mathbf{G}: \begin{bmatrix} 0.833333333 & 0.0 & 0.0 & -0.33333333 & 1.0 & 0.0 \\ 0.0 & 1000.0 & 0.0 & 0.0 & -1.0 & 0.0 \\ 0.0 & 0.0 & 0.2 & 0.0 & 0.0 & 1.0 \\ -0.3333333 & 0.0 & 0.0 & 0.5833333333 & 0.0 & -1.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & -1.0 & 0.0 \\ 0.0 & 0.0 & -1.0 & 1.0 & 0.0 & 0.0 \end{bmatrix}, \mathbf{L}^T: \begin{bmatrix} -1.0 \\ 1.0 \\ 0.0 \\ 0.0 \\ 0.0 \\ 0.0 \end{bmatrix} \tag{7.30}$$

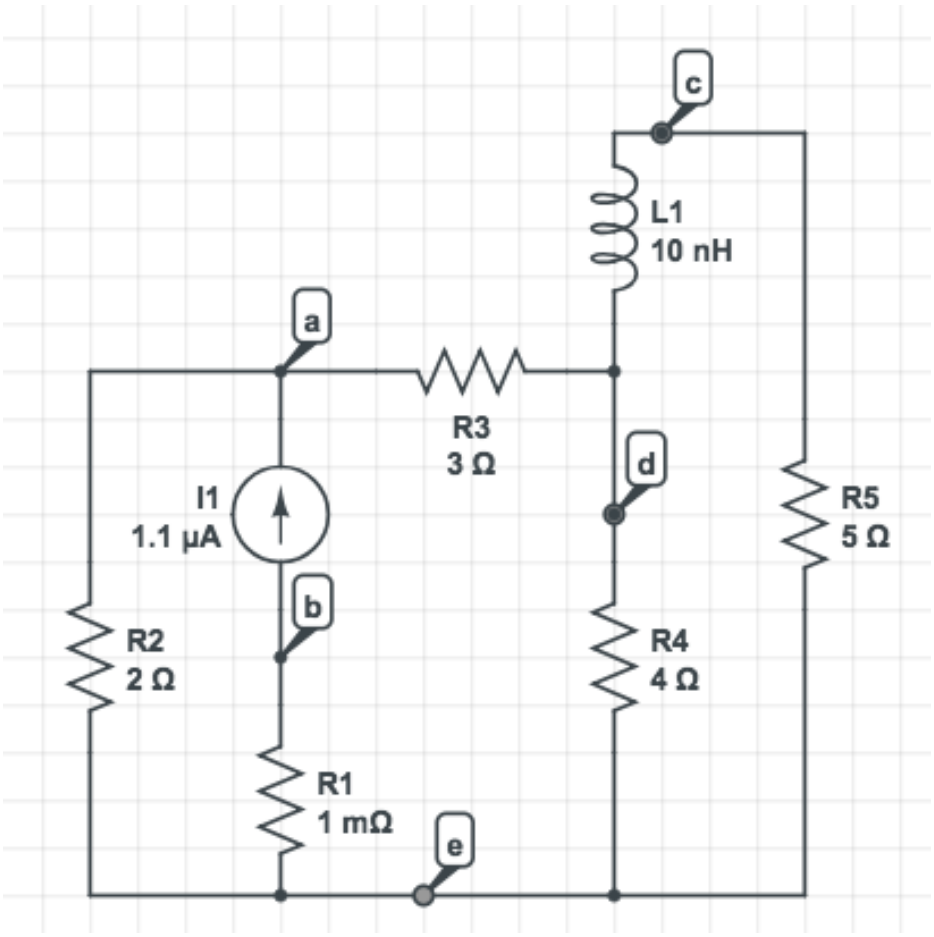

Figure 7.13: Sample Circuit Containing Current Sources and Inductors for Testing the State-Space Formulation

7.2.5 Example 5

The circuit in Figure 7.14 was an outside example [4] used to externally validate the solution to be correct. It also tests that comments are properly ignored.

R1 1 2 1
R2 2 3 0.5
Cc 2 3 100
L1 3 4 10
V1 1 5 5
C1 2 5 1
C2 3 5 2
R3 4 5 0.25

; I2 5 4 3
V2 4 5 10

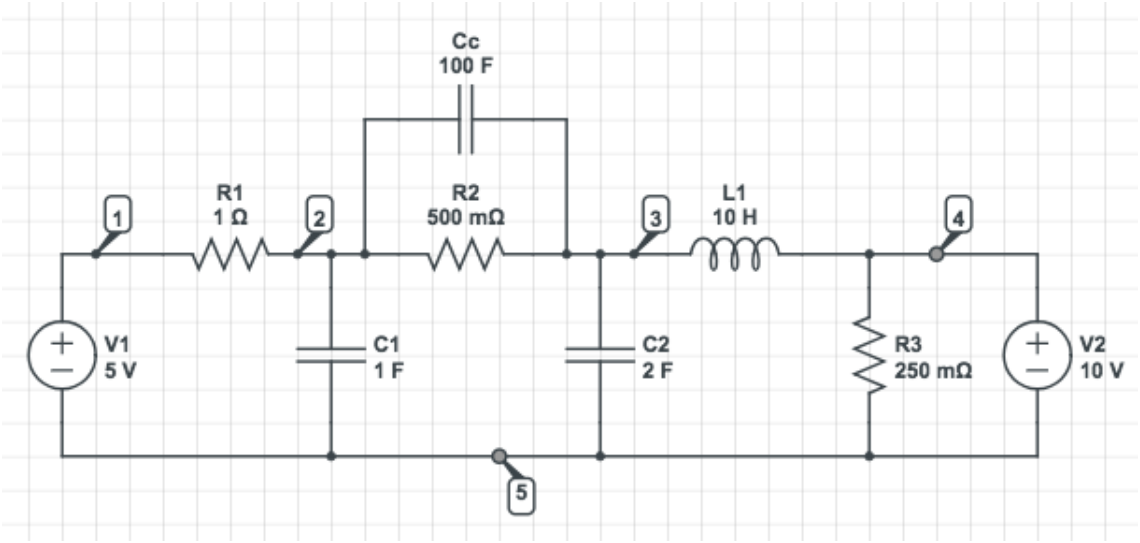

Figure 7.14: Example Circuit [4] for Testing the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 101.0 & -100.0 & 0 & 0 & 0 & 0 \\ 0 & -100.0 & 102.0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 10.0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & -1 \end{bmatrix} \tag{7.31}$$

$$\mathbf{G}: \begin{bmatrix} 1.0 & -1.0 & 0 & 0 & 0 & 1 & 0 \\ -1.0 & 3.0 & -2.0 & 0 & 0 & 0 & 0 \\ 0 & -2.0 & 2.0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 4.0 & -1 & 0 & -1 \\ 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}, \mathbf{L}: \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{7.32}$$

7.2.6 Example 5

The circuit in Figure 7.15 was used to test the functionality of a voltage-controlled current source element.

Vs up gnd 5000000u
R1 up mid 1k
R2 up mid 0.003M
R3 mid gnd 0.1M
C1 up hi 3p
R4 gnd lo 10000c
G1 hi lo up mid 1m

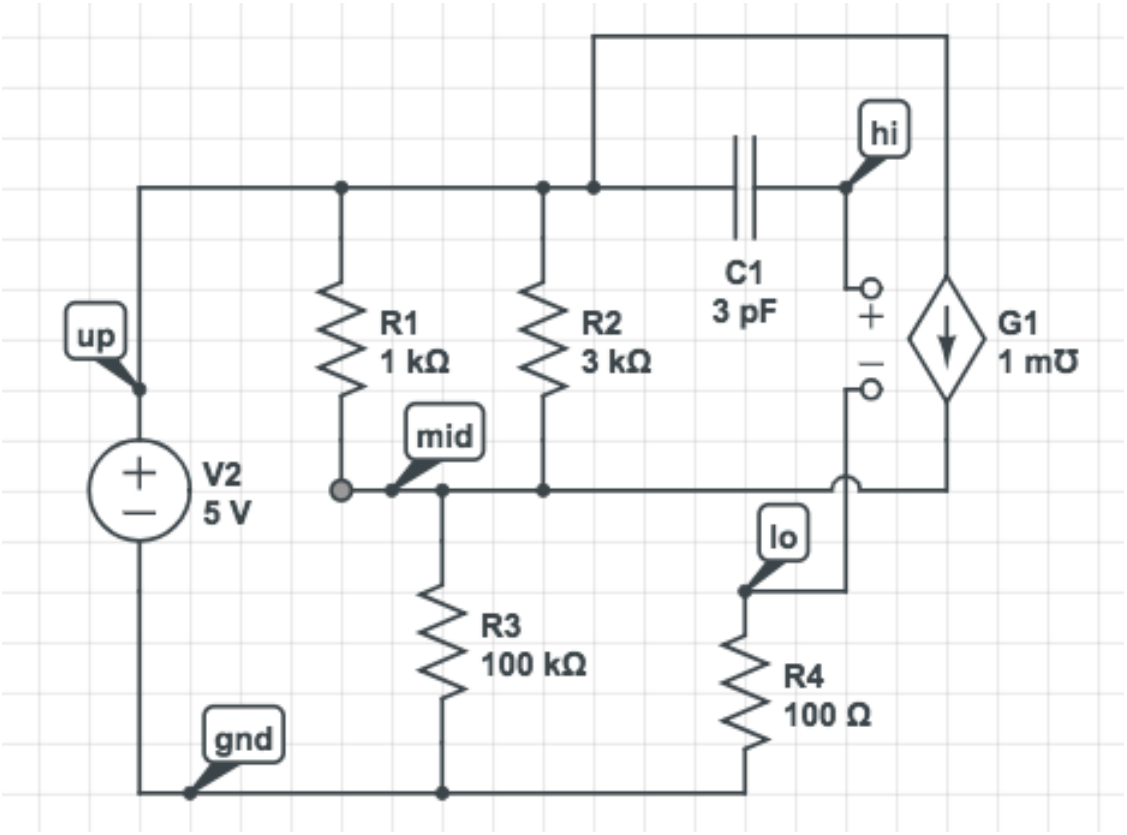

Figure 7.15: Example Circuit for Testing the Voltage-Controlled Current Source in the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 3e-12 & 0 & -3e-12 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -3e-12 & 0 & 3e-12 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & 0 \end{bmatrix} \tag{7.33}$$

$$\mathbf{G}: \begin{bmatrix} 0.0013333333 & -0.0013333333 & 0 & 0 & 1 & 0 \\ -0.0013333333 & 0.0013433333 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0.01 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 1000.0 \end{bmatrix}, \mathbf{L}^T: \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & 0 \end{bmatrix} \tag{7.34}$$

7.2.7 Example 6

The circuit in Figure 7.16 was used to test the functionality of a current-controlled current source element.

Vs a 0 5
R1 a b 1k
R2 b e 5k
Vm e 0 0
C1 b 0 1p
C2 b c 1f
R3 c d 1k
R4 d 0 5k
Fs c 0 Vm 0.1m

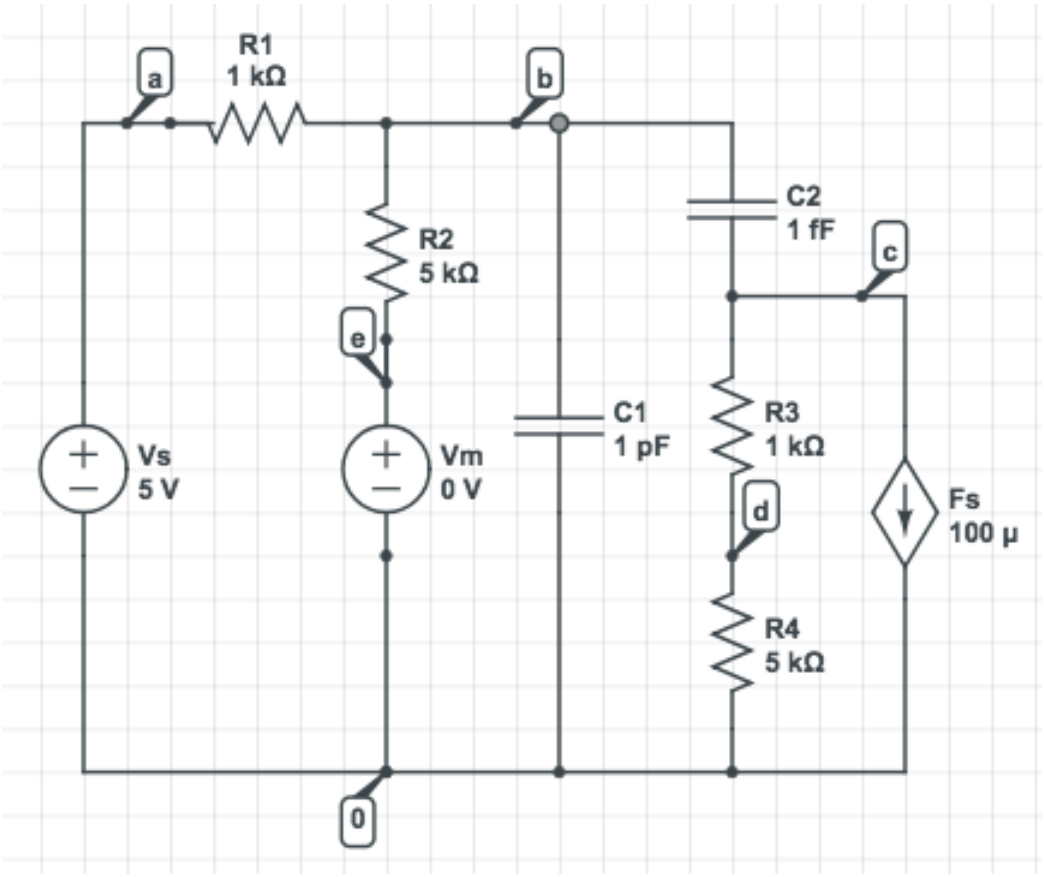

Figure 7.16: Example Circuit for Testing the Current-Controlled Current Source in the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1.001e-12 & 0 & -1e-15 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1e-15 & 0 & 1e-15 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{7.35}$$

$$\mathbf{G}: \begin{bmatrix} 0.001 & -0.001 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ -0.001 & 0.0012 & -0.0002 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -0.0002 & 0.0002 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0.001 & -0.001 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & -0.001 & 0.0012 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -0.0001 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{L} = \mathbf{B}^T \tag{7.36}$$

7.2.8 Example 7

The circuit in Figure 7.17 was used to test the functionality of a voltage-controlled voltage source element.

Vs up gnd 5000000u
R1 up mid 1k
R2 up mid 0.003M
R3 mid gnd 0.1M
C1 up hi 3p
R4 gnd lo 10000c
E1 hi lo up mid 1m

$$\mathbf{C}: \begin{bmatrix} 3e-12 & 0.0 & -3e-12 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ -3e-12 & 0.0 & 3e-12 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0.0 & 0.0 \\ 0.0 & 0.0 \\ 0.0 & 0.0 \\ 0.0 & 0.0 \\ -1.0 & 0.0 \\ 0.0 & 0.0 \end{bmatrix} \tag{7.37}$$

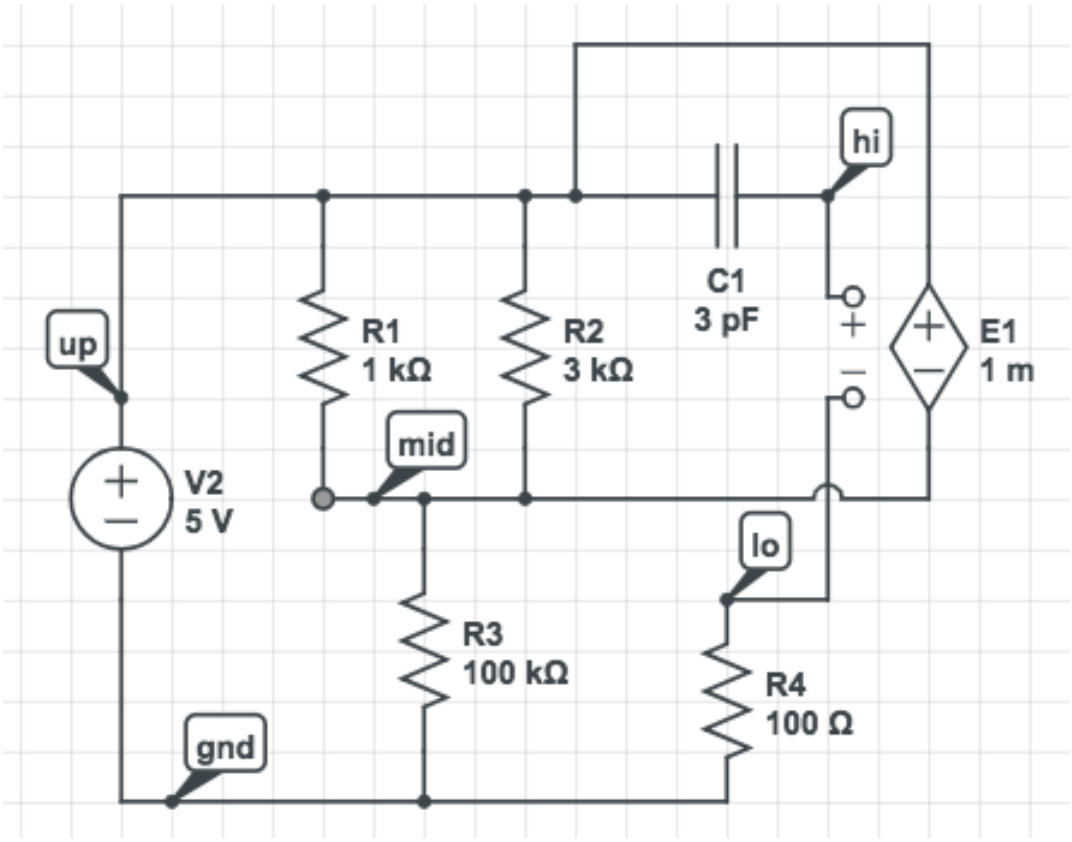

Figure 7.17: Example Circuit for Testing the Voltage-Controlled Coltage Source in the State-Space Formulation

$$\mathbf{G}: \begin{bmatrix} 0.0013333 & -0.0013333 & 0.0 & 0.0 & 1.0 & 0.0 \\ -0.0013333 & 0.0013433 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & -1.0 \\ 0.0 & 0.0 & 0.0 & 0.01 & 0.0 & 1.0 \\ -1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ 0.001 & -0.001 & -1.0 & 1.0 & 0.0 & 0.0 \end{bmatrix}, \mathbf{L} = \mathbf{B}^T \quad (7.38)$$

7.2.9 Example 8

The circuit in Figure 7.18 was used to test the functionality of a current-controlled voltage source element.

Vs a 0 5

R1 a b 1k

R2 b e 5k

Vm e 0 0

C1 b 0 1p
C2 b c 1f
R3 c d 1k
R4 d 0 5k
R5 f 0 1
Hs c f Vm 10k

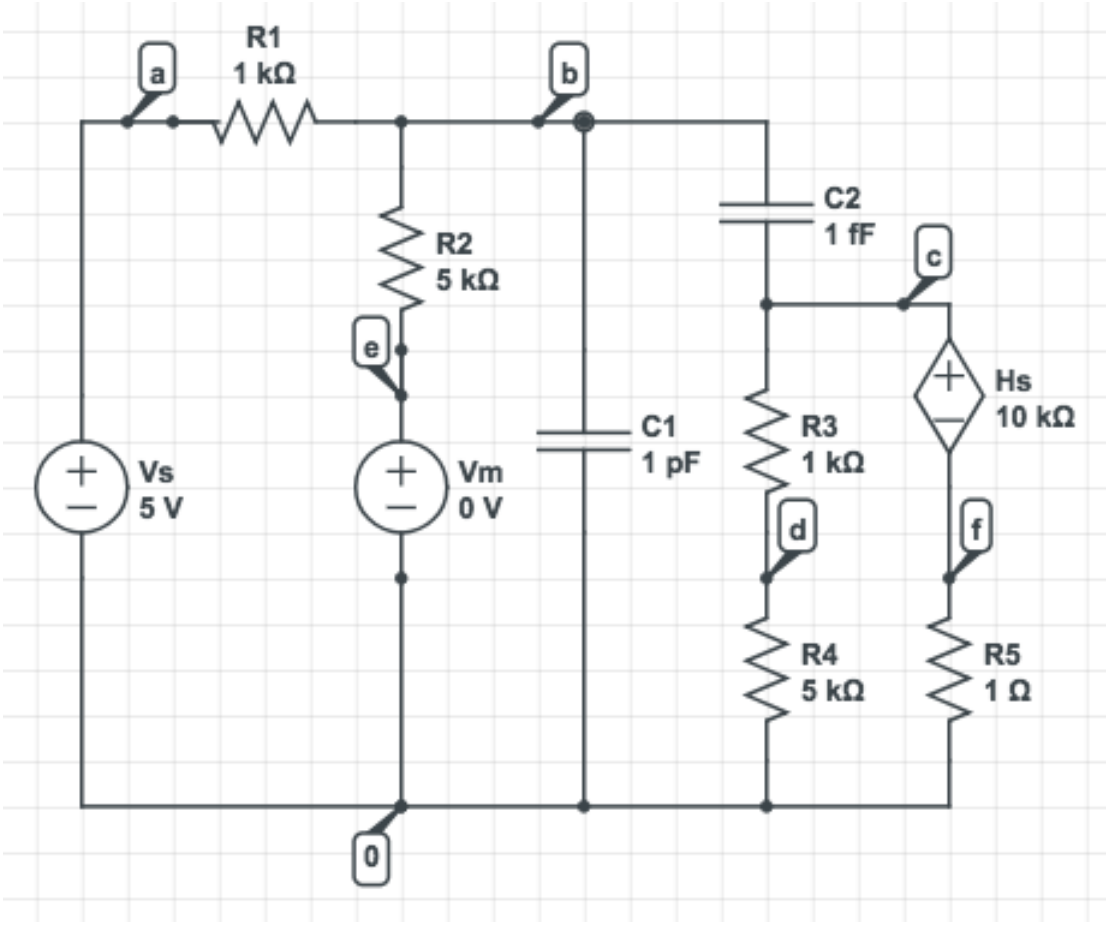

Figure 7.18: Example Circuit for Testing the Current-Controlled Voltage Source in the State-Space Formulation

$$\mathbf{C}: \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1.001e-12 & 0 & -1e-15 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1e-15 & 0 & 1e-15 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{B}: \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{7.39}$$

$$\mathbf{G}: \begin{bmatrix} 0.001 & -0.001 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ -0.001 & 0.0012 & -0.0002 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -0.0002 & 0.0002 & 0 & 0 & 0 & 0 & 1 & 0.0001 \\ 0 & 0 & 0 & 0.001 & -0.001 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -0.001 & 0.0012 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1.0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{L} = \mathbf{B}^T \tag{7.40}$$

CHAPTER 8

CONCLUSION

In this thesis, we have discussed how to generate the steady-state MNA formulation and State-Space formulation stamps of a given circuit from its netlist. The ability to generate these stamps is a critical step towards being able to compute the behavior of the circuit in an efficient manner. The stamp computation is broken up into two passes for both formulations. The first pass is used to determine the size of the stamp and some stamp-specific properties of the circuit such as the number of independent sources present. The second pass then fills in the values in the matrices based on the circuit elements and the formulation being used.

Having this program allows for the simple and automated analysis of multiple circuits and parameter settings. This would be dramatically more efficient than manually repeatedly modifying circuits slightly for each analysis that needs to be performed, and it would allow the user to leave the simulation to run and come back to a complete analysis. Further steps towards a fully functional version of this program, in addition to further improvements and enhancements that can be made to this code, can be found in Chapter 9.

CHAPTER 9

FUTURE WORK

9.1 Improve Efficiency

Currently in progress is the ability to analyze the circuit by defining matched ports. The idea behind this is as follows. Given a base white-box circuit, we want to understand the response of the circuit at different ports to various excitations at these ports. It would be very inefficient to recreate and recompile a netlist for each setup when the base circuit is the same for all these analyses. One solution to this is to create intermediate matrices that store the formulation of the base circuit and simply modify that for each desired ports-excitation combination. The ability to store this intermediate result as a text file and read it back into the program has already been implemented, as can be seen in the code in Appendix B. The full implementation of this tool still requires the implementation of a configuration file. Contained in this file would be the location of the intermediate result text files, the name of the Ground node in the circuit (if any), the input port(s) that describes the excitation(s) being provided to the circuit, the output port(s) where a measurement is desired to be made, a list of all other ports in the circuit that are neither an input nor an output, and the load impedance that is considered a "match" load for all ports.

As alluded to earlier, an additional commonly used component of a SPICE netlist is the subcircuit. It would be very beneficial to include its implementation for both steady-state MNA and State-Space formulations. This is an important next step beyond the code developed here, especially for the State-Space formulation example with ports from above, because the true benefit of the method comes from not having to recompute a stamp from an existing netlist. This difference is really only significant when recomputing the stamp takes significant time, implying that the circuit used to generate it

is very large. The vast majority of large circuits are broken up into combined subcircuits, making its implementation a very beneficial next step.

While we are considering the efficiency of generating the stamps for these circuits, it is easy to see that there is some inefficiency in the current process of parsing the netlist two times, especially in the cases we considered above where our netlists become very large or contain many subcircuits. This can be done by using matrices with the ability to dynamically add additional rows and columns. Alternatively, we can use a resizing scheme that doubles the size of our matrix every time we run out of space. As discussed in data structures courses, this method will on average result in a constant time (O(1)) addition to the runtime, which is better in the long term than doing a second pass which takes linear time (O(n)).

9.2 Additional Functionality

It would also be nice to be able to be able to stamp additional types of circuit elements beyond what is already included. Specifically, we would like to stamp components such as bipolar junction transistors (BJTs) (Qxxxxxxx), metal oxide semiconductor field-effect transistors (MOSFETs) (Mxxxxxxx), junction gate field-effect transistors (JFETs) (Jxxxxxxx), mutual inductors (Kxxxxxxx), voltage-controlled switches (Sxxxxxxx), and current controlled switches (Wxxxxxxx). Since these are nonlinear components, it is likely that many of these would require a substitution of an approximate model of the device, if at all possible in the first place.

Finally, it would be beneficial to develop a program to create a stamp of the transient MNA formulation for completeness. After completing the generation of all three stamp formulations from a SPICE netlist, the logical progression would then be to generate the same stamps from the Latency Insertion Method (LIM) description of the circuit. These would then all be usable to take a circuit and efficiently generate a stamp, which could then be used to compute the behavior of the circuit.

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