CHARACTERIZATION OF VARIOUS TYPES OF POWER AMPLIFIERS

BY

ZIJIAN LI

THESIS

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Adviser:

Professor José E. Schutt-Ainé

ABSTRACT

Over the years, the wireless communication market has experienced remarkable development since the first handheld phone introduced by Motorola. Nowadays, the smartphone is one of the most indispensable personal items, with a wide variety of applications that can benefit our daily life. Consequently, the thirst to achieve better wireless transceiving system design, with a low market cost, has gradually become the primary goal of modern RFIC manufacturers.

In all RF transceivers, the power amplifier plays a key role in driving the antenna on the transmitting end, while low-noise amplifier boosts the receiving end signal. Together these components account for the basic operation of a duplexed system. Among the various requirements in designing a power amplifier, PAE (power added efficiency) and linearity are the two most important characteristics. In the modern RF industry, engineers are sparing no effort to increase the PAE in order to increase the battery life; however, linearity requirements, such as ACLR for W-CDMA, E-UTRA for LTE, and ACPR for CDMA2K, must be obtained in order to achieve the basic power amplifier functionality. Detailed explanations will be provided in later sections. Other power amplifier design requirements and specifications also include gain, 2FO/3FO harmonic rejection, noise, stability, ruggedness, leakage power etc.

This thesis introduces the fundamental principles and knowledge of various types of power amplifiers and highlights their unique pros and cons among the different topologies. A high-efficiency, high-frequency switching mode power amplifier will be discussed mostly with regard to its design and measurement testing. Moreover, a conventional class E power amplifier output matching network will be designed using ADS (Advanced Design System) with the simulation results. Furthermore, basic power amplifier measurement will be performed using VNA, NVNA, and PSA.

To my grandfather Kuihe, for his forever trust.

ACKNOWLEDGMENTS

I am grateful to everyone who helped and supported me in the past five years of my university studies. I have been lectured by many famous professors during my undergraduate times, and actively involved in many researches as a graduate student. As I approach the end of my student life, I now realize this journey was arduous, but worthy and special. Thus, while completing this thesis, I would like to use this opportunity to mention all my supporters, both on stage and behind the scenes, with pride.

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LIST OF ABBREVIATIONS

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone System
BW	Bandwidth
CDMA	Code Division Multiple Access
CE	Circuit Envelope
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
E-UTRA	Evolved Universal Terrestrial Radio Access
EDGE	Enhanced Data Rates for GSM Evolution
ESG	Electrical Signal Generator
EVM	Error Vector Mode
FDM	Frequency Division Multiplexing
GPRS	General Packet Radio Service
GSM	Global System for Mobile communication
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HPHP	High-Pass High-Pass

IBIS	Input/output Buffer Information Specification
IC	Integrated Circuit
IEEE	The Institute of Electrical and Electronics Engineers
IIP	Input Interception Point
IMD	Inter-Modulation Distortion
LNA	Low-Noise Amplifier
LPLP	Low-Pass Low-Pass
LTE	Long Term Evaluation
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSG	Mixed Signal Generator
NMOS	N-type Metal-Oxide-Semiconductor
NMT	Nordic Mobile Telephone
NTT	Nippon Telegraph and Telephone
NVNA	Nonlinear Vector Network Analyzer
OFDM	Orthogonal Frequency Division Multiplexing
OIP	Output Interception Point
PA	Power Amplifier
PAE	Power Added Efficiency
PM	Phase Modulation
PNA-X	Power Network Analyzer - X-parameters
PSA	Power Spectrum Analyzer
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
TACS	Total Access Communication System
TD-SCDMA	Time Division - Synchronous Code Division Multiple Access

TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TTL	Transistor-Transistor Logic
VNA	Vector Network Analyzer
W-CDMA	Wideband Code Division Multiple Access
ZVZCS	Zero-Voltage Zero-Current Switching

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Over the years, the wireless communication market has experienced rapid development since the first mobile phone introduced by Motorola in 1973. These giant handheld phones weighed more than 1 kg and required a long charging time and short battery life. In 1980, AMPS introduced the first generation analog cellular system, which facilitated the widespread use of mobile (cellular) phones. People did not start using the word "smartphone" until 2007 when Apple introduced the iPhone 2G (second generation). However, the first genuine smartphone product dates to 1992 when IBM introduced the Simon Personal Communicator. On this machine, individuals could receive and send emails as well as use basic third party applications, such as the snake game. With the steady increase in the number of people using cellular phones, the demand for newer applications, longer battery life and higher data rates has long posed opportunities and challenges in wireless communication.

In all RF transceivers, the power amplifier plays a key role in driving the antenna on the transmitting end. An amplifier operates by keeping the period of the output waveform the same as that of the input, but with a greater magnitude as shown in Figure 1.1. In conventional amplifier designs, input always targets a relatively small signal, i.e. 1 mW or less. A power amplifier, similar to a conventional amplifier, functions by raising the power level of the input signal, but aims to deliver large power at the output, i.e. usually around 1 W.

A large-signal amplifier, or power amplifier, requires strong transistors to withstand amplification without blowing out. In most cases, a heavily doped emitter/source and a thicker base/gate are imperative to power transistor

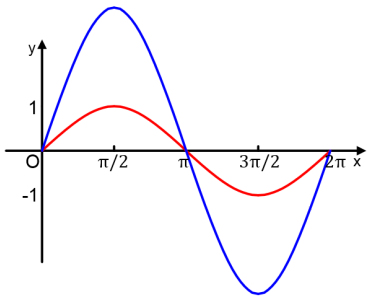


Figure 1.1: Input (Red) and Output (Blue) Waveforms of an Amplifier

designs [1]. In modern technology, commercial products tend to use the compound III-V direct bandgap element gallium arsenide (GaAs) rather than silicon due to its lower temperature coefficient at microwave frequencies. Due to the power hungry nature of power amplifiers, transistors are sized small in order to minimize power consumption and save battery life. Since the battery accounts for 90% of the area of a modern smartphone, it is important to shrink the size of chips, but keep their original functionality. For example, linearity requirements, a key requirement to measure the non-linear effect, can be violated with the scaling trend of the chips. To remedy this, techniques such as adding a boost-stage in the amplifier are frequently used. Other high-level power amplifier design parameters, such as stability and ruggedness, are influenced by the scaling trend as well. Thus a design process would be long and tedious, but meaningful.

The goal of this thesis is to bridge the gap between researcher and engineer by introducing the fundamental principles and knowledge of various types of power amplifiers and highlighting their unique pros and cons among the different topologies. Class E high-efficiency switching mode power amplifiers will be heavily discussed as a reference to demonstrate the non-linear and power hungry nature of power amplifiers. Basic lab measurement will be performed on a commercial power amplifier to show the agreement between simulation and measurement results.

1.2 Scope of this Thesis

This thesis is intended to both introduce basic design techniques of power amplifiers and serve as a future reference for students who would like to pursue research in the field of radio-frequency integrated circuits (RFICs).

1. Chapter 1 introduces a brief history and background of the main topic of this thesis.

2. Chapter 2 provides an overview of various types/classes of linear power amplifiers, including individual classic building blocks, design figures of merit and drawbacks under modern technology.

3. Chapter 3 presents a detailed description of widely popular power amplifiers used in industry nowadays – the class D, class E and class F switching mode power amplifier.

4. Chapter 4 provides an example of output matching network design by showing the simulation result on Advance Design System (ADS) software.

5. Chapter 5 covers the fundamental theory in power amplifier lab measurement, such as adjacent channel leakage ratio (ACPR), and provides an organized procedure for setting up the lab environment for basic power amplifier measurement.

6. Chapters 6-8 describe the lab results using vector network analyzer (VNA), power spectrum analyzer (PSA) and X-parameters network analyzer (PNA-X) on two commercial power amplifiers and show the agreement between lab measurements and original theoretical assumptions made in the previous chapters.

7. Chapter 9 concludes the thesis with a general evaluation of all research work presented in two years of master's studies, together with a brief discussion of future work in RFIC design.

8. Finally, the Appendix provides extended information on other research and academy works, such as the ECE451 lab manual, not mentioned in this thesis, but meant to be useful even if only a little, as a guide for future graduate students.

1.3 History of RFIC

Over the years, from the great James Clark Maxwell to Alexandre Graham Bell, from John Bardeen to Gordon Moore, countless scientists made decisive contributions to the development of wireless communication. A brief history of radio frequency and integrated circuits will be presented in this section.

The era of electromagnetics started with four famous equations – the Faraday/Maxwell Equations. In 1864, James Clark Maxwell and Michael Faraday explained electrical and magnetic phenomena the propagation of fields and waves traveling at the speed of light [2]. They expanded the theory to other types of radiation, such as radio, television, X-rays, lasers, etc. [2]. In 1876, Bell first discovered that "It would be possible to transmit sounds of any sort if we could only occasion a variation in the intensity of your current exactly like that occurring in the density of the air while a given sound is made" and patented the first telephone which is considered the first application of Maxwell's equations in the RF field [3].

In 1980, the first generation (1G) of wireless telephone technology was marked by Motorola's initial mobile phone product, DynaTAC 8000X. With this invention, telephones finally reached the era of "having no wires" and calls could be made in one country through the analog signal (up to 2.4 kbps). A typical 1G analog system included NTT, NMT, TACS, and AMPS [4]. However, drawbacks of 1G technology, such as poor voice quality and battery life, forced engineers to improve the technology. Only one year later, the second generation (2G) was first launched in Finland with a tremendous increase in data transfer rate, 64 kbps, which enabled features such as text and picture messages by transferring through digital signals. A typical 2G digital system included GSM, EDGE, and GPRS [4]. In the 2000s, the third generation (3G) brought the data speed to 2 Mbps with the advent of what is nowadays commonly referred to as the "smartphone" on which web-based applications are accessible. 3G can be treated as the industrial revolution of wireless communication giving people the benefits of the high speed web, more secure video conferencing, large emails and fantastic 3D games. A typical 3G system included W-CDMA, CDMA2K, and TD-SCDMA [4]. With the demand for higher data rate and signal bandwidth, the fourth generation entered the stage in the 2010s [5]. Table 1.1 illustrates the improvement of 4G over 3G technology. The word "MAGIC" points to 4G technology

Table 1.1: Properties of 3G and 4G Wireless Technology [5]

Technology	3rd Generation	4th Generation
Data Rate	3MB/s	100MB/s
Bandwidth	5-20MHz	100MHz
Operating Frequency	1-2GHz	1-7.5GHz
Data Speed	6Mbps	15Mbps

and stands for Mobile mutimedia, Any-where, Global mobility solutions, Integrated wireless and Customized services. A typical 4G system included LTE [4]. Figure 1.2 shows the evolution of wireless phones from 1G to 5G technologies. 5G is still in progress and will be judged by future researchers!

Figure 1.2: Evolution of 1G to 5G Wireless Technology [6]

Clearly, wireless communication has undergone striking development since 1864. However, this remarkable development would not have been possible without transistors.

John Bardeen, together with Walter Brattain and William Shockley, was awarded the Nobel Physics Prize for inventing the initial point-contact transistor in December 1947. Shockley invented the junction transistor one month later, which greatly benefited companies such as Texas Instruments and SONY, while giving birth to Fairchild Semiconductor and, later, Intel [7]. In 1958, Robert Noyce, along with Jack Kilby at Texas Instruments, introduced the first integrated-circuit logic gates – Fairchild Micrologic family [8] and this truly successful IC logic design became the pioneer of the later TTL family [9]. With the advent of IC logic gates, more transistors

had been integrated on a single die. In the 1960s, Gordan Moore predicted that the number of transistors that could be integrated on one die would increase exponentially over time. This prediction was so acute that the real number followed closely [10]. Figure 1.3 shows the year of introduction and the number of transistors per chip, clearly demonstrating the exponential increase predicted by Moore. Nowadays, Intel, the leading company in silicon research, already employs 7,200,000,000 transistors with vast scaling of CMOS transistor technology on its newly introduced CPU – 22-core Xeon Broadwell-E5 [11].

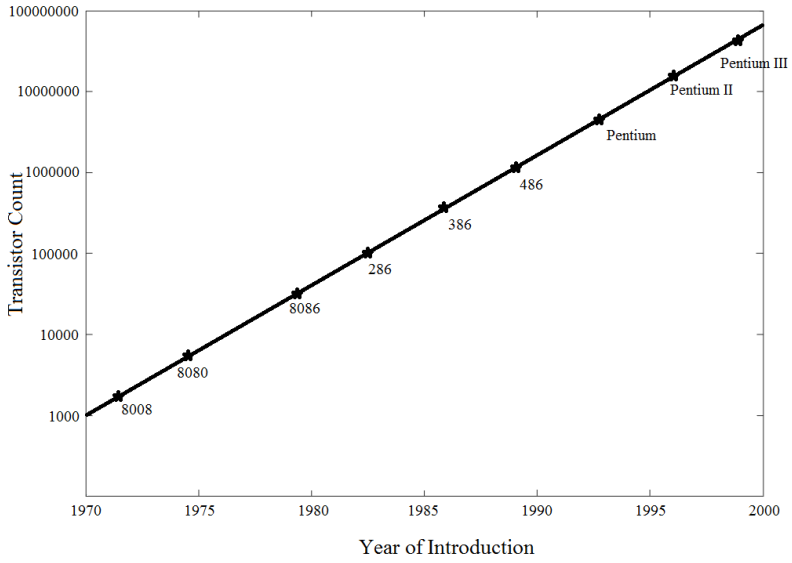


Figure 1.3: Evolution of Transistor Count on Intel Microprocessor [12]

CHAPTER 2

RF POWER AMPLIFIER OVERVIEW

2.1 The MOSFET Transistor

The metal-oxide-semiconductor field-effect transistor (MOSFET) has long been the most widely used physical/electronic device in modern technology. Over the years, countless pioneer scientists and researchers have devoted tremendous time to find the relationships among the four magical terminals within a MOSFET. This section intends to introduce the basic static and dynamic behavior of a MOSFET.

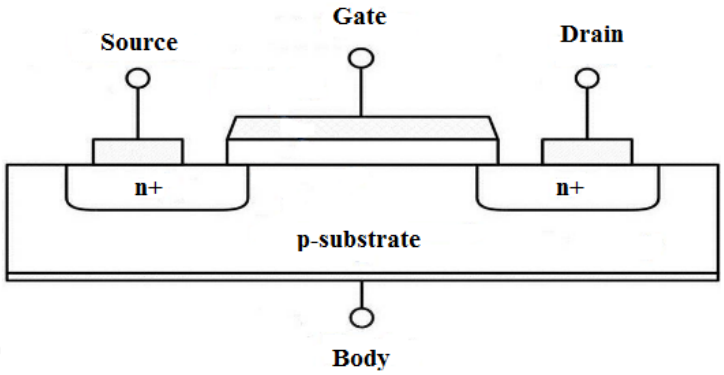


Figure 2.1: Cross Section of a MOSFET

Figure 2.1 shows the cross section view of an n-type MOSFET (NMOS). Similarly, PMOS is a p-type MOSFET with the same terminal names but switched doping substrate. In this chapter, NMOS will be used to demonstrate the MOS behaviors since an n-substrate can be easily made from p-substrate but not the reverse. The four terminals of a MOSFET are the gate, source, drain, and body (bulk). Both source and drain terminals are made from metal materials, whereas the gate terminal is made from polysilicon material. Source and drain terminals take a naturally symmetric shape and

form into a PN junction under reverse bias from external devices [13]. This external voltage can shape the channel, which connects the source and drain terminals, to provide different regions of operation in MOSFET applications.

2.1.1 Static Behavior

Typical MOS transistor behaviors under static conditions include change of threshold voltage under body effect, various regions of operation under reversed bias external source, I-V characteristics on drain current, and leakage current under sub-threshold conditions.

Threshold Voltage

Apart from applying any knowledge from an engineering perspective, the word "threshold" means a level, point, or value above which something is true or will take place and below which it is not or will not [14]. Likewise in electrical engineering, the threshold voltage defines the point where a MOS device can be turned on; in other words, current will flow through source and drain terminal when external bias exceeds threshold voltage. In IC design, ON state refers to superthreshold region when $|V_{GS}| \geq |V_t|$, and OFF state points to subthreshold region when $|V_{GS}| \leq |V_t|$. Figure 2.2 shows the threshold voltage on a simple MOSFET I-V curve. The expression for the

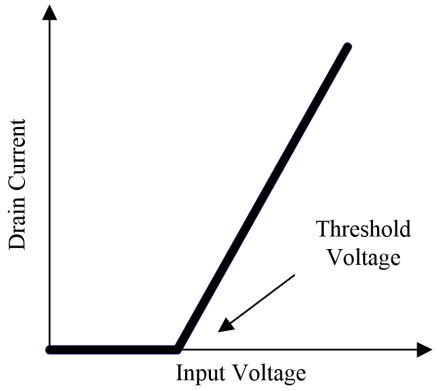


Figure 2.2: Simple MOSFET I-V Curve

threshold voltage V_t under body-biasing condition is

$$V_t = V_{t0} + \gamma(\sqrt{|-2\Psi_F + V_{SB}|} - \sqrt{|-2\Psi_F|}) \tag{2.1}$$

The parameter V_{t0} is called zero bias threshold voltage, which is equal to V_t under zero body-bias. γ is called body-effect coefficient and it only changes with MOS material. Ψ_F refers to body potential and is fixed with technology. Thus, from the equation, by controlling all other fixed parameters, threshold voltage V_t gradually increases with the increase in body bias V_{SB}.

Regions of Operation

Four main regions of operation have been detected in MOSFET transistors, namely cut-off, resistive, saturation, and velocity saturation. As stated in the last section, when $|V_{GS}| \leq |V_t|$ the MOSFET is in the subthreshold (cut-off) region in which no current flows through the transistor. Besides cut-off, the other three regions all fall into the category of superthreshold conditions, in which $|V_{GS}| \geq |V_t|$.

In cut-off region, MOSFET is said to be in OFF state. However, in a real scenario, a MOSFET can never fully turn off because a tiny leakage current flows through the transistor. This can be a major problem in modern IC designs: leakage current leads to increased power consumption when the transistor is supposed to dissipate zero power. The ratio between ON state current and OFF state leakage current is defined by

$$\frac{I_{on}}{I_{off,leak}} = 10^{\frac{|V_t|}{S}} \tag{2.2}$$

where

$$S = \frac{nkT}{q}\ln(10) \tag{2.3}$$

This ratio is a good measure of how leaky the transistor is under subthreshold conditions. A good number for this ratio can be more than 10^6.

Assume now that the input voltage increased above the threshold point, and a small DC source is applied to the drain terminal, but keep $|V_{GS}| > |V_{DS}|$. This will cause a current flow from drain to source and the MOSFET will behave as a tunable resistor. This phenomenon is commonly called the MOSFET resistive region of operation. This current can be determined by

$$I_{D,resistive} = k_n{}'\frac{W}{L}[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.4}$$

where $k_n{}'$ relates to the process transconductance parameter and is determined by the technology. In the resistive region, drain current is proportional to V_{DS} and increases on a logarithmic scale.

As V_{DS} keeps increasing until it reaches the value of input voltage $|V_{GS}|$, the MOSFET moves to the next level, which is the saturation region of operation. In this region, the MOSFET behaves as a constant current source in which the current only changes with the change of $|V_{GS}|$, not V_{DS}. Often this is called a diode-type device. The expression for the current in this region is

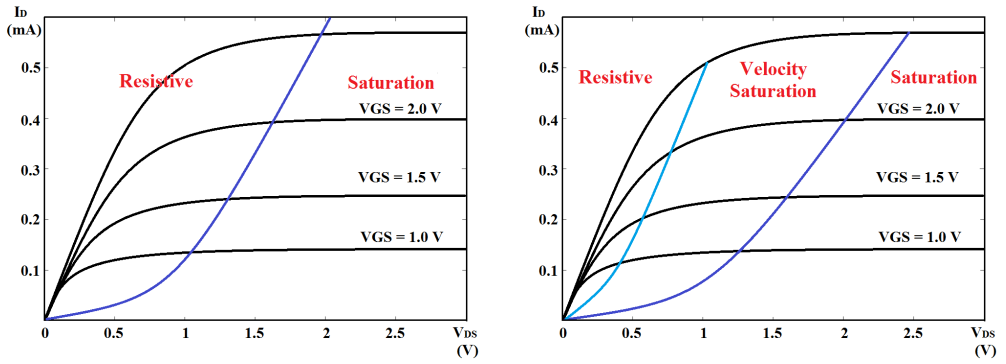
$$I_{D,saturation} = \frac{1}{2} k_n{}' \frac{W}{L} (V_{GS} - V_t)^2 \tag{2.5}$$

$V_{GS} - V_t$ is commonly referred to as the overdrive voltage of a transistor, which is a key parameter in amplifier design. Velocity saturation is closely related to saturation region; the only difference lies in the short channel effect. In particular, with a strong electrical field along the channel, electrons tend to move faster and will rapidly saturate due to the scattering effect. Similarly to the saturation region, a MOSFET under velocity saturation also behaves as a current source, but with slightly different current values.

$$I_{D,vel.saturation} = k_n{}' \frac{W}{L} [(V_{GS} - V_t) V_{DSAT} - \frac{V_{DSAT}^2}{2}] \tag{2.6}$$

Drain Current vs. Voltage

To best understand the I-V characteristic of a MOSFET transistor under various regions of operation, a drain current vs. voltage chart needs to be introduced. Figures 2.3a and 2.3b illustrate the IV characteristics of a MOSFET under long and short channel effects. Clearly shown in (b) is that the MOSFET first reaches velocity saturation before jumping into saturation due to the scattering effect of electrons under strong electrical field.



(a) Long-channel transistor (b) Short-channel transistor

Figure 2.3: IV Characteristics of Long and Short Channel Effect MOSFET [12]

2.1.2 Dynamic Behavior

Typical dynamic behaviors include propagation delay, which is the charging and discharging time of MOSFET capacitance when a sudden rise/fall happens in the input signals, and dynamic power consumption, which is the unwanted energy consumed during this charging and discharging time. Propagation delay, most of the time, can negatively influence the entire network, e.g. timing issues. This section aims to discuss the behavior of MOSFET intrinsic capacitances and how they affect the propagation delays.

MOSFET Intrinsic Capacitance

MOSFET intrinsic capacitances mainly include three types – structural, junction and channel capacitance. In Figure 2.4, structural capacitance covers C_{GD} and C_{GS}, which is formed by the oxide overlap between G, S and D terminals; junction capacitance covers C_{DB} and C_{SB} and results from junction channels and sidewalls; channel capacitance relates to the capacitance through the entire MOSFET channel from gate to body terminal, C_{GB}. To minimize all five parasitic/intrinsic capacitances is always the goal of every process engineer.

$$C_{int} = C_{GD} + C_{GS} + C_{SB} + C_{DB} + C_{GB} \tag{2.7}$$

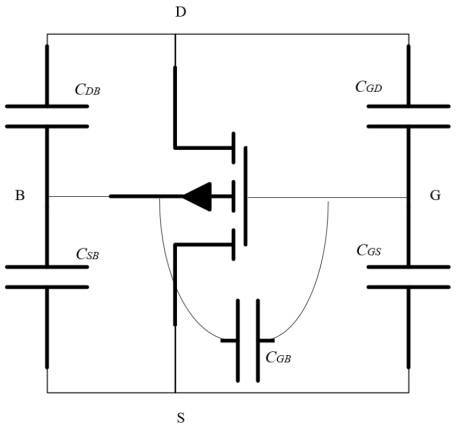


Figure 2.4: MOSFET Capacitance Model

Propagation Delay

Propagation delay is a measure of the time it takes a digital signal to travel from input to output. In MOSFET transistors, it is measured from the half point of the input waveform to the half point of the output waveform during transition [15]. Figure 2.5 gives an example timing analysis in a MOSFET.

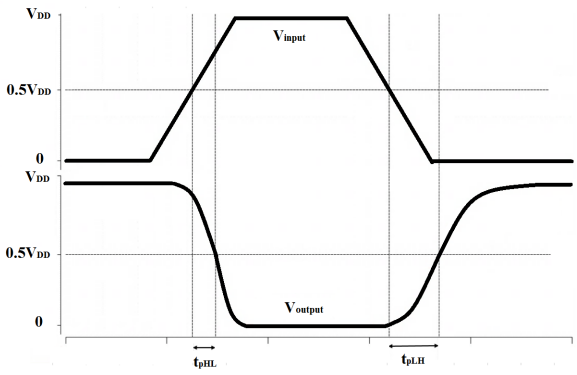


Figure 2.5: Propagation Delay

The expression for propagation delay depends on both the intrinsic capacitance and the supply voltage.

$$t_p = \frac{C_{int}\frac{V_{DD}}{2}}{(\frac{W}{L})I_{DSAT}} \tag{2.8}$$

2.2 Power Amplifier Basics

The power amplifier (PA) has long been considered the most power hungry component in wireless communication systems. A standard PA can consume up to 1 W at its output stage, not to mention more vigorous PAs which can possibly consume 10 W to 100 W. As discussed in previous sections, a thick and strong MOSFET transistor is highly recommended in designing PAs; i.e., a sufficiently thick collector or drain area is needed. However, new challenges arise with large scaling of the transistor collector area, such as PA efficiency and non-linear effects. In this section, fundamentals of PA properties and design parameters will be introduced.

2.2.1 Output Power and Gain

The PA is the key component in the transmission chain of any kind wireless transceiver in a radio system. It is the final amplification stage before the signal is transmitted to the antenna. A block diagram of a superheterodyne full-duplexer transceiver system is shown in Figure B.1 in Appendix B (isolator is there to protect the circuit). In order to provide sufficient output power to overcome the system and transmission loss, high output power is strongly recommended (usually 1 W or more) [16].

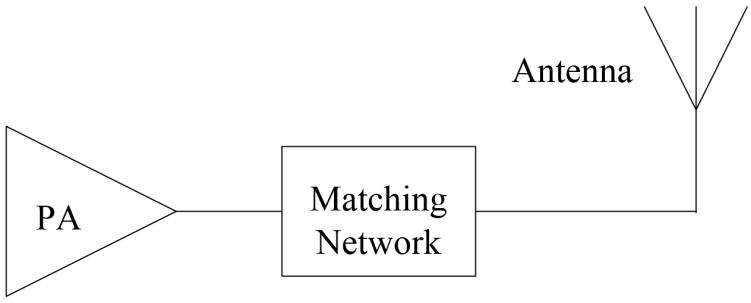


Figure 2.6: Simple PA System

Figure 2.6 shows a simple PA system with an amplifier, an output matching network and an antenna. As a matter of fact, most antennas are designed at 50 Ω. However, to reach 1 W output with a 50 Ω load (antenna), a voltage swing of around 15 V is required. A typical supply voltage falls under 5 V, which means a voltage swing of three times the supply voltage is extremely

hard to achieve. An output matching network would best solve this issue by matching the 50 Ω antenna resistance to a relatively lower value, say 5 Ω. Now the PA will see a 5 Ω load at its output, and a voltage swing of around 1.5 V would easily reach the power requirement. In modern PA output matching network designs, the single/double stage L-C matching technique is widely used. The expressions to calculate the output power are in equations (2.9) and (2.10), and for a sinusoidal wave signal, $V_{rms} = \frac{V_{peak}}{\sqrt{2}}$.

$$P_{out} = \frac{V_{out,rms}^2}{R_{antenna}} \tag{2.9}$$

$$P_{collector} = \frac{V_{collector,rms}^2}{R_{matching}} \tag{2.10}$$

If a lossless matching network is provided, P_{out} should equal to $P_{collector}$. However, in real circuits, all resistive and reactive electronic components are lossy and a loss around 1 dB will be added to the conventional matching network.

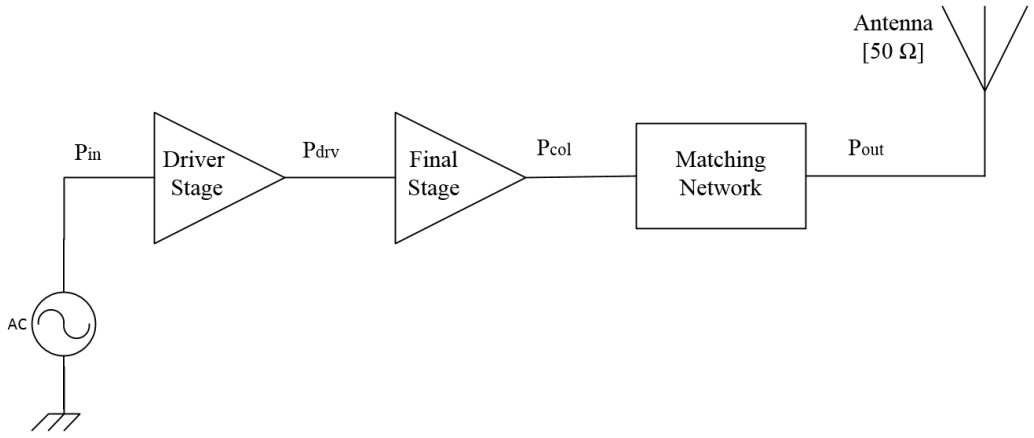


Figure 2.7: Two-Stage PA System

Figure 2.7 shows a conventional two-stage PA with a driver and a final stage. Each stage has its own power gain and the summation of all stages can derive the overall gain. Also, the overall gain can be expressed by taking the ratio of the output power and the input power and converting to decibels.

$$G_{drv} = 10\log(\frac{P_{drv}}{P_{in}}) \quad (2.11)$$

$$G_{col} = 10\log(\frac{P_{col}}{P_{drv}}) \quad (2.12)$$

$$G_{matching} = 10\log(\frac{P_{out}}{P_{col}}) \quad (2.13)$$

$$G_{overall} = G_{drv} + G_{col} + G_{matching} \quad (2.14)$$

$$G_{overall} = 10\log(\frac{P_{out}}{P_{in}}) \quad (2.15)$$

2.2.2 Efficiency

A main issue with current smartphones is short battery life. Since the PA can arguably be the most power consuming component in a wireless phone, to increase its efficiency seems crucial. For example, a conventional class A PA has an efficiency of up to 50%. To utilize 1 W of output power, the battery needs to burn at least 2 W. However, with a better class E design, the efficiency can go up to 80%; then only 1.25 W is burned. Thus a good engineer always focuses on increase the PA efficiency when the basic functionality is achieved.

In power amplifier designs, efficiency is not widely characterized in the usual way, which is taking the ratio of output power to DC supply power, i.e. $\eta = \frac{P_{out}}{P_{dc}}$. Power added efficiency (PAE) is introduced to characterize the system, since some of the design may require low gain but high input power [17]. The expression for PAE is

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad (2.16)$$

PAE is a key parameter of PA designs and is considered the sole efficiency of the system, regardless of gain. A PAE above 45% indicates a well-designed PA.

2.2.3 Linearity

Another important PA design parameter is linearity, which can be classified in many ways. The point A in Figure 2.8 is called the 1 dB compression point

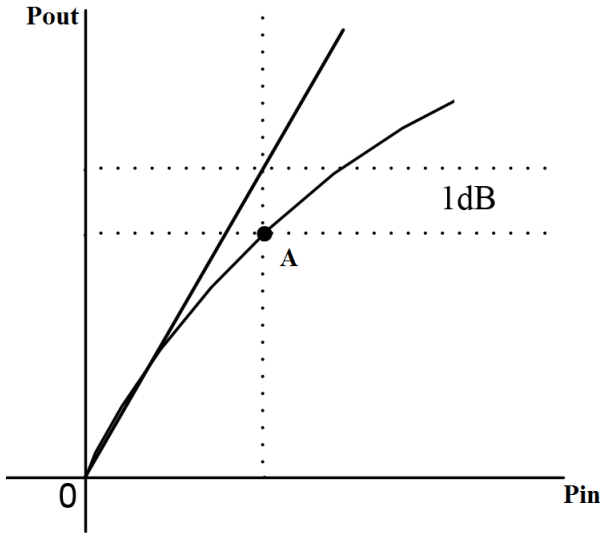


Figure 2.8: 1 dB Compression Point of a Non-linear Network

which can best characterize the nonlinearity of a network with single-tone input. At low input power, PA tends to behave linearly as the ideal line. With the increase of power, nonlinear effects due to amplitude compression dominate PA performance. This phenomenon can be best explained in the following.

Consider a PA with input signal of $V_{in}(t) = a_1 \cos \omega_1 t$ with three nonlinear power series terms of $P = k_1 V_{in} + k_2 {V_{in}}^2 + k_3 {V_{in}}^3$. Output signal can be expressed as

$$V_{out}(t) = k_1 a_1 \cos \omega_1 t + k_2 {a_1}^2 \cos^2 \omega_1 t + k_3 {a_1}^3 \cos^3 \omega_1 t \tag{2.17}$$

Using trig identities, the output signal can be written as

$$V_{out}(t) = \frac{1}{2} k_2 {a_1}^2 + k_1 a_1 (1 + \frac{3}{4} \frac{k_3}{k_1} {a_1}^2) \cos \omega_1 t + ... \tag{2.18}$$

The term $k_1 a_1 (1 + \frac{3}{4} \frac{k_3}{k_1} {a_1}^2)$ points to the amplitude of the fundamental harmonic of the PA output signal. Here, $1 + \frac{3}{4} \frac{k_3}{k_1} {a_1}^2$ is the effective compression term of the fundamental harmonic of the output signal caused by nonlinearity

[18].

Similar to the 1 dB compression point, IIP3 point can help to characterize nonlinearity of a two-tone input PA network. In real life measurement, the adjacent channel leakage/power ratio (ACLR/ACPR) is often used to measure the PA linearity. Detailed measurement theory will be introduced in Chapter 5.

2.3 Class A Amplifier

It is universally acknowledged that the class A amplifier, also called the linear amplifier, is the most basic amplifier. It is widely assumed that the class A amplifier is by no means linear. In fact, many authors have introduced the non-linear nature of the class A amplifier [16],[17],[19]. It is safe to say that a class A amplifier is not *fully* linear, but rather *highly* linear.

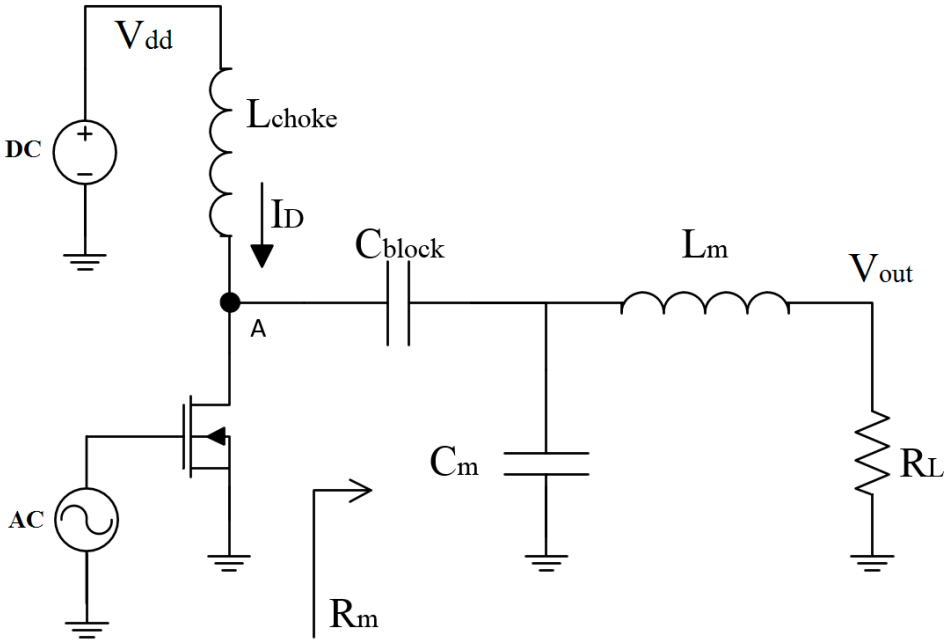


Figure 2.9: Class A Power Amplifier

Figure 2.9 illustrates a single-stage class A PA with 1 section of LC output matching network. DC represents the supply voltage (commonly referred to as V_{dd}) and AC defines the input signal (usually a swing from -10 to 0 dBm).

RF choke is made from inductance in order to produce a voltage swing that is twice the supply voltage. A DC blocking capacitor lies between the collector output and matching network input. C_m and L_m are matching components, which differ from design to design. This single section LC matching network can provide a large bandwidth but limited matching range. Point A defines the output of the transistor. R_m is equivalent input resistance after the matching network.

Supposing a regular input signal and a normal gain are provided to the PA, efficiency can be calculated directly from P_{out} and P_{dc} (no need to use PAE). P_{dc} should be the same as the power consumed through the inductor.

$$P_{dc} = \frac{{V_{dd}}^2}{R_m} \tag{2.19}$$

Since the choke inductor can provide twice the voltage to point A, then P_A can be calculated by

$$P_A = \frac{(V_{dd}/\sqrt{2})^2}{R_m} \tag{2.20}$$

Assuming the output matching network is lossless, then

$$P_A = P_{out} \tag{2.21}$$

Lastly, the efficiency is

$$\eta = \frac{P_{out}}{P_{dc}} = 50\% \tag{2.22}$$

Fifty percent of efficiency means that in order to deliver 1 W to the output stage, 2 W must be burned from the battery! Not to mention the assumption of a lossless matching network, which is never true in real life circuit design. The reason for low efficiency in a class A PA is that the transistor is always on and never stops operating, which means a conduction angle of 360°. Conduction angle is defined as the time percentage of the input signal when the transistor is in ON state, and it is a number between 0° and 360° (2π). Figure 2.10 shows the voltage and current waveforms of a typical class A PA. As shown, the transistor never shuts off since current and voltage are always above 0. Due to this "always on" property, the class A PA produces a large amount of heat from constantly carrying the current. If the heat is not sinked properly, the PA and the supply source may be damaged. Therefore, more efficient amplifier classes have been developed to overcome this

drawback.

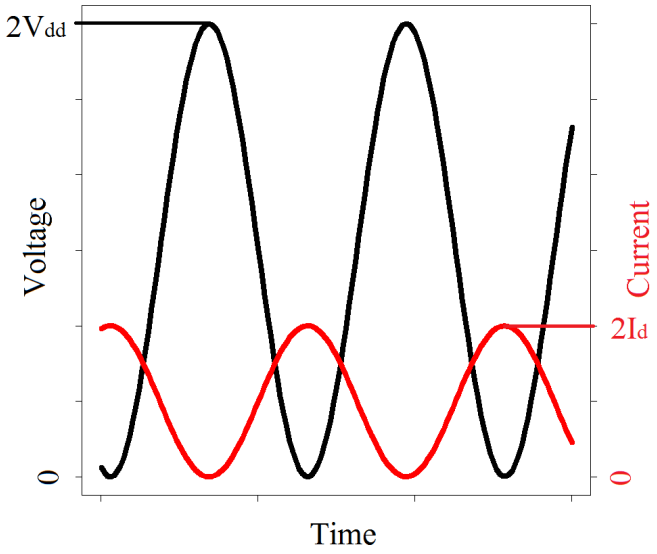


Figure 2.10: Voltage and Current Waveforms for Class A PA

2.4 Other Linear Amplifiers

Other types of linear power amplifiers include class B, class AB, and class C. They all serve as solutions to the low efficiency issue in the class A PA. Table 2.1 shows the differences among four major types of linear PA. Detailed explanation will be given in this section.

Table 2.1: Linear Power Amplifier Performance Comparison

types	efficiency (max)	conduction angle
class A	50%	360°
class B	79%	180°
class AB	50-79%	180°-360°
class C	<100%	> 0°

2.4.1 Class B Amplifier

Class B PA is designed similar to class A, but the conduction angle is decreased from 360° to 180°, which means the amplifier is on only half the

time. In most cases this is achieved by a push-pull structure (Figure 2.11). In push-pull structure, each transistor is required to shut off for half of the period, thereby achieving a higher efficiency by reducing the idle power loss as in class A PA.

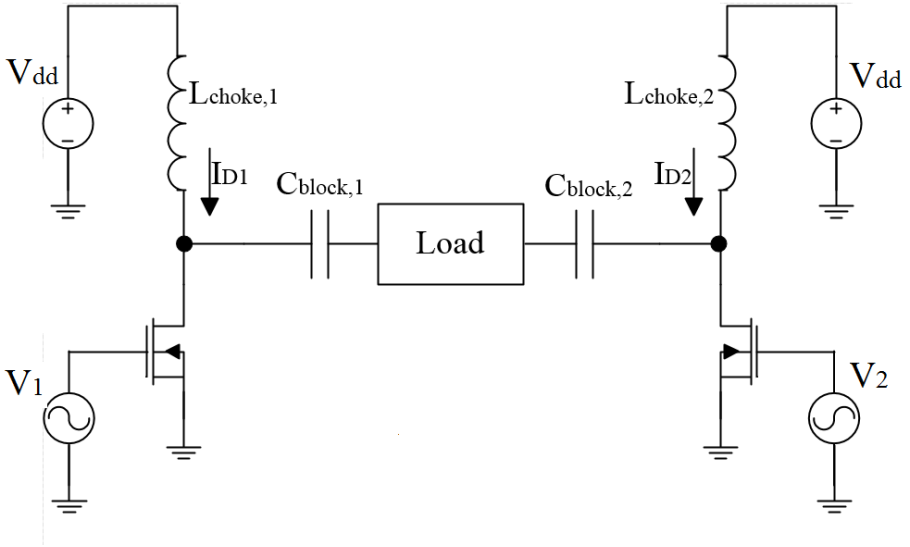


Figure 2.11: Push-Pull Class B Power Amplifier

Efficiency calculation for class B PA resembles that for class A. The only difference is in the P_{dc} calculation. This is easily explained since each transistor turns on alternatively.

$$P_{dc} = \frac{{V_{dd}}^2}{R_m} \tag{2.23}$$

Since the choke inductor can provide twice the voltage to the collector output, P_{out} can be calculated by

$$P_{out} = \frac{(V_{dd}/\sqrt{2})^2}{R_L} \tag{2.24}$$

By integrating the supply current in each transistor over half of the period, a π factor has been deducted from the P_{dc}:

$$P_{dc} = \frac{1}{\pi}\frac{{V_{dd}}^2}{R_L} \tag{2.25}$$

Lastly, the efficiency is

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi}{4} \approx 79\% \tag{2.26}$$

Figure 2.12 shows the voltage and current waveforms of a typical push-pull class B PA. Clearly, each transistor is on only half the period which could greatly increase the efficiency. However, with more components introduced, the network may suffer from more distortion and gain compression.

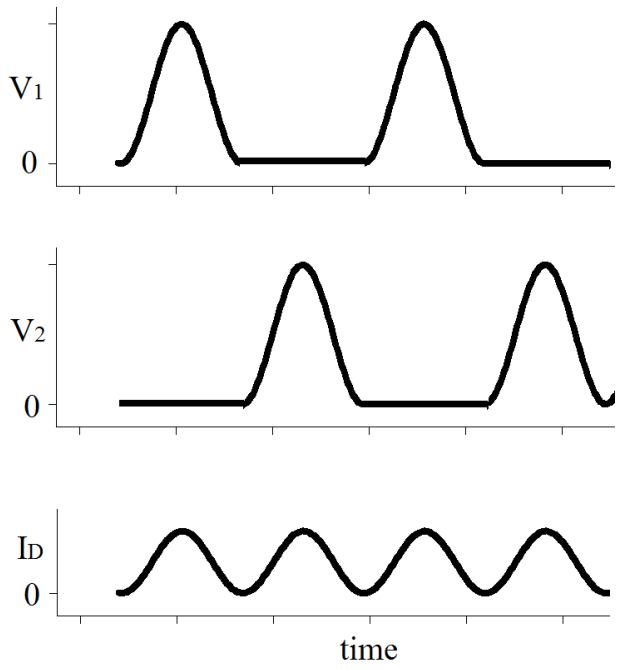


Figure 2.12: Voltage and Current Waveform for Class B PA

2.4.2 Class AB Amplifier

The class AB PA is a special combination of the aforementioned class A and class B with a conduction angle between 180° and 360°. In fact, a class A PA exhibits fewer non-linear effects, such as distortion and gain compression, but suffers greatly from its low efficiency. On the other hand, class B improves efficiency with a potential trade-off of nonlinearity. Thus, the class AB amplifier can serve as a middle solution to compromise the others' drawbacks.

2.4.3 Class C Amplifier

In class C stage, the conduction angle is further reduced. Although a seemingly high efficiency can be theoretically achieved, the transistor is turned off most of the time, which is hard for practical use. Many authors have derived the equation (2.27) for class C PA efficiency [17],[20].

$$\eta = \frac{1}{4}\frac{\theta - \sin\theta}{\sin(\frac{\theta}{2}) - (\frac{\theta}{2})\cos(\frac{\theta}{2})} \tag{2.27}$$

From this equation, class C PA efficiency can possibly reach 100% when θ, the conduction angle, drops to zero. However by L'Hopita's rule, when θ approaches to zero, efficiency also falls to 0, which makes power amplifier design pointless. Thus class C PA is rarely used in industry commercial products. Figure 2.13 shows the voltage and current waveforms of a class C PA.

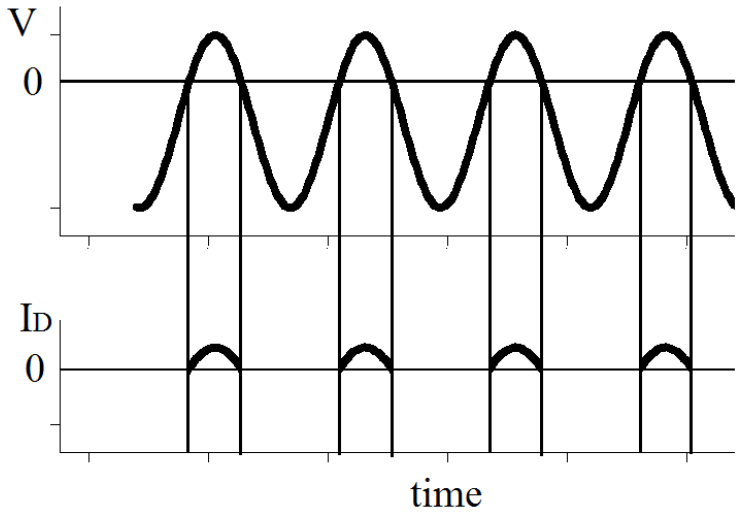


Figure 2.13: Voltage and Current Waveform for Class C PA

CHAPTER 3

SWITCHING MODE POWER AMPLIFIERS

Conventional class A, B and C PAs have long been recognized for their highly linearized operation, but low output efficiency. The reason behind this is that transistors in conventional PAs are operated as voltage-controlled current sources, which dissipate tremendous unwanted power and hurt efficiency when transistors are idle. To remedy this, researchers came up with an idea of using transistors as switches instead of current sources. Switching mode techniques have been widely used for many years in power electronics, and certainly offered great solutions for power savings. Examples of zero-voltage/zero-current switching (ZVZCS) DC-DC converters are introduced in [21],[22]. This ZVZCS technique was soon applied to RF designs and formed into the original shape of switching mode amplifiers. Undoubtedly, ZVZCS technique has markedly increased transistor efficiency in class D switching mode PAs. Furthermore, to increase the operating frequency to RF ranges (GHz) and keep this high efficiency, class E and class F switching mode PAs have been invented. Although they can provide high efficiency and greatly save battery life, all three switching mode PA prototypes face an unavoidable linearity issue since the voltage waveform is not continuous throughout a period. To remedy this potential hazard and achieve linear performance, specific technologies, such as inter-stage matching network and gain boosting stage, have been introduced in current PA designs.

3.1 Push-Pull Class D Amplifier

The class D power amplifier, one of the earliest power amplifiers to use the transistor as a switching device, was invented in 1959 [23]. It has a push-pull, two-switch topology with switches each operating for half a period alternatively [24]. Figure 3.1 shows a conventional class D PA design in which M_1

and M_2 are p-type and n-type MOSFETs, respectively. Assuming a 50%

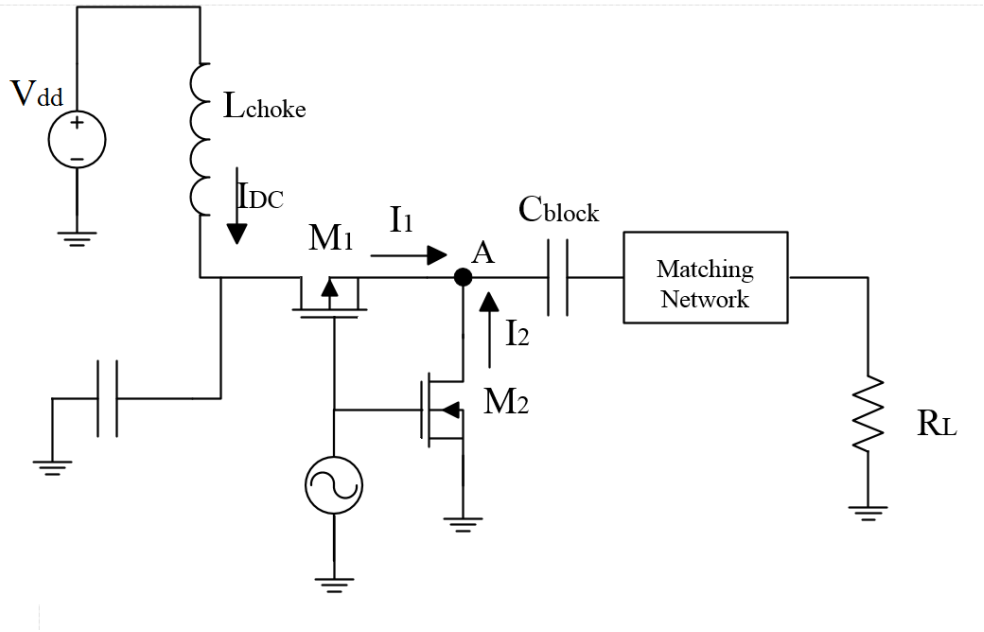


Figure 3.1: Push-Pull Class D Power Amplifier

duty cycle assigned to the AC source, during the first half period, M_1 turns on when I_{DC} flows through M_1 and biases point A with a voltage equal to V_{dd}. Next half period, M_1 turns off and M_2 turns on, which decreases the voltage at point A to zero. With M_1 and M_2 conducting alternately, a resulting full-wave current will flow through the load R_L. Figure 3.2 demonstrates the voltage and current waveform for a push-pull class D PA [19]. Obviously, since no loss occurred in the entire transition, the efficiency should have a value of 100% assuming all components are ideal.

$$\eta_{max} = \frac{P_L}{P_{dc}} = 100\% \tag{3.1}$$

However, in real life this is never the case. A typical value of class D PA efficiency falls between 70% and 75%.

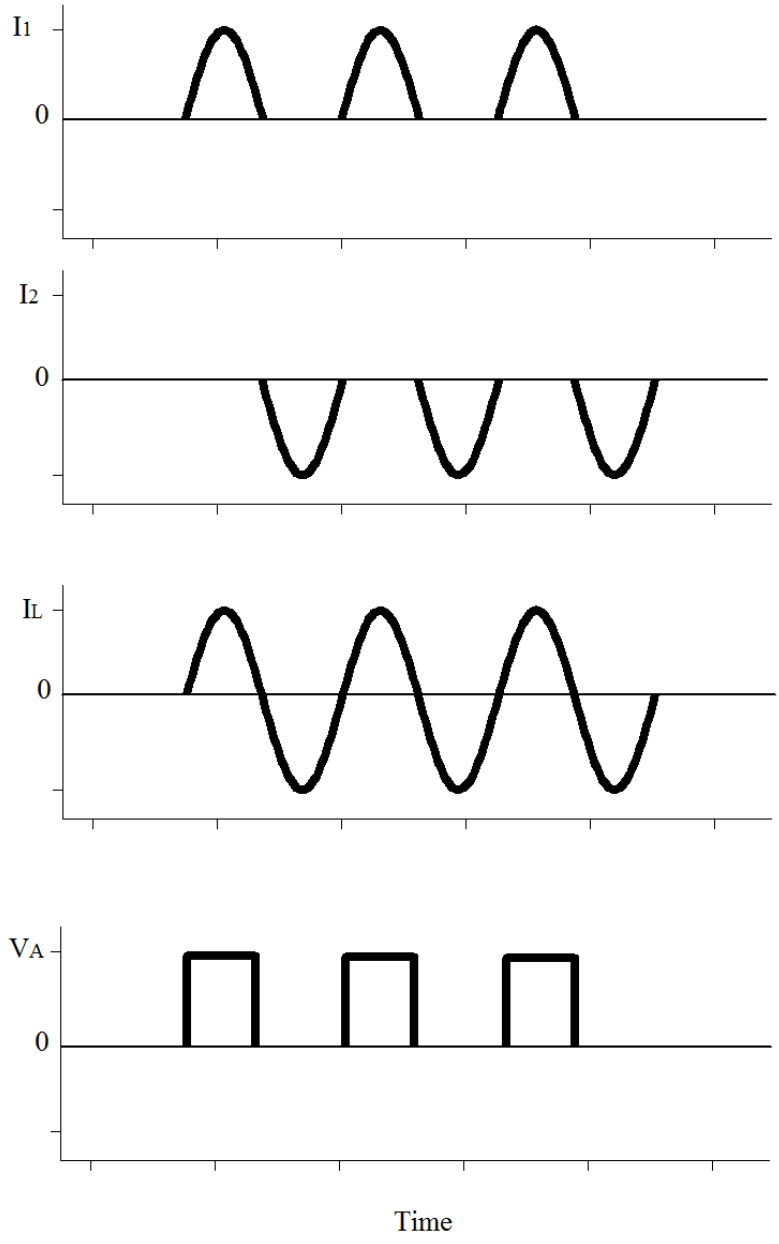


Figure 3.2: Voltage and Current Waveform for Class D PA

Class D PA is widely used in low-frequency audio amplification for producing hi-fi quality sounds. However, at high frequency, non-linear effects arise from the distortion caused by frequent switching. Thus, an amplifier with high efficiency, together with high-frequency operation, is crucial for mobile phones to work properly. This introduces the central focus of the thesis – the class E PA.

3.2 High-Efficiency Class E Amplifier

The class E power amplifier was first designed by Gerald Ewing, a PhD student at Oregon State University in 1965 [25]. At the time he introduced the circuit, he did not call it class E, but said that he designed a high-efficiency radio-frequency power amplifier. His PhD thesis [25] became the earliest source on class E PA. After Ewing, many researchers, such as the Sokal family, spent countless hours developing the amplifier.

Nathan Sokal mentioned in his paper [26] that there are three clear advantages of class E PA over all other previously introduced PAs. Firstly, he mentioned that class E PA has great efficiency enhancement compared to conventional class A, B and C PAs by reducing power loss by a factor of about 2.3 at the same output power and frequency. Secondly, he argued that class E PA can operate at a narrow bandwidth with high output power, whereas class A, B, C and D must operate at a bandwidth at least 1.8 times larger than class E. Lastly, with full confidence, he proved that all class E PAs are designable, which means the PA is built as designed and works as expected, without tweaking.

The Class E PA is used the most in current commercial products because of its high efficiency, and it is one of the few amplifiers being patented [U.S. 3,919,656, 1975] [19]. Three switching properties which can best characterize class E PA are [27]:

1. The transistor drives a minimum current when the voltage across it is at maximum, i.e. OFF state.

2. The transistor imposes a minimum voltage when the current is at its peak, i.e. ON state.

3. The transition time between ON and OFF state must be kept at a minimum.

Figures 3.3 and 3.4 show a simple class E PA and its waveform. To simplify, the three properties above can be expressed as

$$V_A|_{I>0} = 0 \tag{3.2}$$

$$I|_{V_A>0} = 0 \tag{3.3}$$

$$\frac{dV_A}{dt}|_{I=0^+} = 0 \tag{3.4}$$

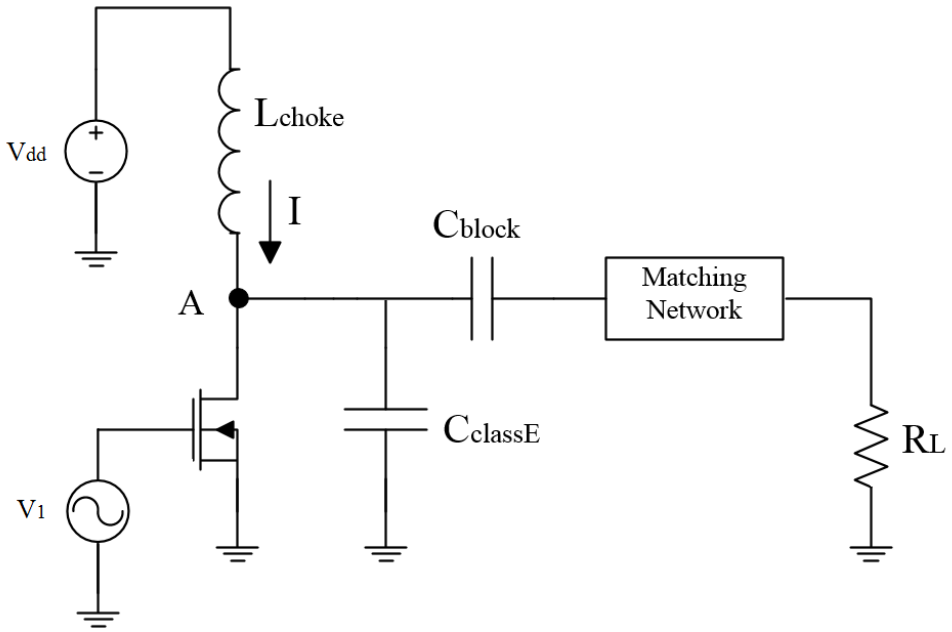


Figure 3.3: Single-Stage Class E Power Amplifier

From Figure 3.3, when the transistor is on, current I will flow through it with a zero voltage at point A. When the transistor is off, current I will flow through the class E capacitor and charge it to a maximum value around $3.56V_{dd}$ [17], causing of current to flow through the load as well. This vital capacitor, "class E cap," is the improvement from class D to class E such that no parasitic effect can arise since it is always discharged to ground. This also helps to improve the linearity issue in switching mode amplifiers. Also, since ZVZCS occurred in the entire transition, the efficiency for class E PA should have a value of 100% assuming all components are ideal.

$$\eta_{max} = \frac{P_L}{P_{dc}} = 100\% \tag{3.5}$$

However, in real life this is never the case. A typical value of class E PA efficiency falls in the range of 75-80%.

In most modern class E PAs, optimizing the "class E cap" is not enough to solve the linearity issues. A gain booster stage can be added in the network to further enhance the linearity performance. Note that the gain booster stage here is different than in analog IC design, which tries to significantly

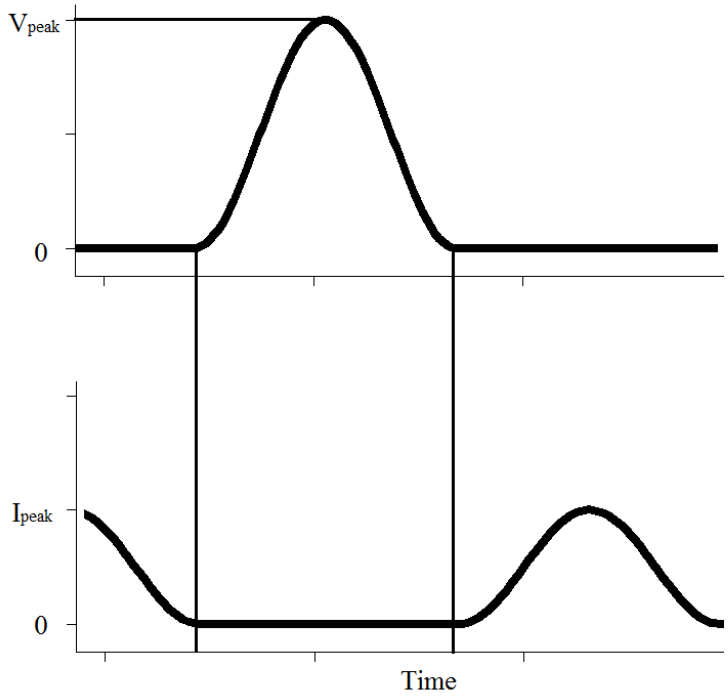


Figure 3.4: Voltage and Current Waveform for Class E PA

scale up the gain. However, it is a way to sharpen the gain shape at higher output power. When the gain is sharpened, linearity performance, such as ACPR and ACLR, can be improved greatly. Other techniques to improve the linearity include adding an inter-stage impedance matching network between driver and final stages to reduce the mismatches, and adding feed-forward circuits where linearity suffers the most.

Harmonic degeneration is another potential risk in class E PA design. Harmonics are integer multiples of fundamental frequencies and often can do harm to amplifier designs. To remedy this, a filtered-type output impedance matching network is indispensable for rejecting the unwanted frequencies of signals. Impedance matching will be discussed in detail in the next chapter.

Lastly, a knee voltage exists in the class E PA voltage waveform when the transistor is in its ON state. In other words, voltage can never shut off entirely when current is flowing through the transistor. Usually this knee voltage is around 0.3 V and it is crucial in calculating the efficiencies.

3.3 Harmonically Tuned Class F/ F^{-1} Amplifier

The class F is widely considered as a harmonically tuned or harmonically terminated amplifier. It has the same features as the class E amplifier, i.e. high efficiency, high power, high frequency operation and bad linearity. The only two differences are the topology and the output voltage waveform. The class F PA (Figure 3.5) is based on the class A configuration with a more complicated output matching network (3.6).

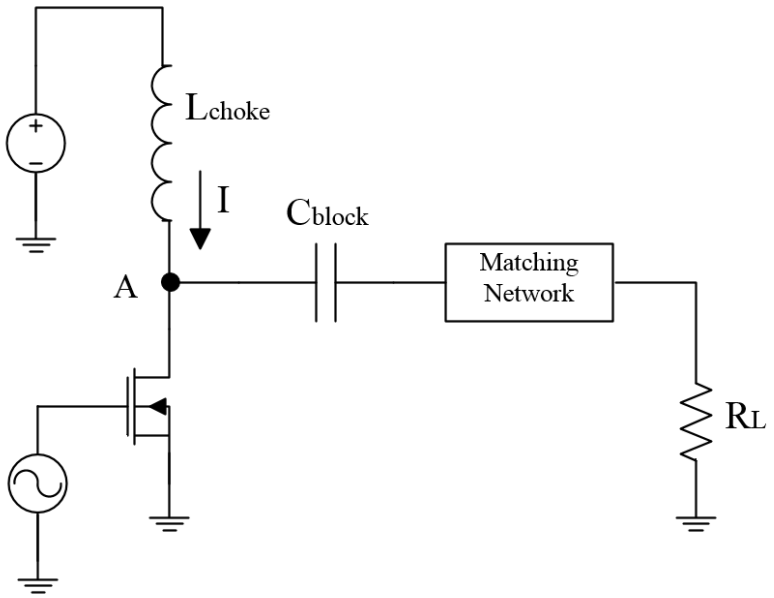


Figure 3.5: Single-Stage Class F Power Amplifier

The inductor and capacitor pairs in Figure 3.6 are called resonance pairs. The value of each resonant frequency of nth pairs is the $(2n+1)$th harmonic frequency of the class F PA. For example, for a class F PA designed at a center frequency of 2 GHz, the resonant frequency for the pair L_1 and C_1 is 5 GHz (third harmonic), and the resonant frequency for the pair L_2 and C_2 is 10 GHz (fifth harmonic). As a matter of fact, a parallel LC pair behaves as an open circuit when operating at its resonant frequency. With this harmonic termination, the voltage across the transistor exhibits a sharpened waveform at the edges, and therefore power loss is reduced at zero voltage transition (Figure 3.7) [17].

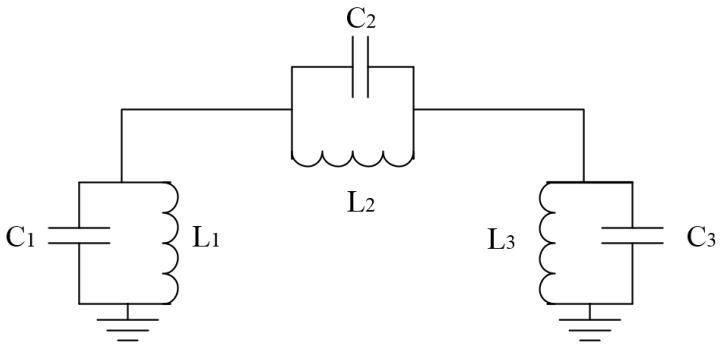


Figure 3.6: Third-Order Class F Output Matching Network

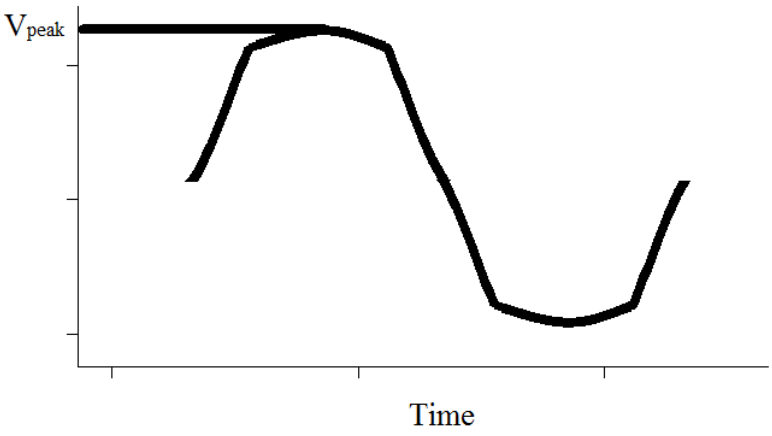


Figure 3.7: Voltage Waveform for Class E PA

Figure 3.7 shows a third-order harmonic termination class F PA voltage waveform. In order to obtain a flat-band waveform, more resonant pairs need to be introduced. (This phenomenon resembles the Butter-worth bandpass filter designs [28]). Since class F PA is also defined as a switching mode amplifier, it can theoretically achieve 100% collector efficiency with infinite number of resonant pairs, made from ideal components, presented in the output matching network.

Inverse class F PA has the exact same amplifier configuration as class F, but a slightly different harmonic termination technology. Instead of being resonant at $(2n+1)$th for the nth pair, it is operated at $(2n)$th harmonic

frequency. Table 3.1 shows the termination comparison between class F and inverse class F PA.

Table 3.1: Class F and Inverse Class F Harmonic Termination Comparison

Harmonics	$2f_0$	$3f_0$	$4f_0$	$5f_0$	$6f_0$	$7f_0$
Class F	short	open	short	open	short	open
Class F^{-1}	open	short	open	short	open	short

So far, eight major classes of power amplifier have been introduced in chapters 2 and 3. Efficiency and linearity comparisons among all classes are summarized in Table 3.2 [29].

Table 3.2: Efficiency (η) and Linearity Comparisons Among All Major Classes of Power Amplifier

Class	A	B	AB	C	D	E	F	F^{-1}
Typical η	35%	60%	35-59%	70%	75%	80%	80%	80%
Max η	50%	79%	50-78%	100%	100%	100%	100%	100%
Linearity	Good	Good	Good	Bad	Bad	Bad	Bad	Bad

CHAPTER 4

IMPEDANCE MATCHING NETWORK – A DESIGN PERSPECTIVE

The impedance matching network is commonly considered as a part of the main design process for an RF microwave component and system [30], in our case RF power amplifier design. Like DC-DC converters, impedance matching networks can help engineers to transform load impedance to a larger or smaller value, depending on the requirement. Figure 4.1 shows a simple impedance matching network connected between source and load impedances. The basic idea of this transformation is to deliver maximum real power to a complex load Z_L; the source impedance Z_S should possess a value equal to the complex conjugate of the load impedance Z_L [31]. This chapter introduces basic impedance matching techniques, such as topologies, complexity, bandwidth etc., and implements a complex class E PA output matching network using Advanced Design System (ADS) computer software.

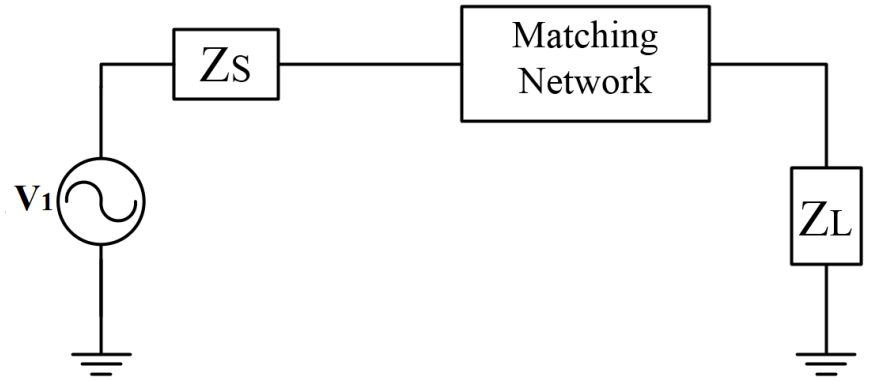


Figure 4.1: Impedance Matching Network

4.1 Simple Lossless L-Network

An L-network serves as the simplest solution for narrow-band impedance matching. Other techniques include Π-network, T-network and transmission lines stub matching networks. However, due to the limited space on a power amplifier module, L-network is most widely used in transforming a low collector impedance to a 50 Ω antenna within the power amplifier. To fully understand impedance matching concepts, a brief introduction to the maximum power transfer theorem is necessary.

4.1.1 Maximum Power Transfer Theorem

Most electrical engineering undergraduate students should learn this concept in their coursework, and this theorem has been introduced by many authors [18],[30],[32]. The theorem states that the maximum power that can be delivered to the load impedance occurs when source and load impedance possess a complex conjugate match of each other [33]. From Figure 4.1, source and load impedance can be written as

$$Z_S = R_S + jX_S \tag{4.1}$$

$$Z_L = R_L + jX_L \tag{4.2}$$

Then the real power delivered to the load can be expressed as

$$P_L = \frac{1}{2} Re\{V_L I_L^*\} \tag{4.3}$$

$$P_L = \frac{1}{2}|V_L|^2 \frac{R_L}{|Z_L|^2} \tag{4.4}$$

Assuming a lossless matching network, current stays the same:

$$P_L = \frac{1}{2}|V_1|^2 \frac{R_L}{(R_L + R_S)^2 + (X_L + X_S)^2} \tag{4.5}$$

From equation (4.5), the maximum real power delivered to the load occurs when

$$R_S = R_L \tag{4.6}$$

$$X_S = -X_L \tag{4.7}$$

The resulting P_{Lmax} is

$$P_L = \frac{|V_{1,rms}|^2}{4R_S} \tag{4.8}$$

Hence, the maximum power transfer is obtained by nulling the reactances while transforming the existing resistances until source and load match (assuming lossless components) [32]. A typical design process using an L-network will be discussed in the following sections.

4.1.2 Double-Stage L-Network Using the Network "Q"

A basic single-stage L-network, which has been mentioned by various authors [16],[18],[30],[32], can be designed using both equations and a Smith chart. A more complicated, but realistic, double-stage L-network will be discussed in this section.

Figure 4.2 shows two impedances (Z_L, Z_S) to be matched using a double-stage L-network. Surely, there are mainly two approaches to calculate the values for each matching component (L_1, C_1, L_2, C_2), namely equations and a Smith chart.

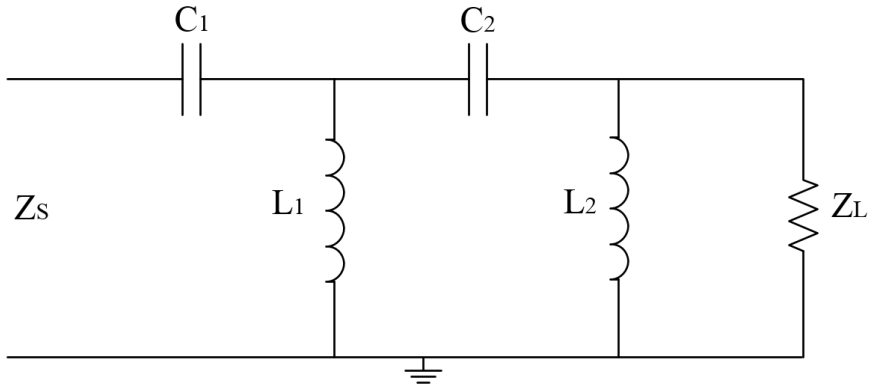


Figure 4.2: Double-Stage L-Network which Transforms Z_L to Z_S

Using Equations

To apply the equations to calculate the values for the matching components, it is important to know the required quality factor for the network (network "Q") and the intermediate impedance between the two stages. For example, to transform 50 Ω load to 5 Ω source with two stages, an intermediate

impedance of around 15.8 Ω can be calculated by equation (4.10) between two stages. In other words, 50 Ω load can be first transformed to a 15.8 Ω load, then transformed to the 5 Ω source. Again, equations for single-stage L-network transformation have been introduced by many aforementioned authors [16],[18],[30],[32]. The equations are:

$$R_{inter} = \sqrt{R_S R_L} \tag{4.9}$$

$$Q = \sqrt{\frac{R_L}{R_{inter}} - 1} \tag{4.10}$$

$$X_P = \pm\frac{R_L}{Q} \tag{4.11}$$

$$X_S = \mp R_{inter} Q \tag{4.12}$$

in which X_P and X_S stand for the parallel and series matching components in the L-network. Calculations are omitted in this part of the thesis. A thorough and complete impedance matching network design will be introduced later.

Using the Smith Chart

The Smith chart, invented by Phillip Smith in 1939 [34],[35], is one of the key design tools in RF microwave engineering. At first, it was introduced to provide convenient solutions for transmission line calculations that were done by conventional equations. Later, use of the Smith chart extended to other RF network designs, such as matching networks. Figure 4.3 shows how to design a double-stage L-network using the Smith chart. In the figure, the network Q circle is defined as the elliptical shape crossing both ends of the Smith chart, i.e. constant Q circle. Matching components L_1, C_1, L_2, C_2 follow the schematic in Figure 4.2. The "M" shape defines a high-pass high-pass (HPHP) configuration in the impedance matching network design and often introduces least loss at the high end of the desired frequency range compared to all other configurations.

4.2 Class E PA Output Matching Network Design

So far, eight major classes of power amplifiers have been introduced, each with its unique advantages and disadvantages (Table 3.2). The class E PA,

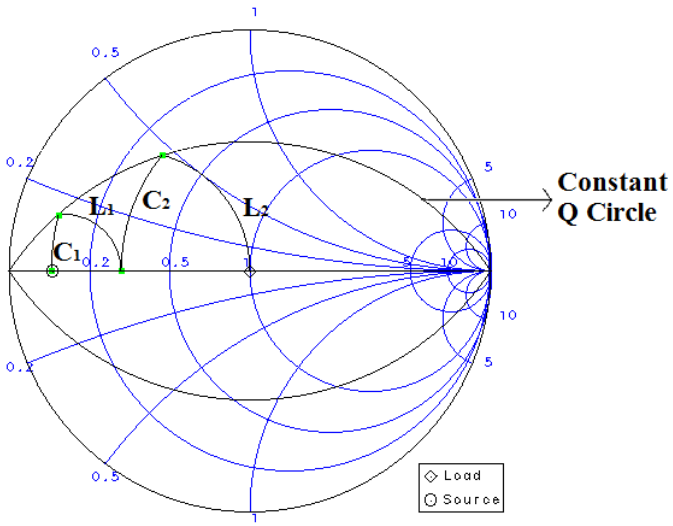


Figure 4.3: Double-Stage L-Network Design Using Smith Chart

considered the first switching mode power amplifier that operates at high frequency, has a figure of merit on its high efficiency. However, without a proper output matching network, everything that happened in class E would have been impossible. This section will build a full conventional double-stage L-network output matching for class E PA. Table 4.1 shows the design goal for the impedance matching network.

Table 4.1: Requirements for Class E PA Output Matching Network

Specification	Abbreviation	Values	Units
Load Resistance	R_L	50	Ω
Source Resistance	R_S	5	Ω
Center Frequency	f_c	1	GHz
Bandwidth	f_ω	400	MHz
Network Q	Q_N	1.5	-
Insertion Loss	S_{21}	-2	dB
Second Harmonic Rejection	$2f_0$	-40	dB
Third Harmonic Rejection	$3f_0$	-60	dB

4.2.1 Smith Chart Tool

Due to the high requirements for second and third harmonic rejection, a low-pass low-pass (LPLP) topology has been chosen to design the network. A low-pass impedance matching network is similar to a low-pass filter [36], which can reject higher frequency signals efficiently. Figure 4.4 shows the typical LPLP topology with inductor as the series passing component and capacitor as the shunt blocking component.

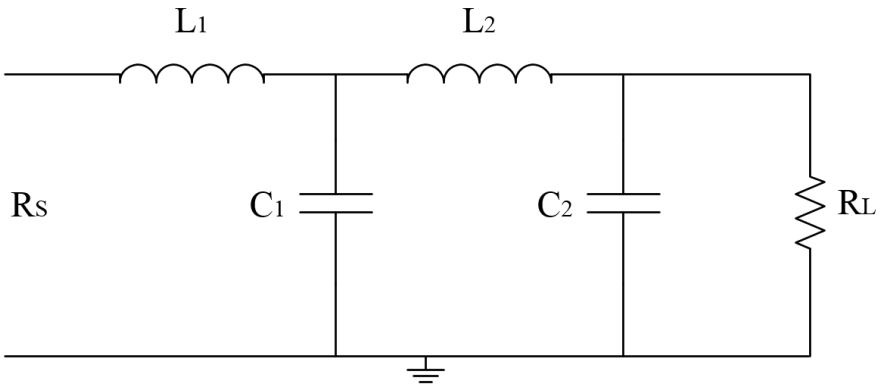


Figure 4.4: Double-Stage L-Network Design Using LPLP Topology

Figure 4.5 presents a LPLP matching network design procedure done by the Advanced Design System (ADS) computer software. This Smith chart tool is highly recommended for RF design beginners, and saves the tremendous time spent manually drawing on the Smith chart. As specified in the design requirements (Table 4.1), a 1.5 network Q circle has been selected on the Smith chart. Initial component values are summarized in Table 4.2.

Table 4.2: Matching Component Values from Smith Chart Tool

Components	Values	Units	Quality Factor (Q)
L_1	1.14379	nH	50
C_1	15.10666	pF	40
L_2	3.67509	nH	50
C_2	4.76098	pF	40

The reason for choosing network Q = 1.5, besides specification, lies in the relationship between network Q and bandwidth (equation (4.13)). As proved in Li [28], in order to achieve functionality, fractional bandwidth (0.2) must

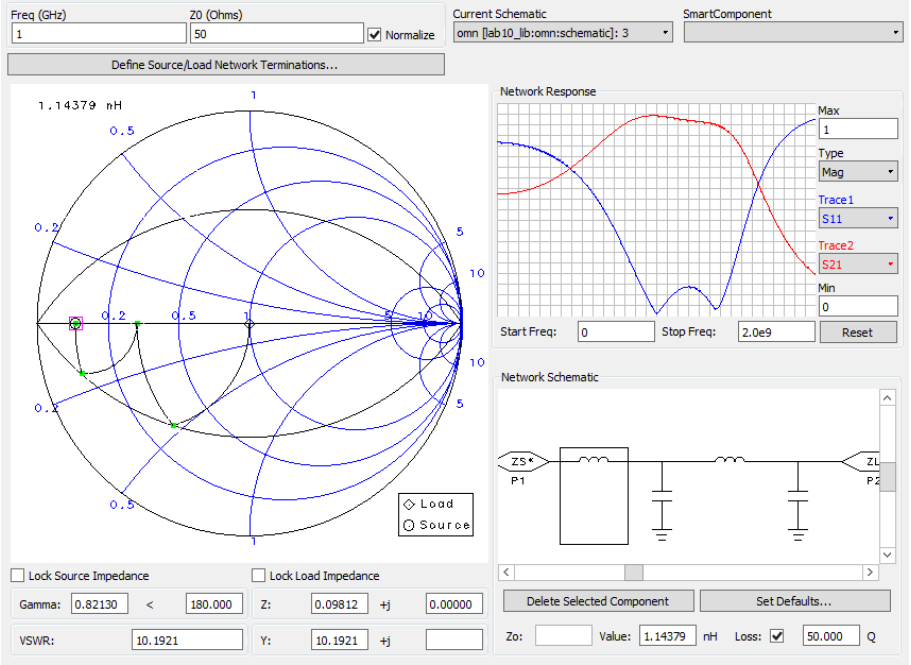


Figure 4.5: LPLP Matching Network Designed by Smith Chart

be smaller than the reciprocal of network Q (0.633). This property ensures the design is achievable.

$$\%BW < \frac{1}{Q} \tag{4.13}$$

4.2.2 Harmonic Traps

A conventional RF power amplifier usually has a harmonic-suppression filter at its output stage in order to reject unwanted signal degenerated from the harmonic frequencies [37]. Usually there is a requirement that the amplitude for the nth harmonic frequency component has to be smaller than a fundamental frequency component by a certain amount, expressed in dB units [37],[38]. In modern PA design, instead of using filters, harmonic traps are more often used to attenuate harmonic frequency components. A harmonic trap is a series LC network which replaces the single component in the shunt arm of the matching network, i.e. C_1 and C_2. Obviously, to reject well, the resonant frequency of each harmonic trap should equal to the harmonic frequency with the greatest amplitude. In most cases, the second and third harmonics have the greatest amplitude and need to be rejected sufficiently in order for the amplifier to work.

In this LPLP output matching network design, a series inductor can be added between the shunt arm capacitor and ground. To reduce the complexity, second-order harmonic rejection is added to the first shunt arm and a third-order to the second shunt arm as shown in Figure 4.6. The values for L_3 and L_4 are calculated by equation (4.14) and summarized in Table 4.3.

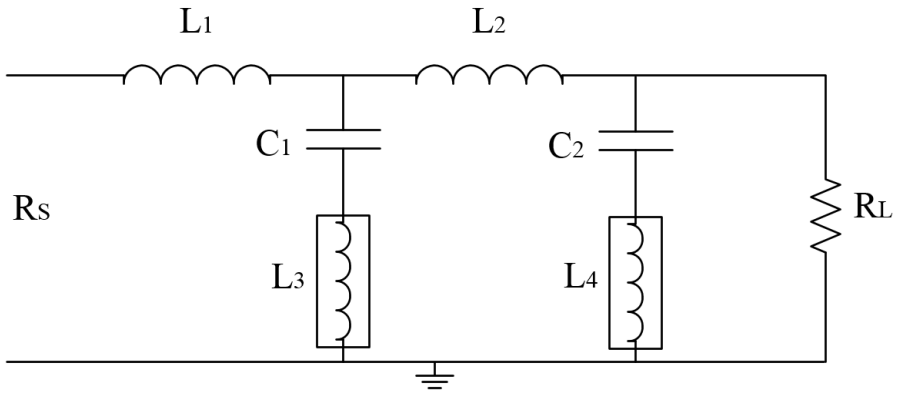


Figure 4.6: LPLP Matching Network with Harmonic Traps

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.14}$$

Table 4.3: Component Values for Harmonic Traps

Components	Values	Units	Quality Factor (Q)	Resonance Frequency
L_3	0.419	nH	50	2GHz
L_4	0.5988	nH	50	3GHz

The inductances of harmonic traps are generally smaller than the inductances of matching components. Thus, in real life fabrication, most engineers take advantage of the ground inductances generated from packing vias to design the harmonic traps. For this purpose, both the area and cost of adding additional inductors can be saved.

4.2.3 Design Implementation

By now, all the major components have been discussed. However, for the amplifier to work properly, additional components, such as choke, blocking caps and the "magical" class E cap are needed. Figure 4.7 displays the entire

design of the proposed LPLP output matching network with the component values summarized in Table 4.2, 4.3 and 4.4.

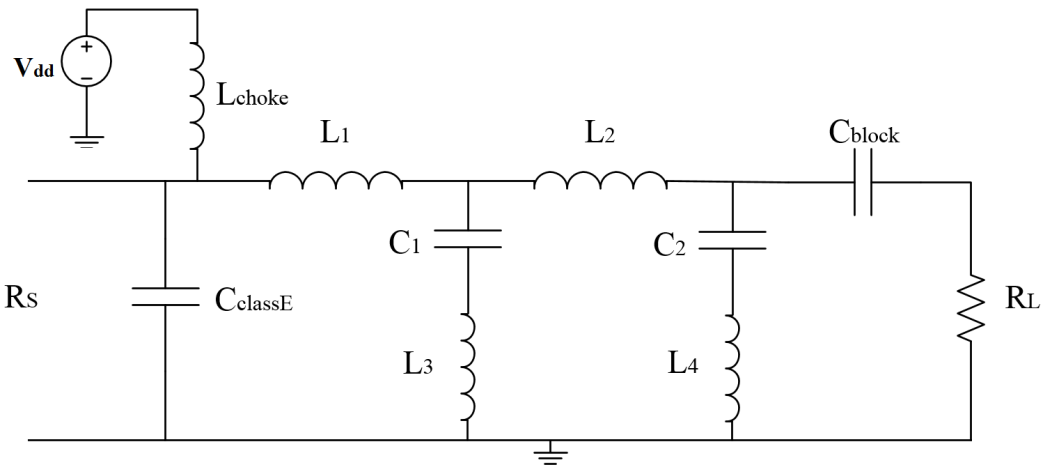


Figure 4.7: Entire Output Matching Network Design

Table 4.4: Additional Components values

Components	Values	Units	Quality Factor (Q)
L_{choke}	5	nH	50
C_{classE}	10	pF	20
C_{block}	1000	pF	∞

4.3 Simulation and Discussion

This section provides simulation results of the aforementioned output matching network using software ADS.

4.3.1 Circuit Schematic in ADS

4.3.2 Return Loss Simulation

Figure 4.9 shows the return loss of the entire network (as depicted in Figure 4.8). Clearly, in the operating bandwidth 800 MHz to 1.2 GHz, all frequency signals have return loss lower than -10 dB. This is a sign of good impedance transformation from load ($R_L = 50\Omega$) to source $R_S = 5\Omega$ impedance.

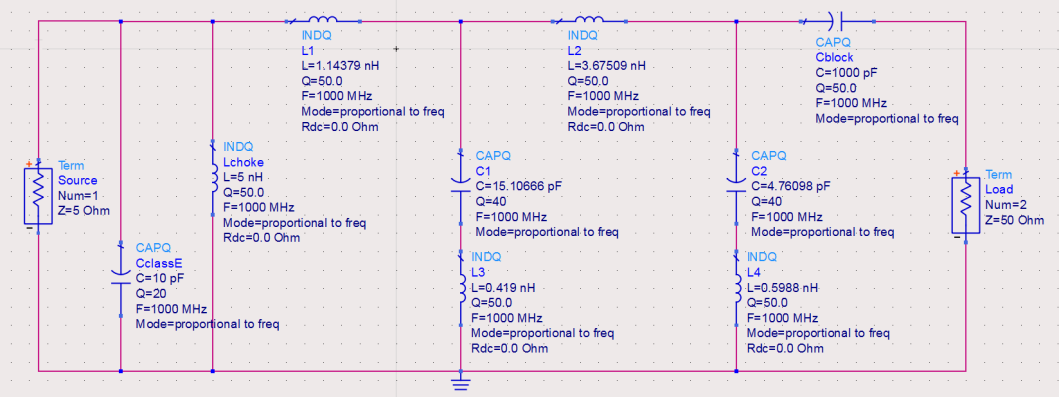


Figure 4.8: LPLP Output Matching Network Circuit Schematic in ADS

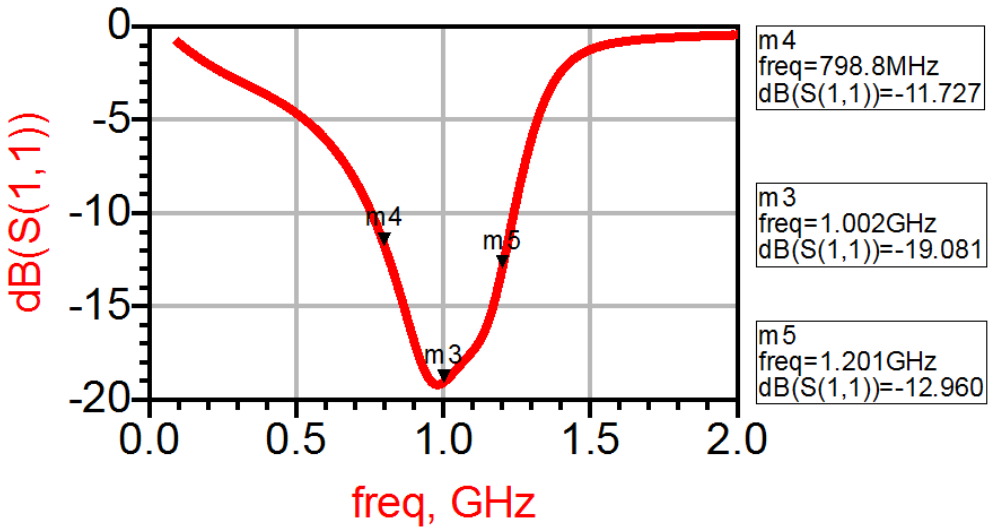


Figure 4.9: Return Loss Simulation Result

4.3.3 Insertion Loss Simulation

Figure 4.10 indicates the insertion loss of the network. In the frequency of operation 800 MHz to 1.2 GHz, all signals have insertion loss lower than the requirement (-2 dB).

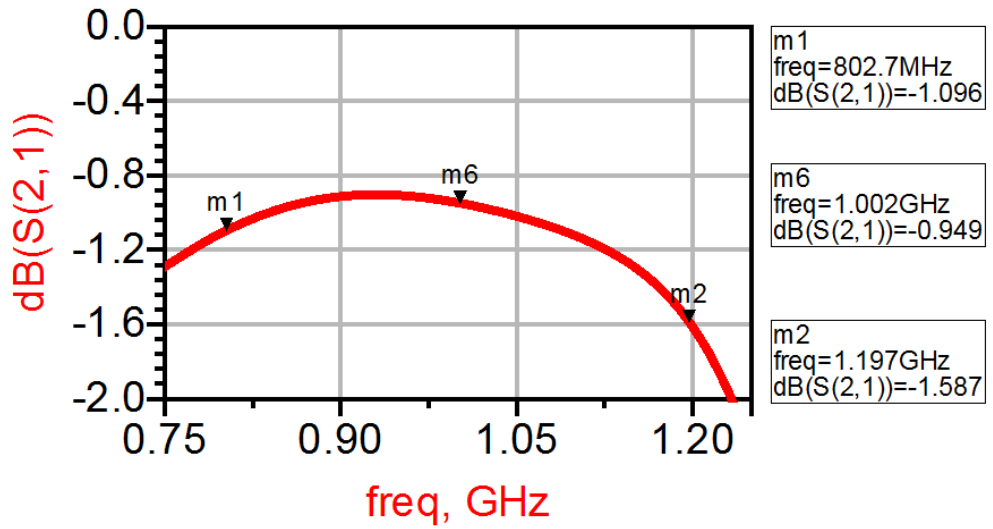


Figure 4.10: Insertion Loss Simulation Result

4.3.4 Harmonic Rejection Simulation

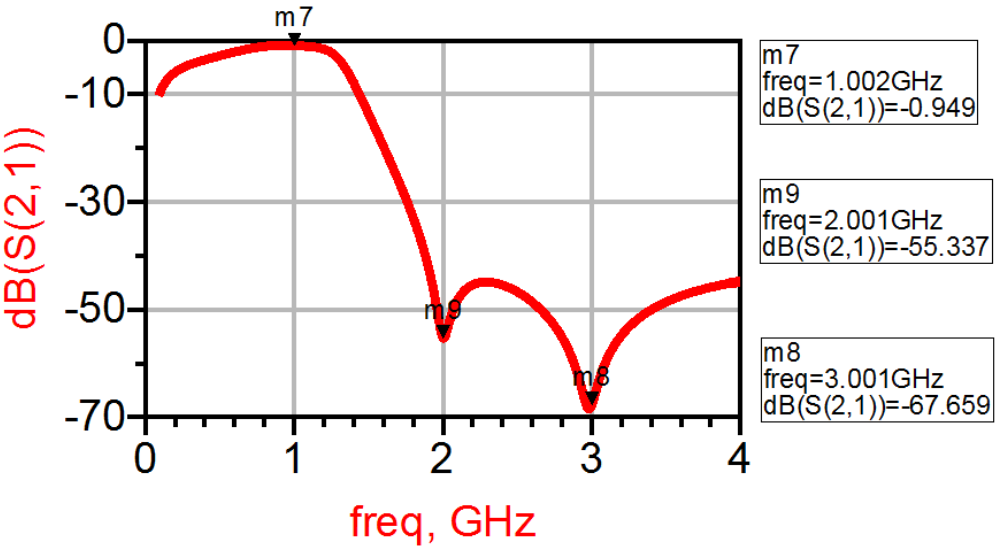


Figure 4.11: Broadband S_{21} Simulation to Analyze Harmonic Rejections

Figure 4.11 displays the broadband S_{21} simulation results. In the second (2 GHz) and third (3 GHz) harmonics of the fundamental frequency (1 GHz), rejections are both below the requirements (-40 dB, -60 dB). Sudden drops (notches) at the second and third harmonic frequencies are results of adding

the harmonic traps under shunt arms.

In conclusion, by analyzing the above simulation results, it is safe to say that all design requirements are met in this class E LPLP output matching network, though there are still many improvements that can be made, such as improving S_{21} further and using areal capacitor/inductor model. In future studies, graduate students should reproduce this impedance matching network with improvements in loss, operating frequency and component models.

CHAPTER 5

MEASUREMENT THEORY AND IMPLEMENTATION

Modern wireless communication system design focuses on high performance, while preferring low-cost active RF components in order to meet the demands for higher data rate and longer battery life. The power amplifier, the key building block in all RF transceivers, is known for its highly non-linear and power hungry nature. There is a trade-off between efficiency and linearity for all microwave amplifier designs; therefore, engineers are working hard to increase performance while maintaining the balance. This chapter provides theories for various power amplifier measurements and simulations. Both single-tone and two-tone input signals will be provided to the power amplifier to measure its efficiency and nonlinearity. Further analysis includes measuring adjacent channel power ratio (ACPR) with code division multiple access (CDMA) modulated input signals. In the end, the entire measuring environment will be discussed.

5.1 Single-Tone Input System

5.1.1 Measurement Theory

The single-tone input measurements mainly include power added efficiency (PAE), power gain, 1 dB gain compression and power versus time if modulated signals were provided. Single-tone means there exists only one frequency in the input signal. Due to nonlinearity, output signals should consist of multiple frequencies, but all fall within the harmonics of the fundamental input signal. In chapter 2, detailed explanations of PAE and 1 dB compression gain have already been introduced. Equation (5.1) shows the important relationship between the RF power and DC power. Figure 5.1 presents the 1 dB gain compression point on a P_{in} to P_{out} plot. Equations for calculating

1 dB compression gain were provided in chapter 2.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{5.1}$$

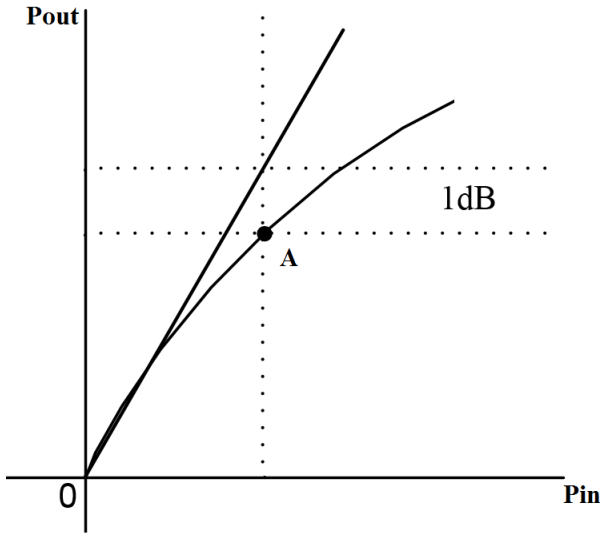


Figure 5.1: 1 dB Compression Point of a Non-Linear Network

Power gain is defined as the power ratio between output and input powers. There are mainly three types of power gain – operating power gain G_{op}, transducer power gain G_{tu}, and available power gain G_{av} [30]. Equations (5.2), (5.3) and (5.4) summarize the behavior of each power gain. P_{out}, P_{in} are output and input transmitted powers, and P_{avo},P_{avs} are output and input available powers. Of these three power gain definitions, transducer power gain is the most widely used to characterize the gain of a power amplifier, since it depends on both the input and the output impedances. Detailed S-parameters expressions for the three power gains can be found in Franke's note [18].

$$G_{op} = \frac{P_{out}}{P_{in}} \tag{5.2}$$

$$G_{tu} = \frac{P_{out}}{P_{avs}} \tag{5.3}$$

$$G_{av} = \frac{P_{avo}}{P_{avs}} \tag{5.4}$$

5.1.2 Simulation Method

The harmonic balance (HB) method is usually used in ADS to simulate single-tone input systems. Harmonic balance captures magnitude and phase of nonlinear circuits harmonics, frequency dependence and mismatch effect by calculating the steady-state response of differential equations [39]. As discussed in 1 dB gain compression calculation, a nonlinear circuit will generate harmonic terms of fundamental input frequency at its output. Effectively, output signals can be balanced with various sinusoids to satisfy Kirchhoff's law [40]. This balanced behavior is called harmonic balance, which is widely used in all power amplifier nonlinearity large-signal measurements. In addition to single-tone input systems, HB can also be applied to multiple input frequencies. This is another advantage of HB simulation since it includes harmonics and inter-modulation frequencies. Figure 5.2 shows the ADS symbol for single-tone harmonic balance simulation.

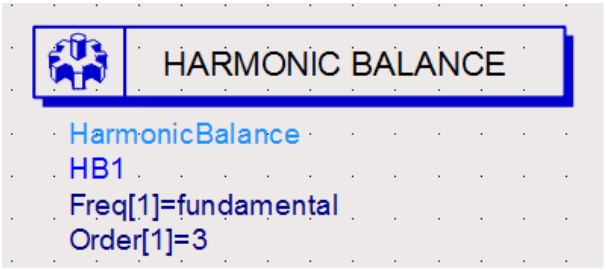


Figure 5.2: ADS Symbol for Single-Tone Harmonic Balance Simulation

5.2 Two-Tone Input System

5.2.1 Measurement Theory

Typical two-tone input measurements include two-tone third-order intermodulation distortion, interception point (IIP3), dynamic amplitude to amplitude (AM-AM) and amplitude to phase (AM-PM).

When two signals with closely spaced frequencies, f_1 and f_2, are the inputs for a nonlinear system (i.e. power amplifier), then the output contains intermodulation product terms as depicted in Figure 5.3. Among all frequencies listed on the output signal spectrum, two of the boxed ones are the biggest

concerns since they cannot be filtered out easily such that they are located too close to the fundamental tones [41]. This phenomenon is called the two-tone third-order inter-modulation distortion and is explained mathematically in the equations below [18].

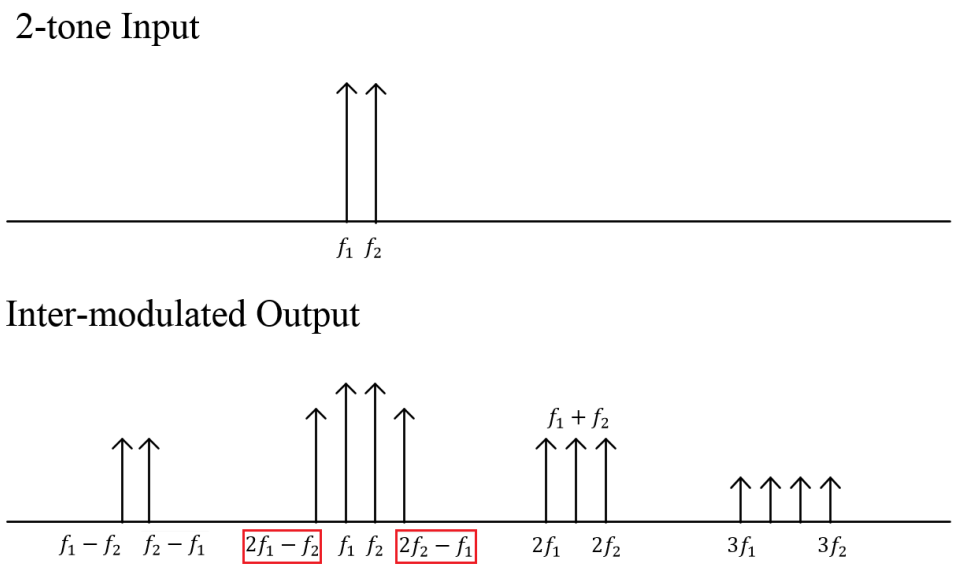


Figure 5.3: First-, Second-, and Third-Order Output Signal Spectrum (bottom) Generated from Two-Tone Input Signal (top)

Consider a nonlinear system with an input signal of $V_{in}(t) = a_1 \cos \omega_1 t + a_2 \cos \omega_2 t$ with three nonlinear power series terms of $P = k_1 V_{in} + k_2 {V_{in}}^2 + k_3 {V_{in}}^3$. The output signal can be expressed as

$$\begin{aligned} V_{out}(t) =& k_1[a_1 \cos \omega_1 t + a_2 \cos \omega_2 t] \\ &+ k_2[a_1 \cos \omega_1 t + a_2 \cos \omega_2 t]^2 \\ &+ k_3[a_1 \cos \omega_1 t + a_2 \cos \omega_2 t]^3 \end{aligned} \tag{5.5}$$

Using trig identities, the two boxed third order output signals can be written as

$$\begin{aligned} V_{out}(t)_{3rd\ order} =& \frac{3}{4} a_2 {a_1}^2 (\cos(2\omega_1 - \omega_2))t \\ &+ \frac{3}{4} a_1 {a_2}^2 (\cos(2\omega_2 - \omega_1))t \end{aligned} \tag{5.6}$$

and the fundamental frequency components are:

$$V_{out}(t)_{1st\ order} = k_1[a_1 \cos \omega_1 t + a_2 \cos \omega_2 t] \tag{5.7}$$

Two-tone third-order inter-modulation distortion is a risk for the system, since the two inter-modulated frequencies are spaced closely to the fundamental tones; especially their amplitudes are not negligible. To quantitatively analyze this behavior, many authors [41],[42],[43],[44] introduced the inter-modulation distortion (IMD) test to find the interception point (Figure 5.4 [18]). In the plot, IIP3 stands for the input third-order interception point and OIP3 stands for the output third-order interception point. In real world design, this point can help engineers to find the relative nonlinearity of a power amplifier system.

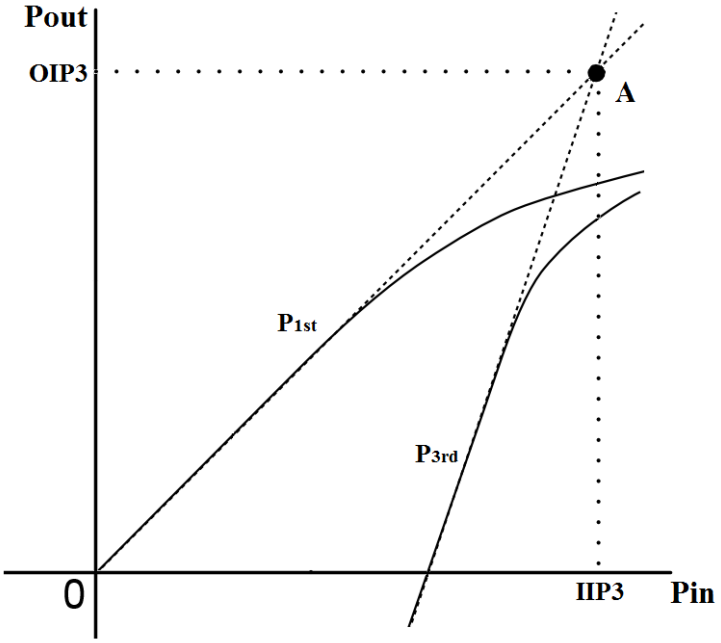


Figure 5.4: Inter-Modulation Distortion Interception Point Demonstration

Dynamic AM-AM and AM-PM behaviors exist in the transformation of the input amplitude variation into variations of the output amplitude and phase, respectively [45]. In other words, these behaviors indicate the amount of unwanted amplitude/phase variations caused by input amplitude variation. Figure 5.5 displays a AM-AM/AM-PM comparison between linear and nonlinear systems. Clearly, a linear system has no amplitude and phase variations across the output power range, whereas a nonlinear system exhibits variations.

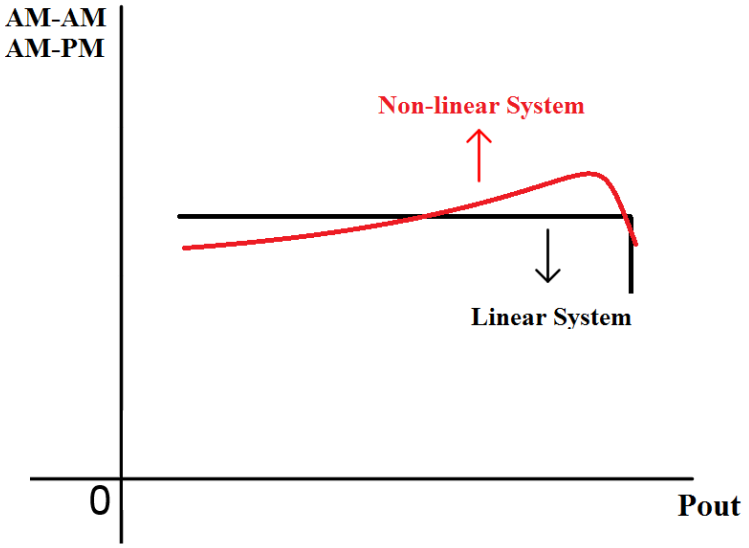


Figure 5.5: AM-AM and AM-PM Comparison Between Linear and Non-Linear System

5.2.2 Simulation Method

For a two-tone input system, obviously, HB simulation is still applicable and used widely in simulating inter-modulation distortions. On top of the HB simulation, circuit envelope (CE) is a more accurate simulation method since it focuses on narrow bandwidth. There are many applications associated with CE. Among them are adjacent channel power ratio, error vector magnitude, PAE, power vs. time etc. [46]. In practice, HB is widely used for simulating steady-state RF signals, whereas Envelop is often related to non-steady-state RF simulations. Figure 5.6 shows the ADS symbol for CE simulation.

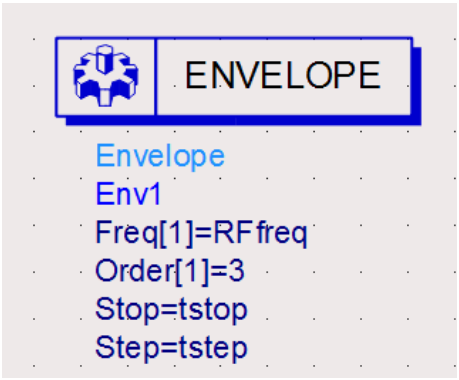


Figure 5.6: ADS Symbol for Envelope Simulation

5.3 Adjacent Channel Power Ratio

The adjacent channel power ratio (ACPR), also called adjacent channel leakage ratio (ACLR), is a measure of distortion power leaking into the left/right adjacent channels in relation to the carrier power in the reference channel [47]. In wireless communication, ACPR is an increasingly imperative linearity measurement which requires much time and highly specialized equipment. Thus, in early days, two-tone third-order inter-modulation distortion (IMD) test served as the main engine of linearity measurements. Nowadays, with the introduce of sophisticated measurement equipment, ACPR test is performed on a power spectrum analyzer with the device under test (DUT) connected to a digitally modulated input signal, i.e. CDMA, NADC. It characterizes the likelihood of a given system that may cause interference with the neighboring channels [48]. Comparison results on IMD and ACPR tests will be shown in later chapters.

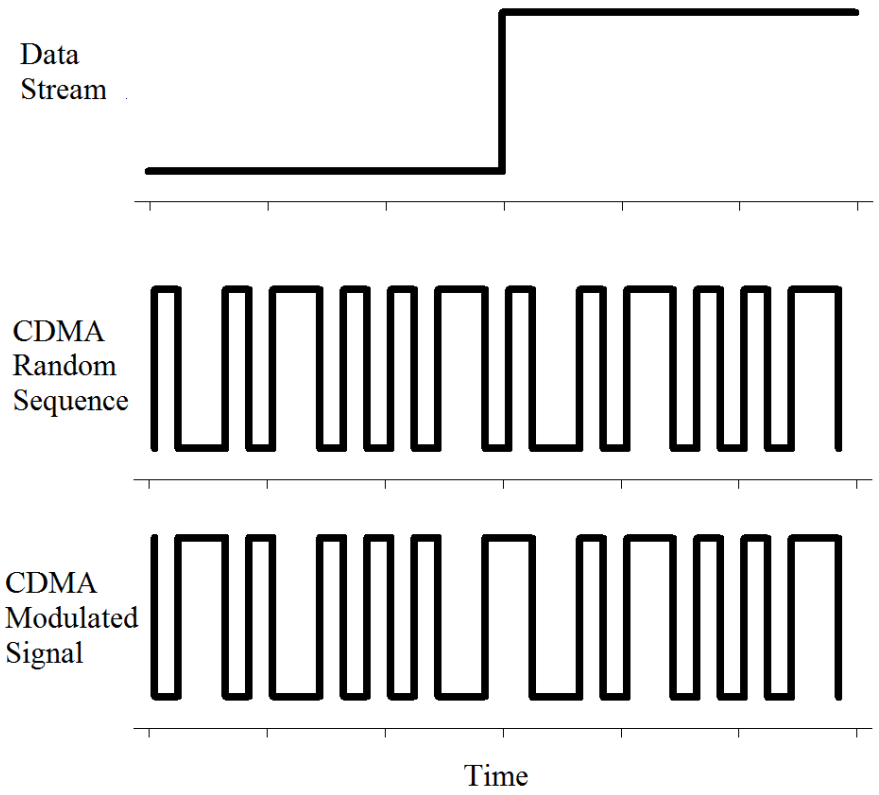


Figure 5.7: CDMA Modulation

Code division multiple access (CDMA) was first introduced under the IS95

standard, which later evolved into the worldwide 3G communication system. It is an access method which allows multiple information to be sent simultaneously using single channel carrier [49]. To be specific, it is operated by multiplying the conventional data stream with a pseudo-random chip sequence to provide fast data rate transformation (Figure 5.7). This behavioral is called digital modulation which spreads the original form into a larger bandwidth data stream. Other digital modulations include QPSK, OFDM, and TDD etc. [19].

A comparison between unmodulated and CDMA digitally modulated signals is shown in Figure 5.8. The reason for the square-wave like shape is that the CDMA modulated signal has a number of signals transmitted in one period. As a matter of fact, square wave can be generated using an infinite number of the same amplitude, but different frequencies of sinusoidal waves. Thus, this square-like shape best illustrates that CDMA modulated signals can transfer data with a higher rate than unmodulated ones.

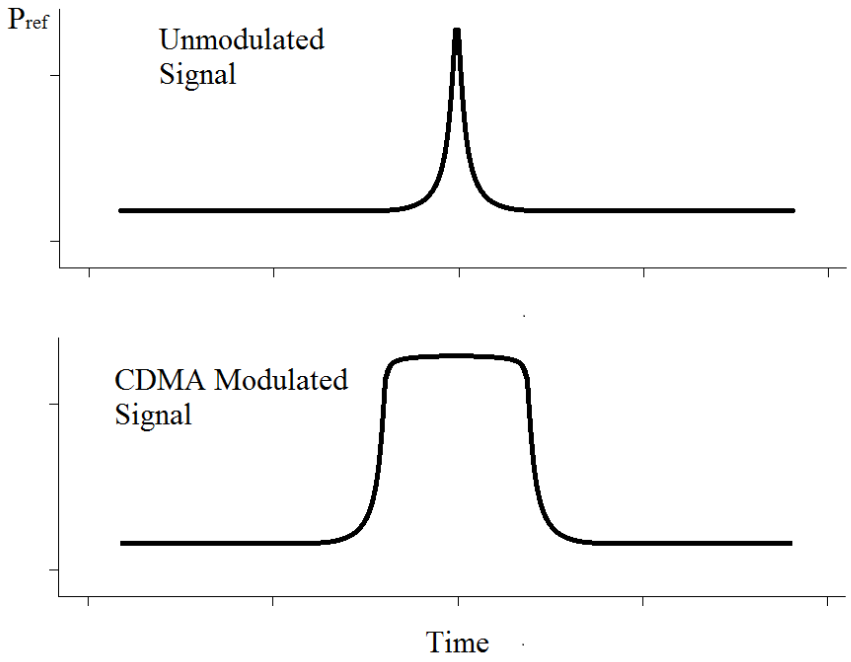


Figure 5.8: Unmodulated vs. CDMA Modulated Signal

Figure 5.9 provides an example ACPR measurement performed on a power spectrum analyzer. In this measurement, a CDMA modulated source is con-

nected directly to a spectrum analyzer. As shown in the plot, this modulated source contains its signal power P_{ref} within a narrow bandwidth (reference channel). One channel away from the reference channel are the lower and upper adjacent channels, which contain the first-order leakage power. Likewise, two channels away from the reference channel (one bandwidth away from the adjacent channels) are the lower and upper alternate channels, which contain the second-order leakage power. Channel bandwidth is defined as the length of the bars (channels).

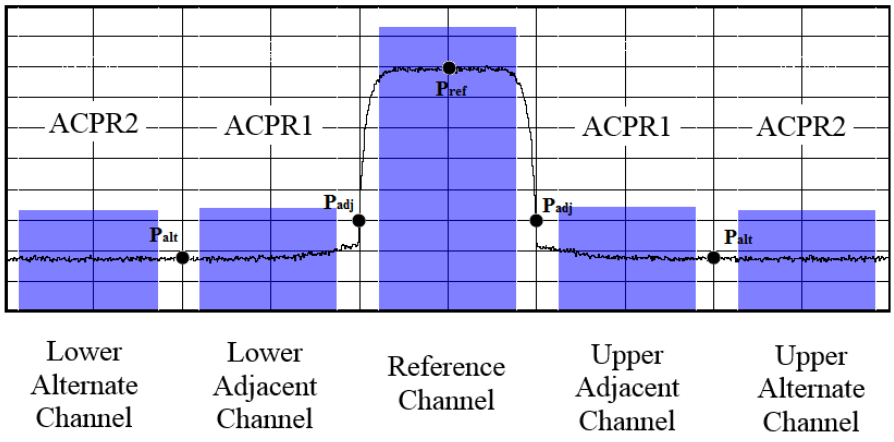


Figure 5.9: ACPR Measurement Example

Equations (5.8) and (5.9) define the expressions for calculating ACPRs (often expressed in dB). Modern power amplifier measurements are performed at a variety of input power levels from -15 to 5 dBm. Typical ACPR1 value falls in the range of -30 to -45 dBc, and ACPR2 value levels in the range of -40 to -65 dBc.

$$ACPR1 = 10 \log \frac{P_{adj}}{P_{ref}} \tag{5.8}$$

$$ACPR2 = 10 \log \frac{P_{alt}}{P_{ref}} \tag{5.9}$$

The reason for wide gap in typical ACPR1 and ACPR2 values is the diverse nature of CDMA modulation. Many CDMA standards exist, two of which are used most often – narrowband CDMA (NB-CDMA) and wideband CDMA (WB-CDMA). It is obvious that NB-CDMA has a narrower reference

channel, whereas WB-CDMA has a broader one. Table 5.1 shows the comparison between two CDMA modulations. Usually WB-CDMA is faster than NB-CDMA modulated signals, but suffers from variety mismatches [48].

Table 5.1: Comparison Between NB-CDMA and WB-CDMA

Modulations	NB-CDMA	WB-CDMA
Channel bandwidth	30 kHz	3.84 MHz
Adjacent channel location (away from carrier)	±885 kHz	±5 MHz
Alternative channel location (away from carrier)	±1.98 MHz	±10 MHz
Typical ACPR1 values	-25 to -35 dBc	-40 to -50 dBc
Typical ACPR2 values	-45 to -55 dBc	-60 to -70 dBc

5.4 Measurement Implementation

So far, all measurement theories and simulation topologies have been introduced. Before moving on to show the lab results, a brief description on measurement environment is well needed.

A power amplifier is essentially a nonlinear device; therefore, to measure a power amplifier's efficiency and linearity, small signal S-parameters measurement is not enough, since it is only suitable for linear systems. Instead, large signal power sweep, output power spectrum and X-parameters measurements should be performed.

5.4.1 Testing Setups

Power Amplifier Measurements Performed

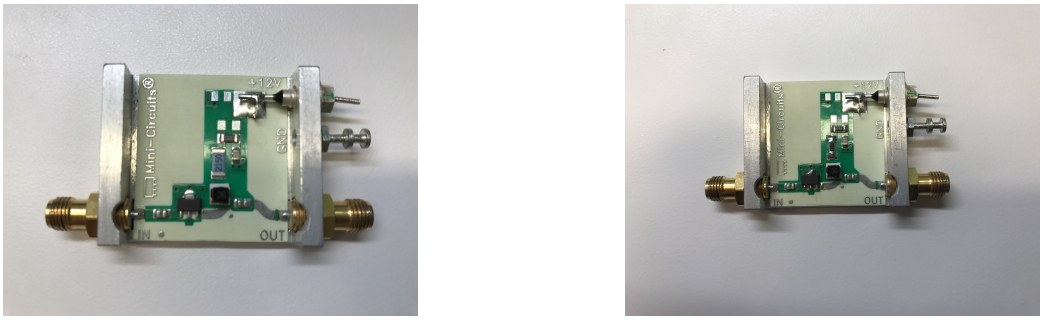
1. Power sweep *(chapter 6)*
2. Output power spectrum with single-tone input *(chapter 7)*
3. Output power spectrum with two-tone input *(chapter 7)*
4. X-parameters *(chapter 8)*

Power Amplifier Tested

1. Surface Mount Monolithic Amplifier DC-8GHz Gali-1+ InGaP HBT microwave wideband amplifier (**Ga1**)
2. Surface Mount Monolithic Amplifier DC-3GHz Gali-S66+ InGaP HBT microwave wideband amplifier (**GaS66**)

Evaluation Board

1. Ga1: TB-409-1+ (Figure 5.10a)
2. GaS66: TB-409-S66+ (Figure 5.10b)



(a) TB-409-1+ (b) TB-409-S66+

Figure 5.10: Evaluation Boards

Input Power and DC Supply Ranges

1. Input power range:
   (a) Ga1: -15 dBm to 5 dBm with 1 dB interval @ 1 GHz
   (b) GaS66: -20 dBm to 5 dBm with 1 dB interval @ 2 GHz
2. DC supply voltage: Both amplifier using 12 V
3. DC current limits:
   (a) Ga1: 40 mA
   (b) GaS66: 16 mA

RF Input Generated Source

1. Power Sweep:
   (a) Agilent E8358A 300 kHz ∼ 9 GHz PNA Series Network Analyzer (Port 1)
2. Output power spectrum with single-tone input:
   (a) HP E4433B 250 kHz ∼ 4 GHz ESG-D Series Signal Generator
3. Output power spectrum with two-tone input:
   (a) HP E4433B 250 kHz ∼ 4 GHz ESG-D Series Signal Generator
   (b) HP E4432B 250 kHz ∼ 3 GHz ESG-D Series Signal Generator
4. X-parameters:
   (a) Agilent N5181B 9 kHz ∼ 6 GHz MXG X-Series Signal Generator
   (b) Agilent U9391C 10 MHz ∼ 26.5 GHz FFM Comb Generator
   (c) Agilent U9391C 10 MHz ∼ 26.5 GHz FFF Comb Generator

DC Supply Source

All tests using Agilent E3648A 0-8 V, 5 A & 0-20 V, 2.5 A Dual Output DC Power Supply.

RF Output analyzed Equipment

1. Power Sweep:
   (a) Agilent E8358A 300 kHz ∼ 9 GHz PNA Series Network Analyzer (Port 2)
2. Output power spectrum with single-tone input:
   (a) Agilent N9020A 20 Hz ∼ 13.6 GHz MXA Signal Analyzer
3. Output power spectrum with two-tone input:
   (a) Agilent N9020A 20 Hz ∼ 13.6 GHz MXA Signal Analyzer

4. X-parameters:

   (a) Agilent N5242A 10 MHz $\sim$ 26.5 GHz PNA-X Network Analyzer

Calibration Kit

1. Power Sweep:

   (a) Agilent 85052D DC to 26.5 GHz 3.5 mm Calibration Kit

2. Output power spectrum with single-tone input:
   No need to calibrate.

3. Output power spectrum with two-tone input:
   No need to calibrate.

4. X-parameters:

   (a) Agilent N4691-60004 300 kHz $\sim$ 26.5 GHz Electronic Calibration Module

   (b) Agilent E4412A 10 MHz $\sim$ 16 GHz, -70 dBm $\sim$ +20 dBm EPM Series Dual-Channel Power Meter

5.4.2 Implementation of Tests Using Vector Network Analyzer

In a linear system, a vector network analyzer (VNA) is mainly used in measuring the S-parameters of the network, whereas in a nonlinear system, a power sweep test using VNA should be performed instead of S-parameters frequency sweep test. In testing a power amplifier, the basic idea behind the power sweep test is to obtain the output power of the amplifier with sweeping its input power. Figure 5.11 displays the measurement setup diagram of test using VNA and Figure 5.12 shows the real measuring environment. Chapter 6 includes all testing results using VNA.

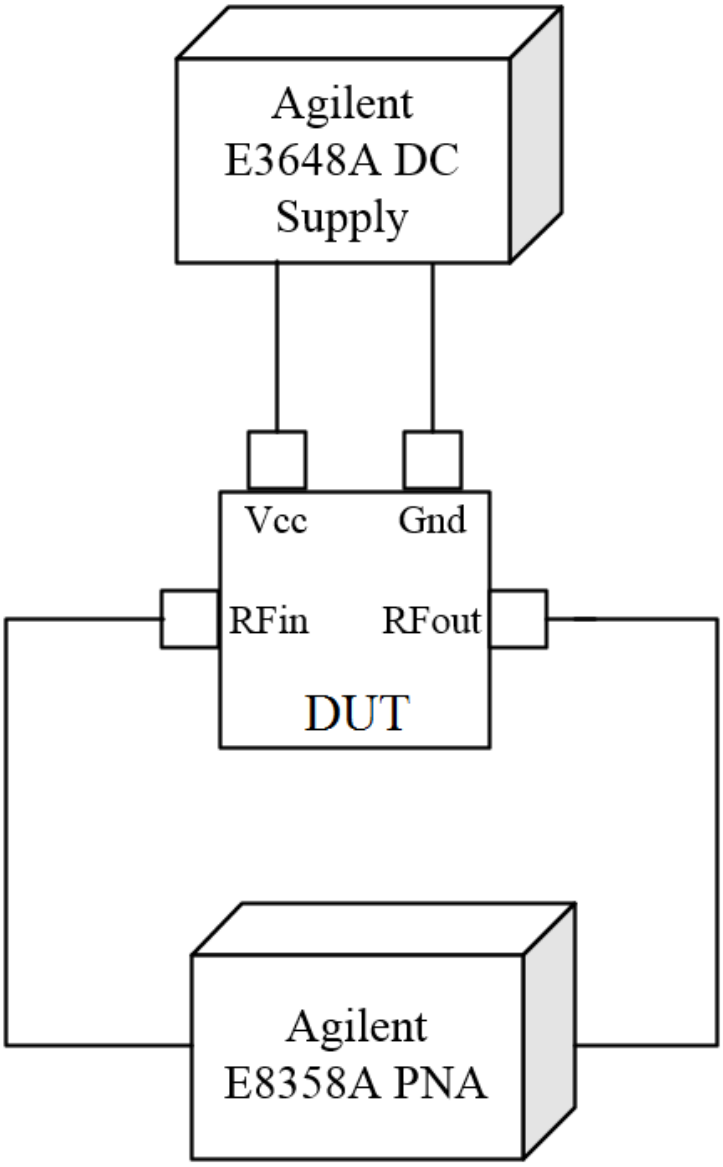


Figure 5.11: Vector Network Analyzer Experiment Setup Diagram

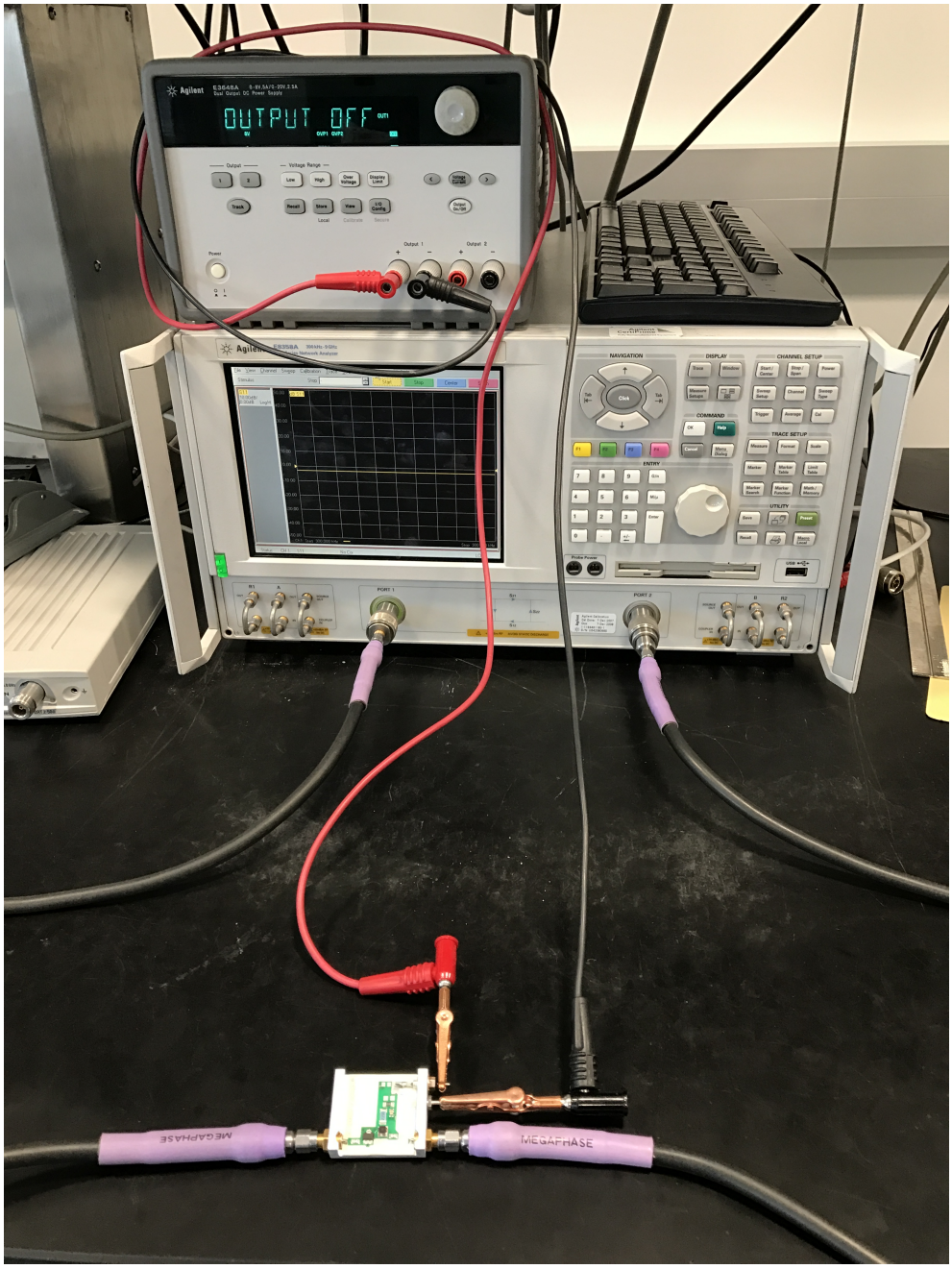


Figure 5.12: Vector Network Analyzer Experiment Setup

5.4.3 Implementation of Tests Using Power Spectrum Analyzer

Power spectrum analyzer (PSA) is a key RF testing equipment that helps the engineer to test the linearity of s system. Unlike a vector network analyzer,

it measures the power level of an input signal over its operating frequency range. The power levels of both known and unknown signals can be measured through PSA. In testing a power amplifier, PSA can measure all linearity parameters, such as ACLR for WCDMA, E-UTRA for LTE, and ACPR for CDMA2K, so long as digitally modulated input signals are able to generate from an electric signal generator (ESG). In this thesis, output power spectra based on single-tone and two-tone are measured through PSA. Figure 5.13 displays the measurement setup diagram of the two-tone input test using PSA, and Figure 5.14 shows the real measuring environment. Chapter 7 includes all testing results using PSA.

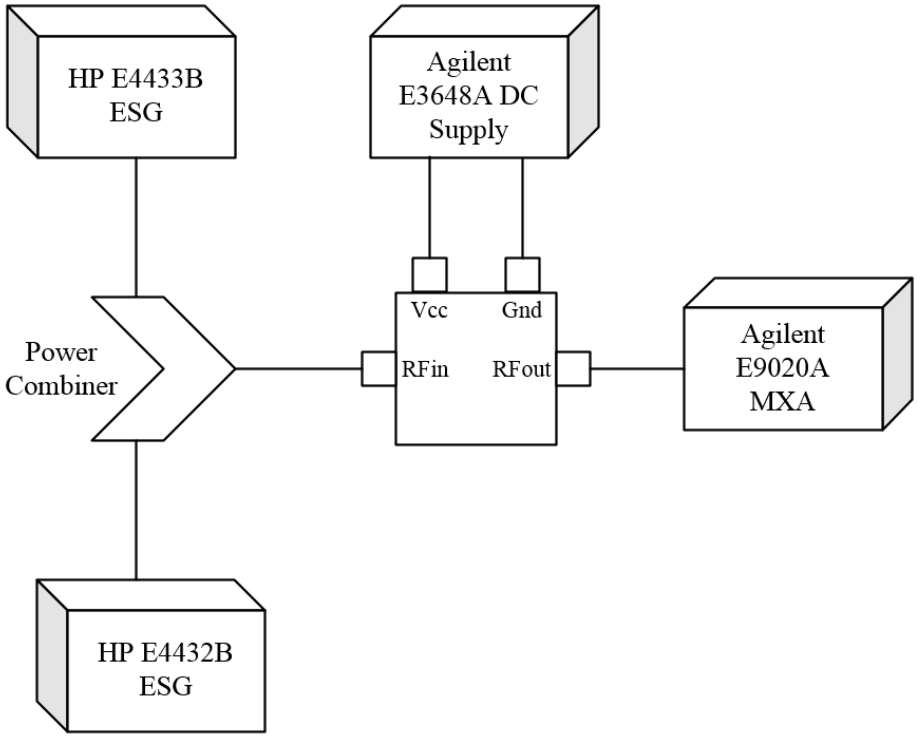


Figure 5.13: Power Spectrum Analyzer Experiment Setup Diagram

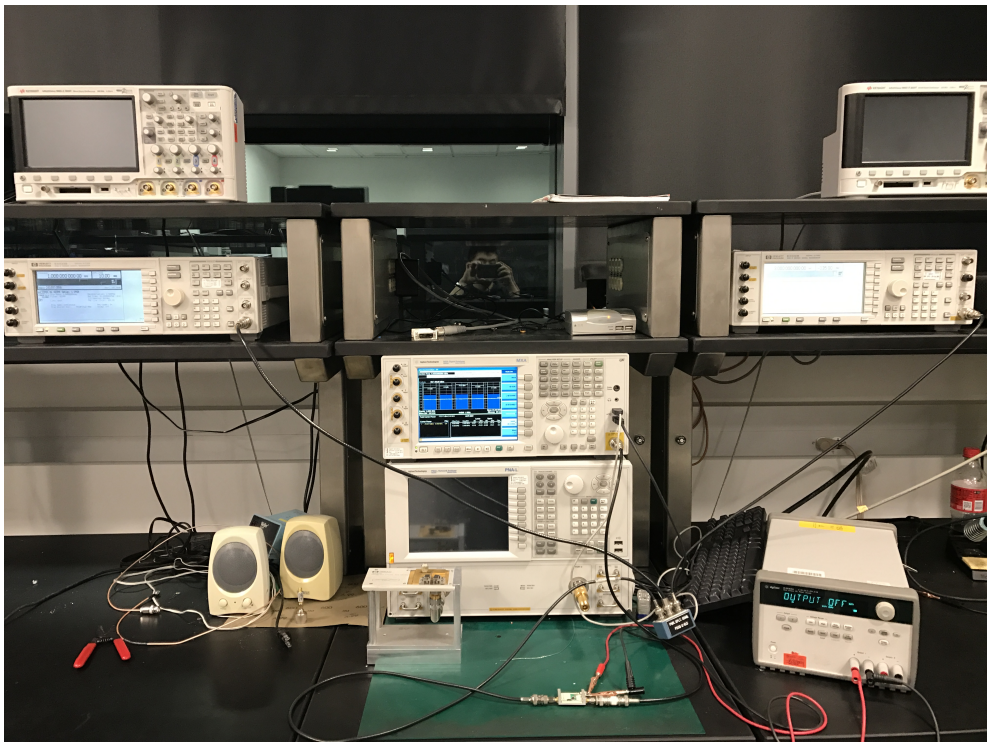


Figure 5.14: Power Spectrum Analyzer Experiment Setup

5.4.4 Implementation of Tests Using PNA-X

PNA-X is the newest and most sophisticated network analyzer Agilent has introduced so far. It is mainly used to measure the X-parameters of a system. X-parameters, often applied to characterize the poly-harmonic distortion nonlinear behavioral model, is the mathematically correct superset and the natural extension of S-parameters to nonlinear devices under large signal input [50]. Precise and detailed X-parameters properties and equations can be found in Root's book [51]. X-parameters, like an IBIS model, can help designers to model the entire large signal behavior of a power amplifier in simulation. However, the process of obtaining the X-parameters is long and complicated. Figure 5.15 shows the measurement setup diagram of obtaining X-parameters. Comb generator and power meter on the right bottom of the diagram work primarily for calibrating the electric signal generator. Figure 5.16 shows the real measuring environment. Chapter 8 includes all testing results using PNA-X.

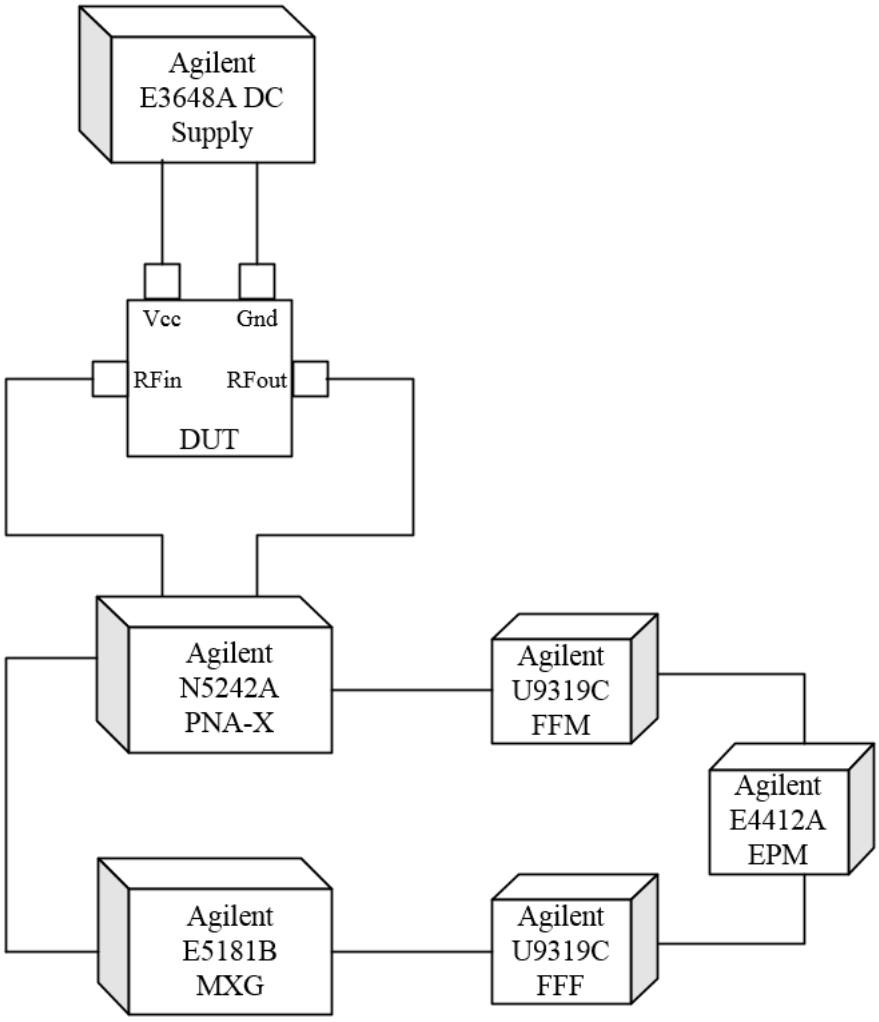


Figure 5.15: X-Parameters Network Analyzer Experiment Setup Diagram

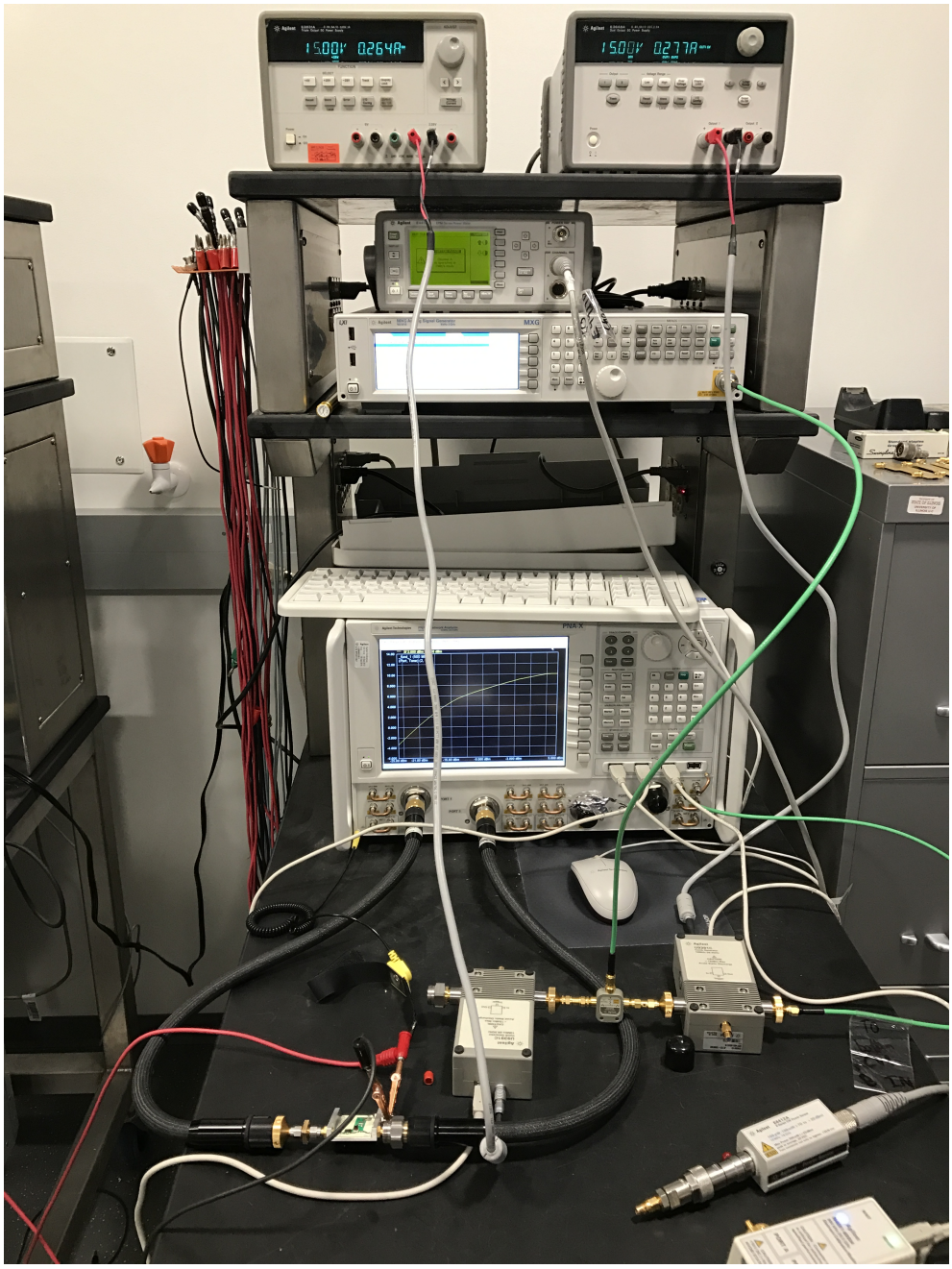


Figure 5.16: X-Parameters Network Analyzer Experiment Setup

CHAPTER 6

MEASUREMENT RESULTS USING VECTOR NETWORK ANALYZER

This chapter contains two parts: measurement and simulation of nonlinear characteristic of power amplifiers. Experimental results include gain, power added efficiency (PAE), and 1 dB compression point (1 dB CP).

6.1 Measurement Results

6.1.1 Measurement Results on Gali-1+ HBT Power Amplifier

This section contains the VNA measurement results on Gali-1+ HBT Power Amplifier. Firstly, equations used to plot various PA parameters are listed in equations (6.1), (6.2) and (6.3). Then, PA Gain vs. Pin, Pout vs. Pin, and PAE vs. Pin are shown in Figures 6.1, 6.2, and 6.3, respectively. Lastly, PA 1 dB compression point calculation method is shown in Figure 6.4.

$$P_{out} = P_{in} + Gain \tag{6.1}$$

$$P_{dc} = 3.4\ V * 0.04\ A \tag{6.2}$$

$$PAE = 100 * (dbmtow(P_{out}) - dbmtow(P_{in}))/P_{dc} \tag{6.3}$$

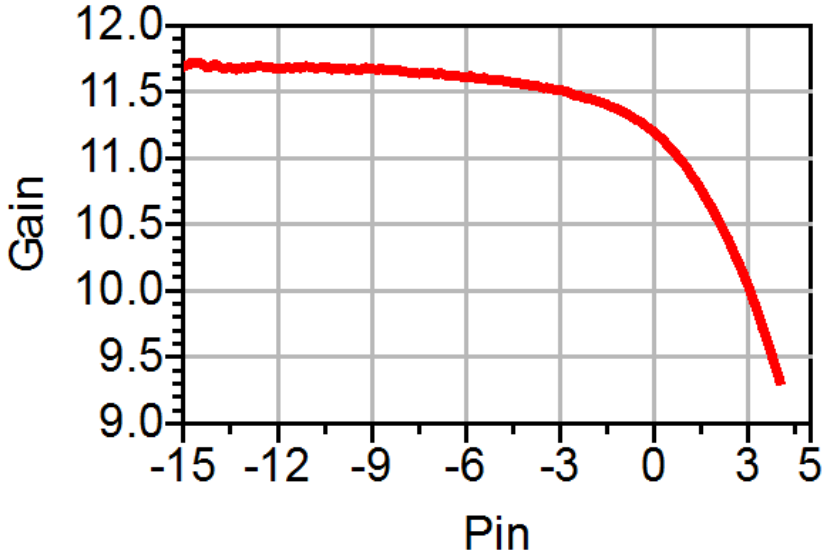


Figure 6.1: Gain of Gali-1+ HBT Power Amplifier

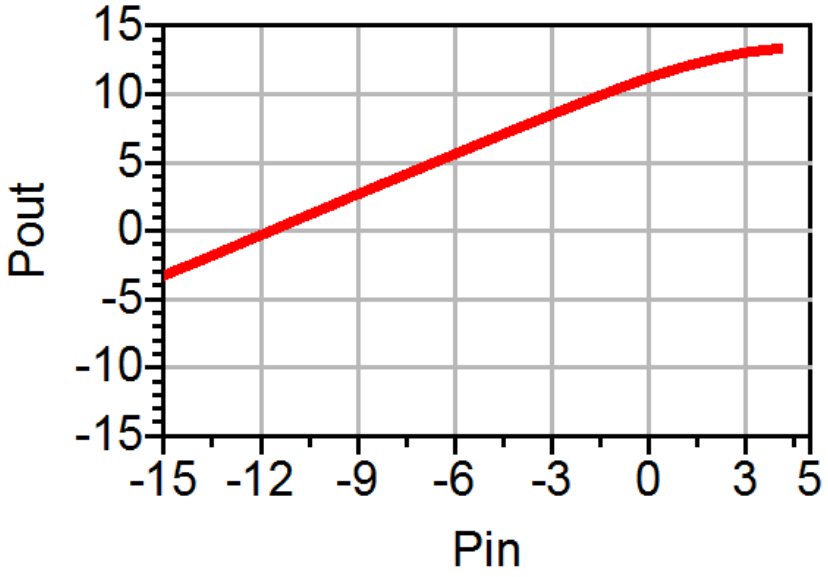


Figure 6.2: Output Power of Gali-1+ HBT Power Amplifier

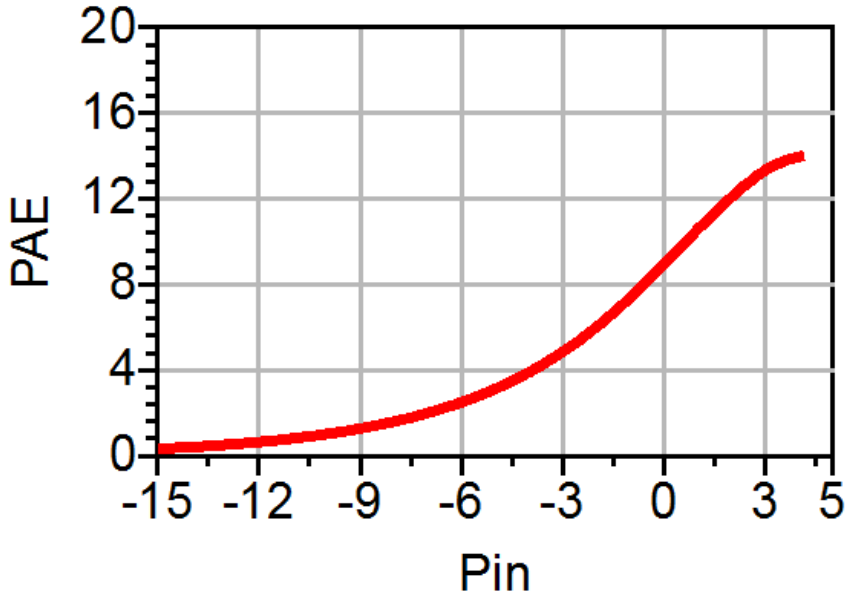


Figure 6.3: Power Added Efficiency of Gali-1+ HBT Power Amplifier

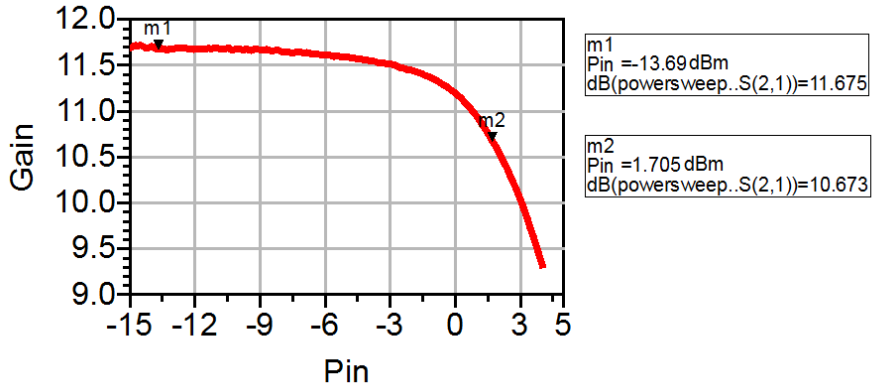


Figure 6.4: 1 dB Compression Point of Gali-1+ HBT Power Amplifier

6.1.2 Measurement Results on Gali-S66+ HBT Power Amplifier

This section contains the VNA measurement results on Gali-S66+ HBT Power Amplifier. Firstly, PA Gain vs. Pin, Pout vs. Pin, and PAE vs. Pin are shown in Figures 6.5, 6.6, and 6.7, respectively. Then PA 1 dB compression point calculation method is shown in Figure 6.8. Lastly, a performance

comparison between the two PAs is summarized in Table 6.1.

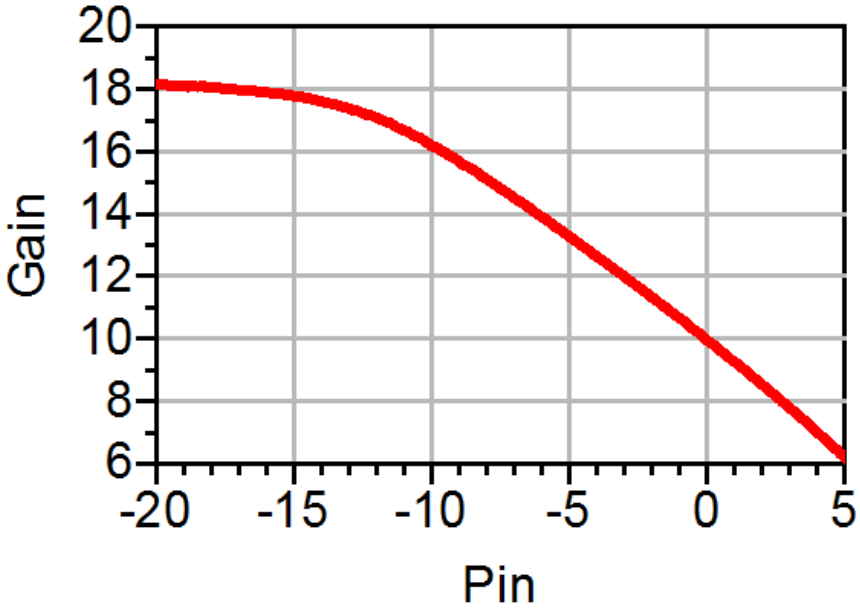


Figure 6.5: Gain of Gali-S66+ HBT Power Amplifier

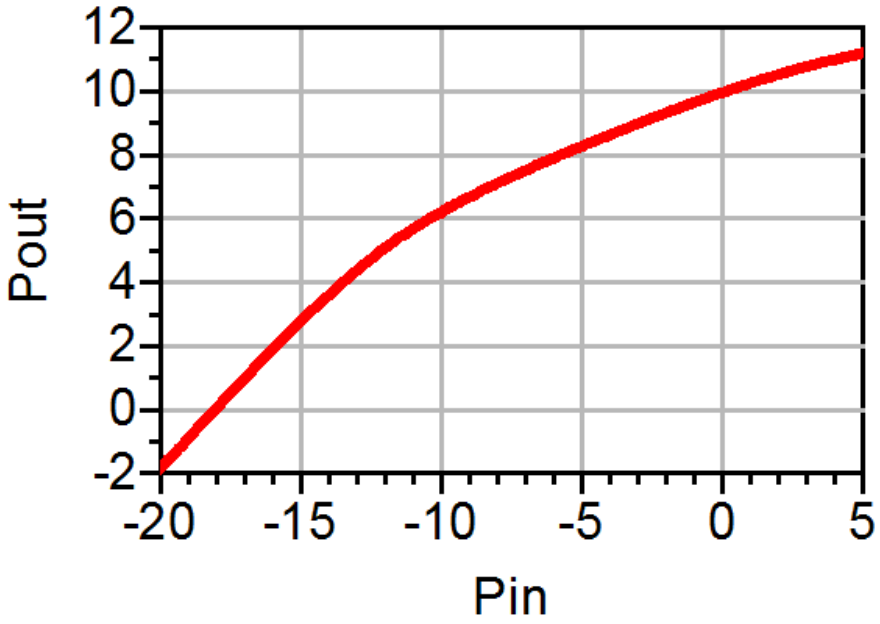


Figure 6.6: Output Power of Gali-S66+ HBT Power Amplifier

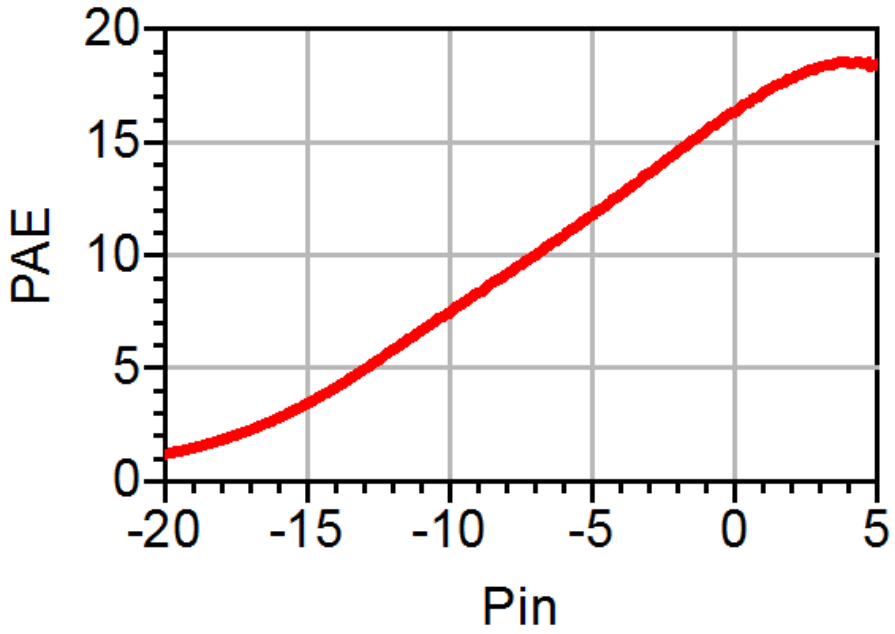


Figure 6.7: Power Added Efficiency of Gali-S66+ HBT Power Amplifier

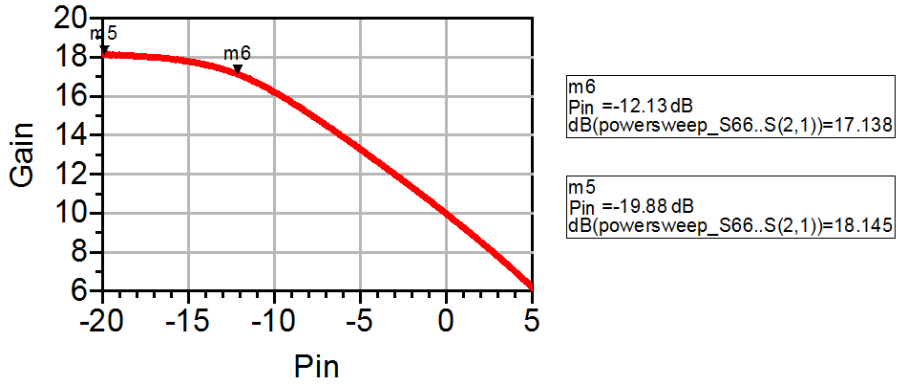


Figure 6.8: 1 dB Compression Point of Gali-S66+ HBT Power Amplifier

Table 6.1: Gali-1+ vs. Gali-S66+ HBT Power Amplifier Performance Summary

Parameters	Gali-1+	Gali-S66+	Pin
Gain	11.7 dB	17.8 dB	-15 dBm
Gain	11.2 dB	9.9 dB	0 dBm
Pout	-3.3 dBm	2.8 dBm	-15 dBm
Pout	11.2 dBm	9.9 dBm	0 dBm
PAE	8.871%	16.4%	0 dBm
PAEmax	13.962%	18.5%	5 dBm
1 dB CP	10.7 dB @ 1.7 dBm	17.1 dB @ -12.1 dBm	NA

Clearly, compared to Ga1, GaS66 has a better performance in power gain and efficiency, but it suffers from huge nonlinearity effect (gain compressed quickly at -12.13dBm). This phenomenon indicates that there is always a trade-off between linearity and efficiency in designing power amplifiers. Engineers should choose correctly depending on the design goals.

6.2 Comparing with ADS Circuit Simulation

6.2.1 ADS Simulation Schematic on Gali-1+ HBT Power Amplifier

This section contains the necessary circuit schematics for ADS simulation. Figure 6.9 shows the transistor level schematic of the TB-409-S1+ evaluation board; Figure 6.10 displays the circuit level schematic of the entire simulation. A 65 Ω resistor is added in the schematic for attenuation purpose.

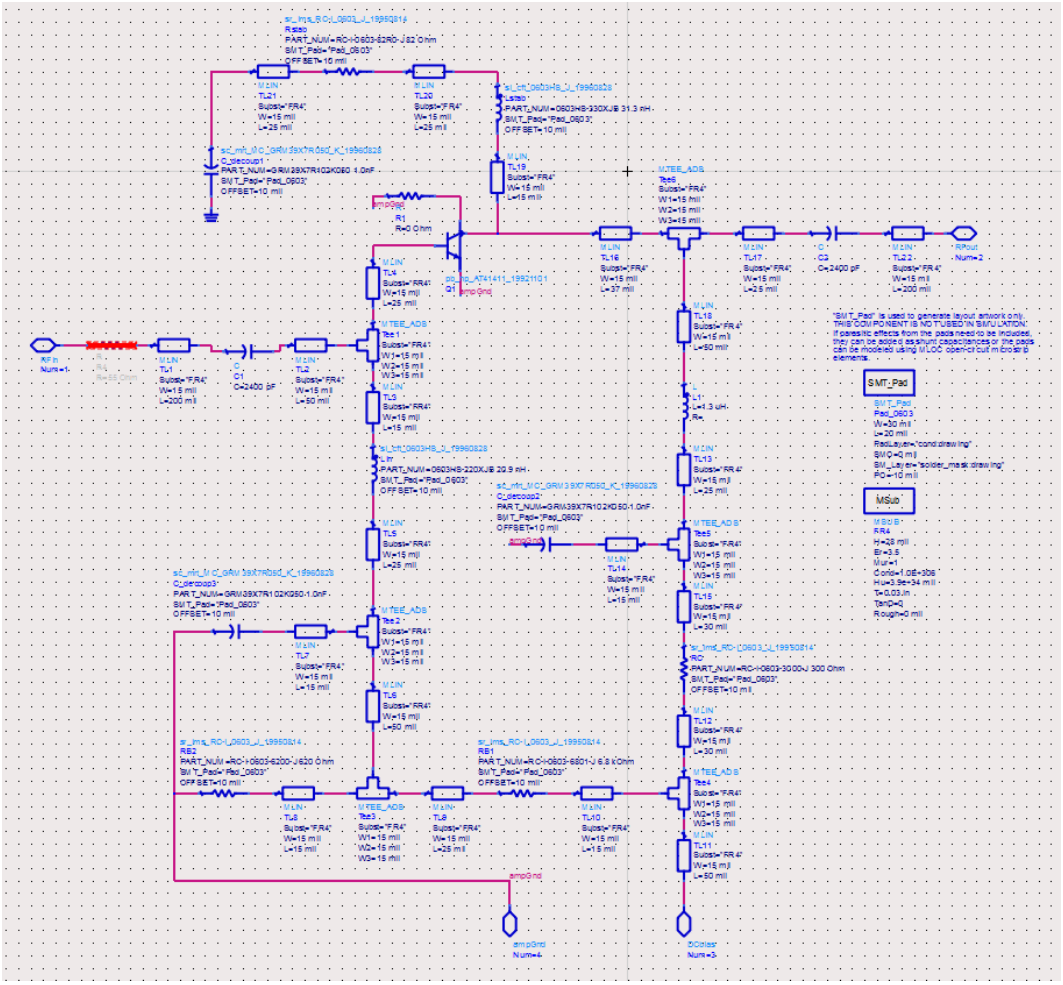


Figure 6.9: Gali-1+ HBT Power Amplifier Transistor Level Schematic

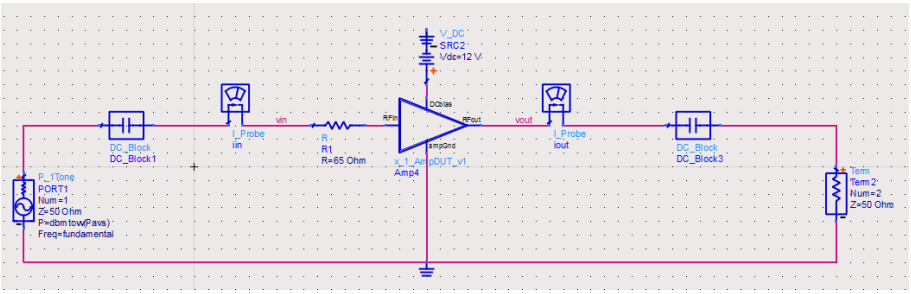


Figure 6.10: ADS Circuit Level Schematic

6.2.2 Comparison Results on Gali-1+ HBT Power Amplifier

This section contains the comparison results between VNA measurement and ADS circuit simulation on Gali-1+ HBT Power Amplifier. Firstly, PA

Gain vs. Pin, Pout vs. Pin, and PAE vs. Pin comparisons are shown in Figures 6.11, 6.12, and 6.13, respectively. Then PA 1 dB compression point comparison is shown in Figure 6.14. Lastly, a performance summary between simulation and measurement at various input power is listed in Table 6.2.

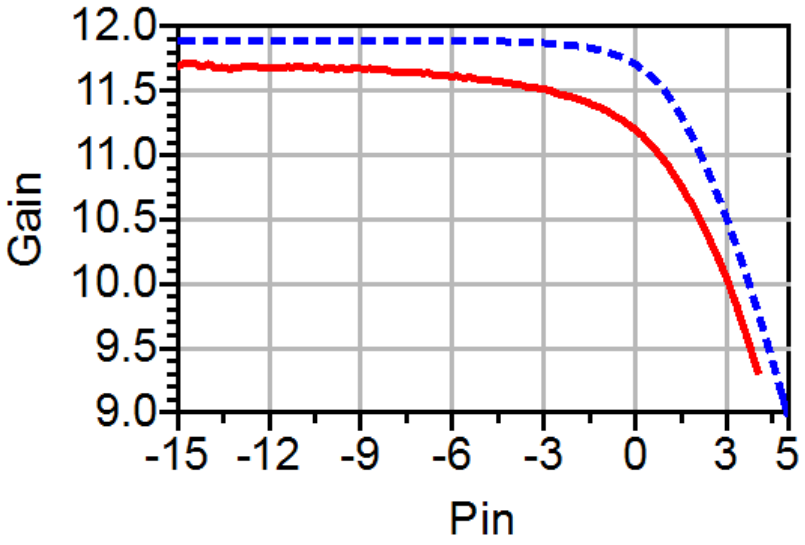


Figure 6.11: Gain Comparison on Measurement (Red) vs. Simulation (Blue Dot)

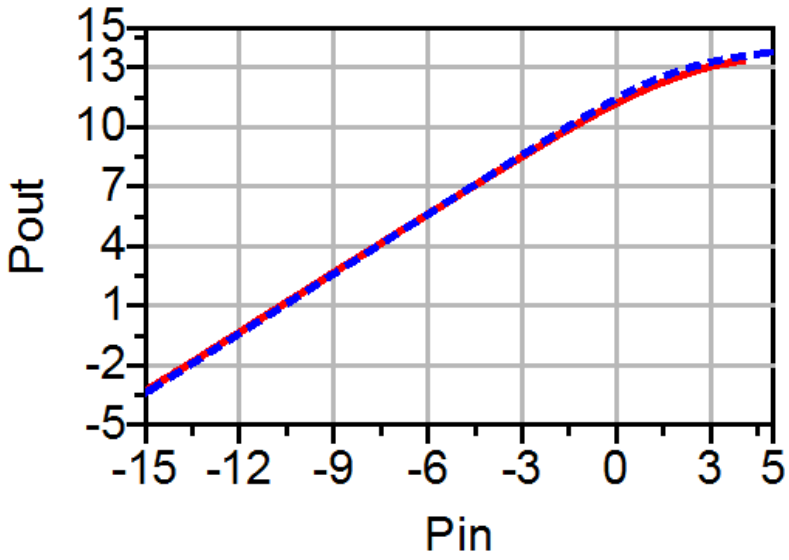


Figure 6.12: Output Power Comparison on Measurement (Red) vs. Simulation (Blue Dot)

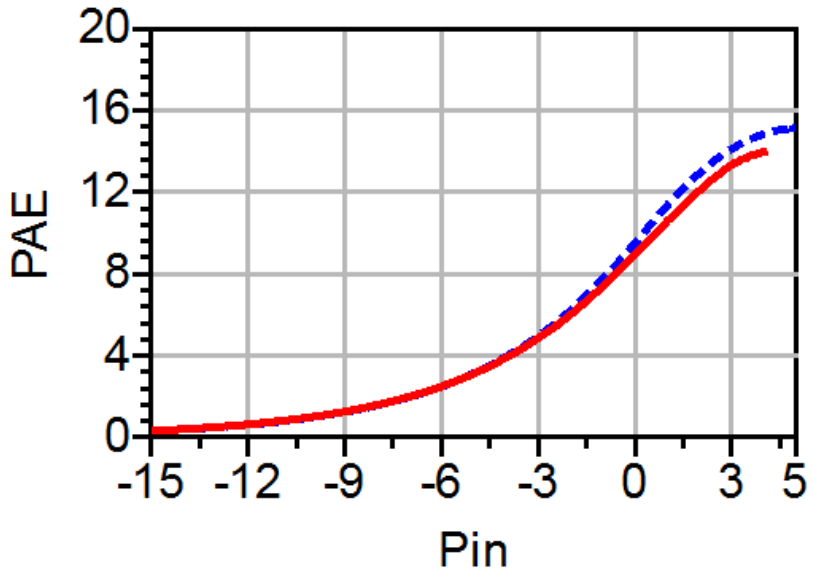


Figure 6.13: Power Added Efficiency Comparison on Measurement (Red) vs. Simulation (Blue Dot)

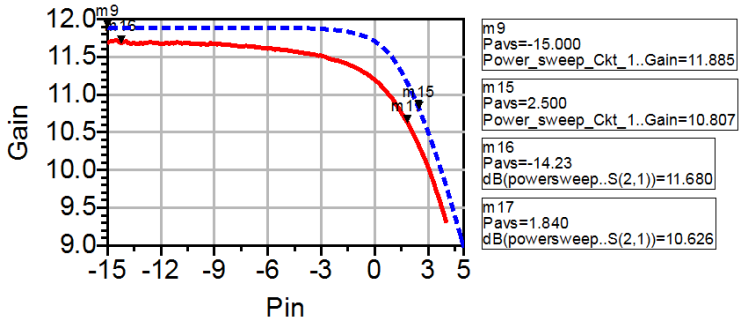


Figure 6.14: 1 dB Compression Point on Measurement (Red) vs. Simulation (Blue Dot)

Table 6.2: Gali-1+ HBT Power Amplifier Comparison Summary

Parameters	Measured value	Simulation value	Pin
Gain	11.7 dB	11.9 dB	-15 dBm
Gain	11.2 dB	11.8 dB	0 dBm
Pout	-3.3 dBm	-3.1 dBm	-15 dBm
Pout	11.2 dBm	11.8 dBm	0 dBm
PAE	8.871%	10.593%	0 dBm
PAEmax	13.962%	20.973%	5 dBm
1 dB CP	10.6 dB @ 1.8 dBm	10.8 dB @ 2.5 dBm	NA

CHAPTER 7

MEASUREMENT RESULTS USING POWER SPECTRUM ANALYZER

This chapter contains two parts: measurement and simulation of nonlinear characteristic of power amplifiers. Experimental results include two-tone third-order inter-modulation distortion (IMD) test, third-order input and output interception points (IIP3 & OIP3), and adjacent/alternate channel power ratio (ACPR1/ACPR2) under narrow-band and wide-band code division multiple access (NB-CDMA & WB-CDMA) digital modulation.

7.1 Measurement Results

7.1.1 Measurement Results on Gali-1+ HBT Power Amplifier

This section contains the PSA measurement results on Gali-S1+ HBT Power Amplifier. Figure 7.1 shows the power spectrum vs. frequency of a two-tone input signal at 1 dBm. Two signals are closely centered at 1 GHz at a distance of 2 MHz apart, i.e. 0.999 GHz and 1.001 GHz. Besides these two fundamental tones, all others are degenerated from PA nonlinearity. Table 7.1 summarizes the nonlinear terms and their corresponding frequencies in the plot.

Table 7.1: PA Nonlinear Term vs. Frequency

Nonlinear Term	Frequency
$2f_1 - f_2$	0.999 GHz
$2f_2 - f_1$	1.001 GHz
$3f_1 - 2f_2$	0.997 GHz
$3f_2 - 2f_1$	1.003 GHz
$4f_1 - 3f_2$	0.995 GHz
$4f_2 - 3f_1$	1.005 GHz
$5f_1 - 4f_2$	0.993 GHz
$5f_2 - 4f_1$	1.007 GHz
$6f_1 - 5f_2$	0.991 GHz
$6f_2 - 5f_1$	1.009 GHz

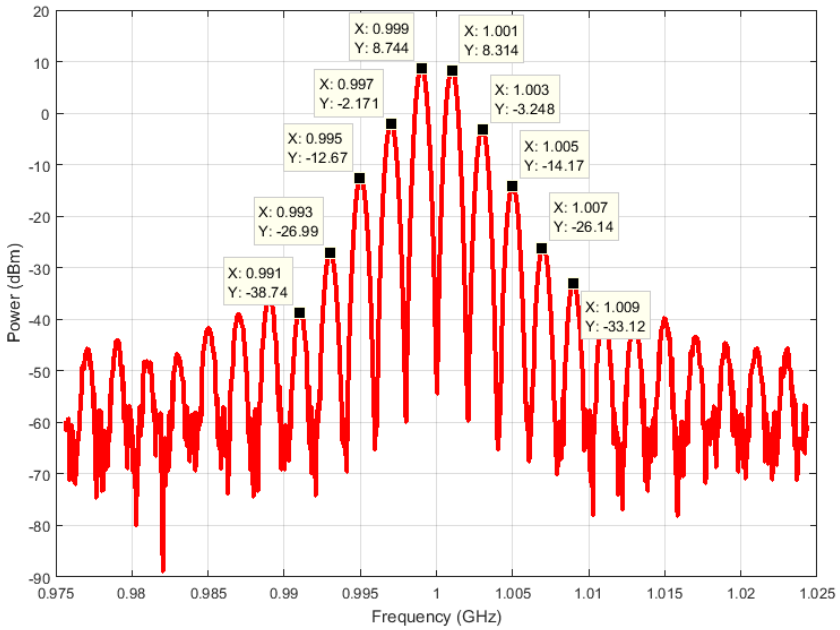


Figure 7.1: Gali-1+ Power Spectrum of Two-Tone Input Signal Centered at 1 GHz

Figure 7.2 shows the two-tone third-order IMD IIP3/OIP3 for Gali-1+ amplifier. Figures 7.3 and 7.4 contain ACPR measurements on Gali-1+ PA with NB-CDMA and WB-CDMA modulated input signals, respectively.

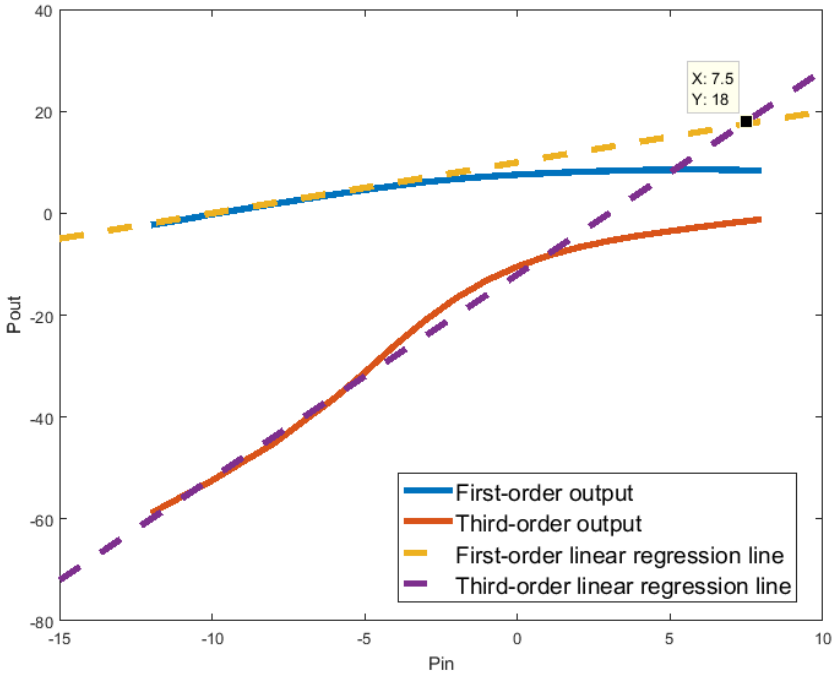


Figure 7.2: Gali-1+ Two-Tone Third-Order IMD Input/Output Interception Point

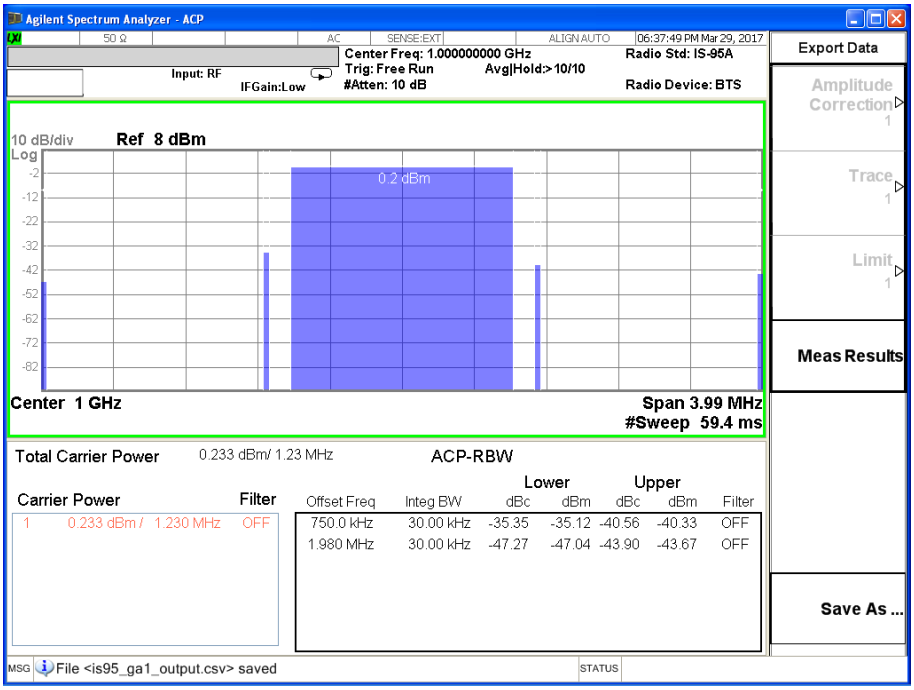


Figure 7.3: Gali-1+ ACPR under NB-CDMA Digital Modulated Input Signal at -10 dBm

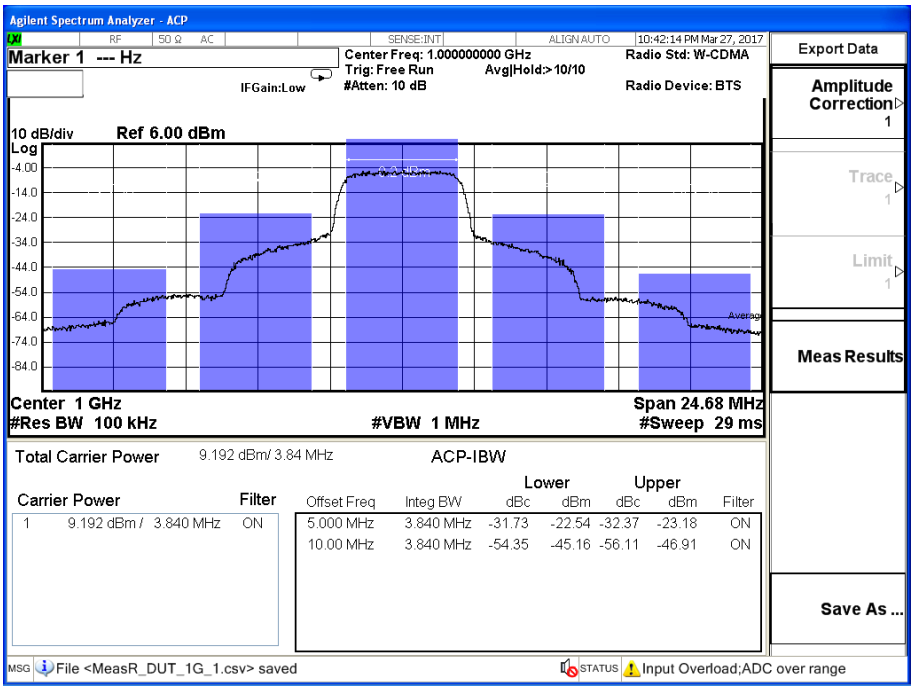


Figure 7.4: Gali-1+ ACPR under WB-CDMA Digital Modulated Input Signal at -10 dBm

7.1.2 Measurement Results on Gali-S66+ HBT Power Amplifier

This section contains the PSA measurement results on Gali-S66+ HBT Power Amplifier. Figure 7.5 shows the power spectrum vs. frequency of a two-tone input signal at -15 dBm. Two signals are closely centered at 2 GHz with a distance of 2 MHz apart, i.e. 1.999 GHz and 2.001 GHz. Besides these two fundamental tones, all others are degenerated from PA nonlinearity. Table 7.2 summarizes the nonlinear term and its corresponding frequencies in the plot.

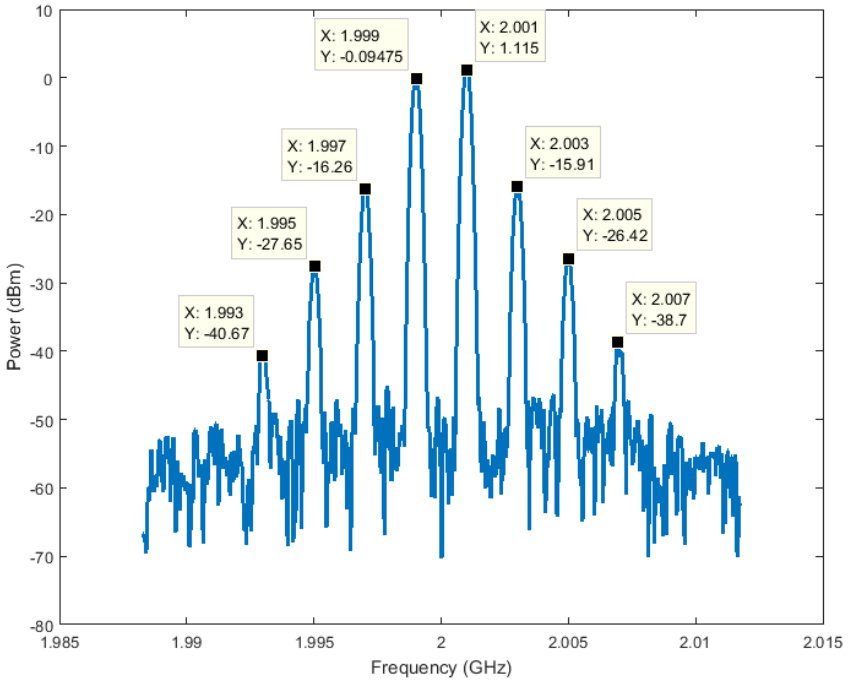


Figure 7.5: Gali-S66+ Power Spectrum of Two-Tone Input Signal Centered at 2 GHz

Table 7.2: PA Nonlinear Term vs. Frequency

Nonlinear Term	Frequency
$2f_1 - f_2$	1.999 GHz
$2f_2 - f_1$	2.001 GHz
$3f_1 - 2f_2$	1.997 GHz
$3f_2 - 2f_1$	2.003 GHz
$4f_1 - 3f_2$	1.995 GHz
$4f_2 - 3f_1$	2.005 GHz
$5f_1 - 4f_2$	1.993 GHz
$5f_2 - 4f_1$	2.007 GHz
$6f_1 - 5f_2$	1.991 GHz
$6f_2 - 5f_1$	2.009 GHz

Figure 7.6 shows the two-tone third-order IMD IIP3/OIP3 for Gali-S66+ amplifier. Figures 7.7 and 7.8 contain ACPR measurements on Gali-S66+ PA with NB-CDMA and WB-CDMA modulated input signals, respectively.

Lastly, a performance comparison between the two PAs is summarized in Table 7.3.

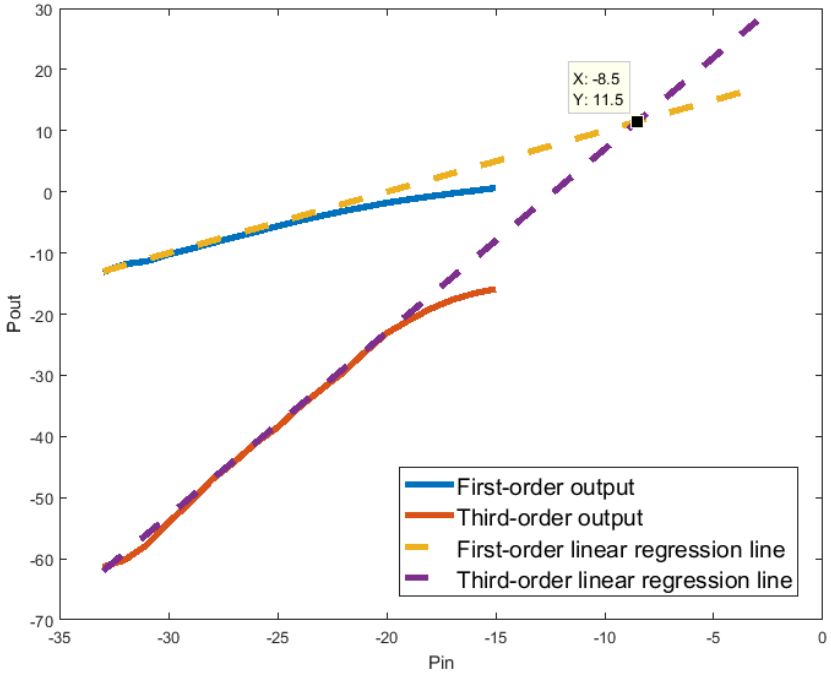


Figure 7.6: Gali-S66+ Two-Tone Third-Order IMD Input/Output Interception Point

Figure 7.7: Gali-S66+ ACPR under NB-CDMA Digital Modulated Input Signal at -13 dBm

Figure 7.8: Gali-S66+ ACPR under WB-CDMA Digital Modulated Input Signal at -13 dBm

Table 7.3: Gali-1+ vs. Gali-S66+ HBT Power Amplifier Performance Summary

Parameters	Gali-1+	Gali-S66+
IIP3	7.5 dBm	-8.5 dBm
OIP3	18 dBm	11.5 dBm
ACPR1 (NB-CDMA)	-35.35 dBc	-35.53 dBc
ACPR2 (NB-CDMA)	-47.27 dBc	-49.31 dBc
ACPR1 (WB-CDMA)	-31.73 dBc	-28.81 dBc
ACPR2 (WB-CDMA)	-54.35 dBc	-49.89 dBc

So far, linearity and efficiency of the power amplifier have both been tested. From Tables 6.1 and 7.3, it can be safely concluded that both Gali power amplifiers belong to the family of class A. Also, Ga1 possess a better linearity than GaS66, whereas GaS66 has a greater efficiency performance. Thus, in real life, it is up to the engineers to decide what to trade off between these two key parameters.

7.2 Comparing with ADS Circuit Simulation

Measurement results will be compared with ADS simulations in this section. Generally these two are not correlating well due to the limitation of circuit simulation. To remedy this, an X-parameters dataset model will be introduced and used in the comparison as well. This dataset model is generated from the circuit but is more related to a real life model. Detailed explanations and measurements on X-parameters will be presented in the next chapter.

7.2.1 ADS Simulation Schematic on Gali-1+ HBT Power Amplifier

This section contains the necessary circuit schematics and equations for ADS simulation. Figure 7.9 shows the circuit level schematic for inter-modulation distortion (IMD) test; Figure 7.10 displays the circuit level schematic for adjacent channel power ratio (ACPR) test. Furthermore, equations (7.1) and (7.2) are used to calculate interception points in IMD test and equations (7.3) to (7.7) are used to calculate input and output ACPRs.

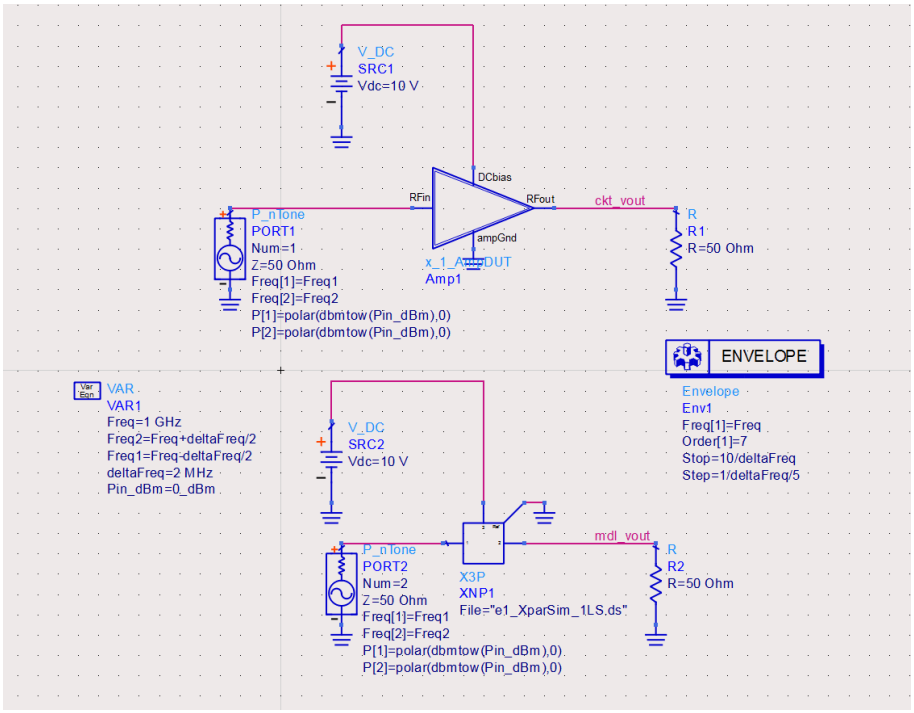


Figure 7.9: ADS Schematics: Circuit (Top) and Dataset Model (Bottom)

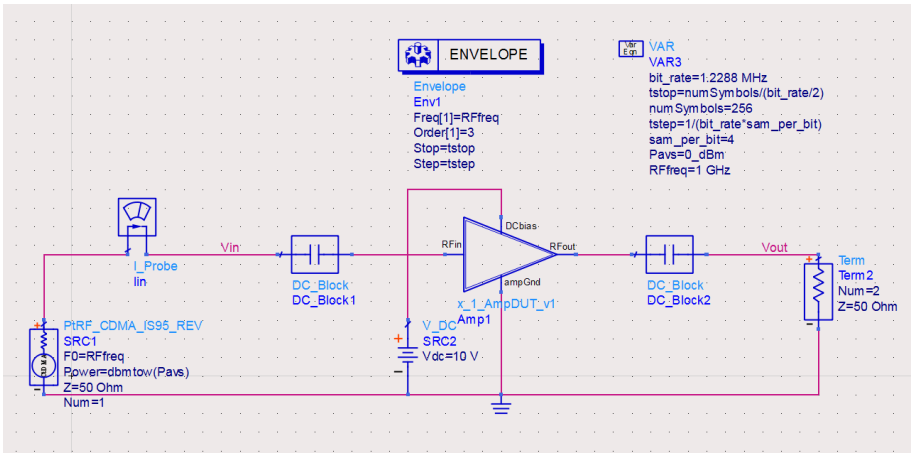


Figure 7.10: ADS Schematics: Test for ACPR

$$OIP3_{dBm} = P_{fundamental} + \frac{(P_{fundamental} - P_{third})}{2} \tag{7.1}$$

$$IIP3_{dBm} = OIP3_{dBm} - Gain_{dB} \tag{7.2}$$

$$
\begin{aligned}
referch &= \{-(1.23\ MHz/2), (1.23\ MHz/2)\} && (7.3)\\
doch &= \{885\ kHz, 915\ kHz\} && (7.4)\\
upch &= \{-915\ kHz, -885\ kHz\} && (7.5)\\
ACPR_{out} &= acpr_{vr}(V_{out}[1], 50, referch, doch, upch, \text{“}Keiser\text{”}) && (7.6)\\
ACPR_{in} &= acpr_{vr}(V_{in}[1], 50, referch, doch, upch, \text{“}Keiser\text{”}) && (7.7)
\end{aligned}
$$

7.2.2 Comparison Results on Gali-1+ HBT Power Amplifier

This section contains the comparison results between PSA measurement and ADS circuit simulation on Gali-1+ HBT Power Amplifier. Firstly, power spectrum vs. frequency comparison is shown in Figure 7.11. Then IIP3 and OIP3 comparison is shown in Table 7.4. Lastly, circuit model simulation of ACPR under NB-CDMA digitally modulated signal is shown in Figure 7.12; measurement result is displayed in Figure 7.13; and the comparison between simulation and measurement is summarized in Table 7.5.

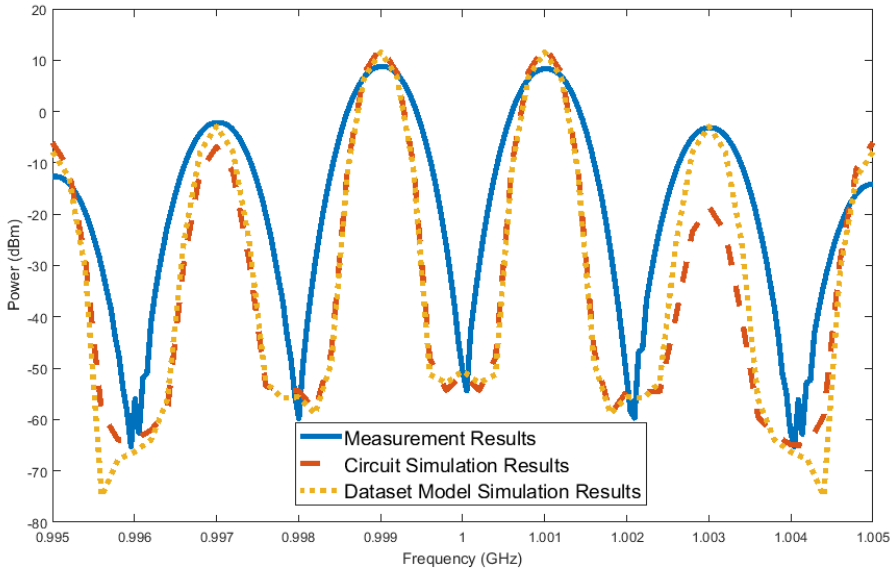


Figure 7.11: Power Spectrum Comparison on Measurement vs. Simulation

Table 7.4: IIP3 and OIP3 Comparison on Measurement vs. Simulation

Models	IIP3	OIP3
Measurements	7.5 dBm	18.0 dBm
Circuit model	12.2 dBm	22.4 dBm
Dataset model	8.3 dBm	18.8 dBm

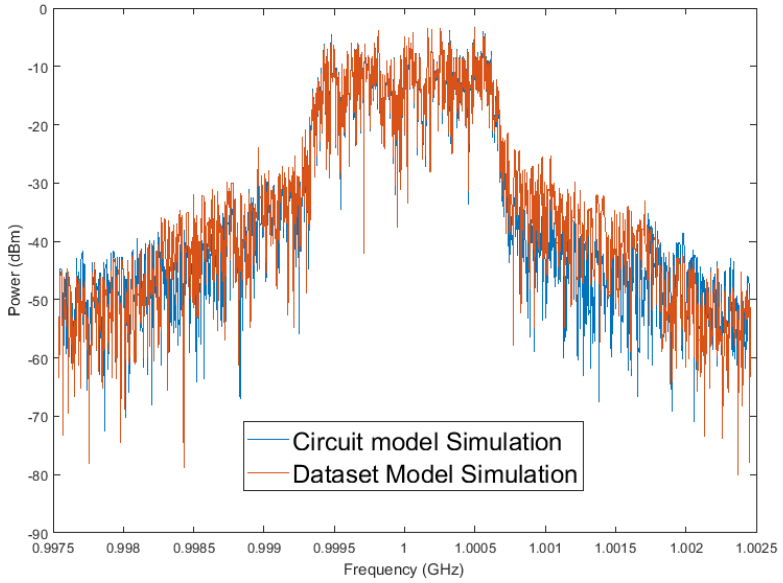


Figure 7.12: ACPR under NB-CDMA Digital Modulated Input Signal at -10 dBm Simulation Results

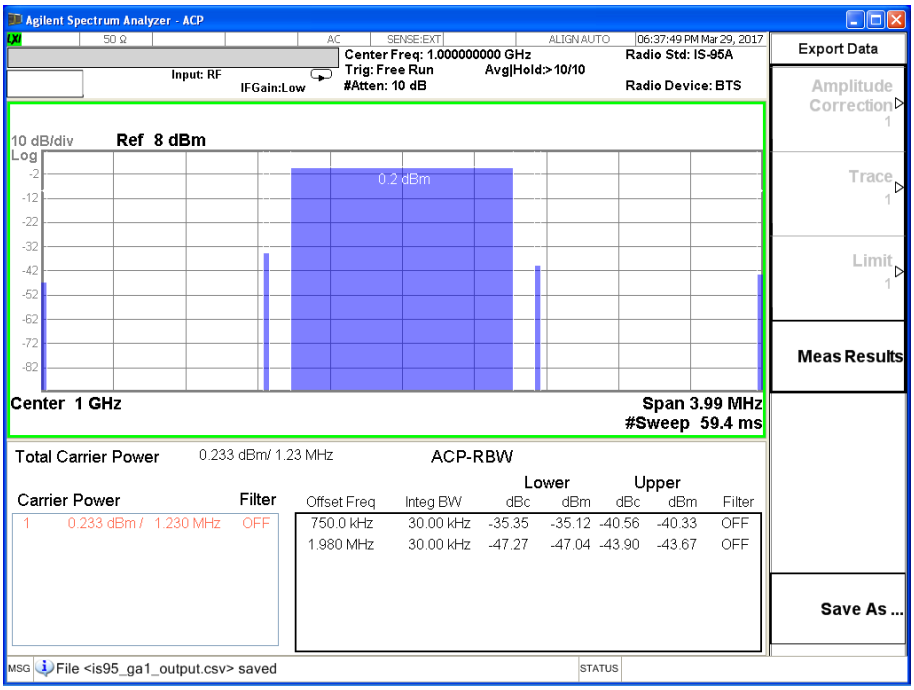


Figure 7.13: Gali-1+ ACPR under NB-CDMA Digital Modulated Input Signal at -10 dBm

Table 7.5: ACPR1 Comparison on Measurement vs. Simulation

Models	ACPR1 lower	ACPR1 upper
Measurements	-35.35 dBc	-40.56 dBc
Circuit model	-41.15 dBc	-41.15 dBc
Dataset model	-38.06 dBc	-38.06 dBc

From two-tone third-order IMD test correlation, it can be safely concluded that the X-parameters dataset model is more accurate than the circuit model. However, in ACPR comparison, clearly, the circuit model has a better comparison result. WB-CDMA should have similar behavior to NB-CDMA on ACPR1 performance. In modern wireless communication, ACPR is the most powerful measurement for linearity. Thus every graduate student who would like to pursue his/her career in RF, should know the basic concept and measurement method behind ACPR.

CHAPTER 8

MODELING PA NONLINEAR BEHAVIOR USING X-PARAMETERS

X-parameters can be measured in the lab with a nonlinear vector network analyzer (NVNA), referred to as PNA-X in this thesis [52]. As discussed in previous chapters, X-parameters is a large signal parameter and is often used to characterize the nonlinear behavior of a power amplifier. Therefore, all PA nonlinear measurements performed with VNA and PSA can be modeled with X-parameters. In this chapter, initially, X-parameters model, obtained from NVNA (PNA-X), is used to compare with the power sweep measurements from VNA and check if there is an agreement between two measurements. Then, this X-parameters model is also used to compare with the power spectrum measurements from PSA and check to see the agreement.

8.1 Comparing PNA-X X-Parameters Model with VNA Measurements

8.1.1 Comparison Results on Gali-1+ HBT Power Amplifier

This section contains the comparison results between PNA-X X-parameters model and VNA measurements on Gali-1+ HBT Power Amplifier. Firstly, PA Gain vs. Pin, Pout vs. Pin, and PAE vs. Pin comparisons are shown in Figures 8.1, 8.2, and 8.3, respectively. Then PA 1 dB compression point comparison is shown in Figure 8.4.

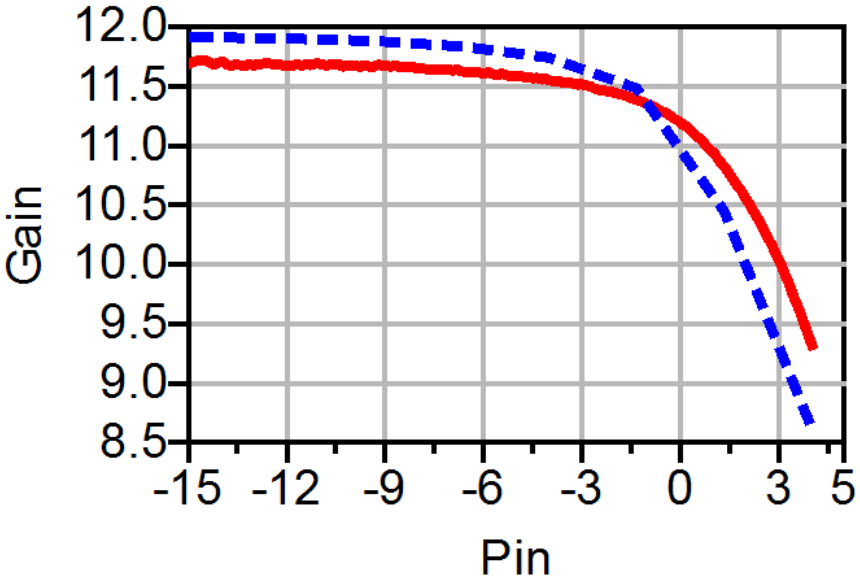


Figure 8.1: Gain Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

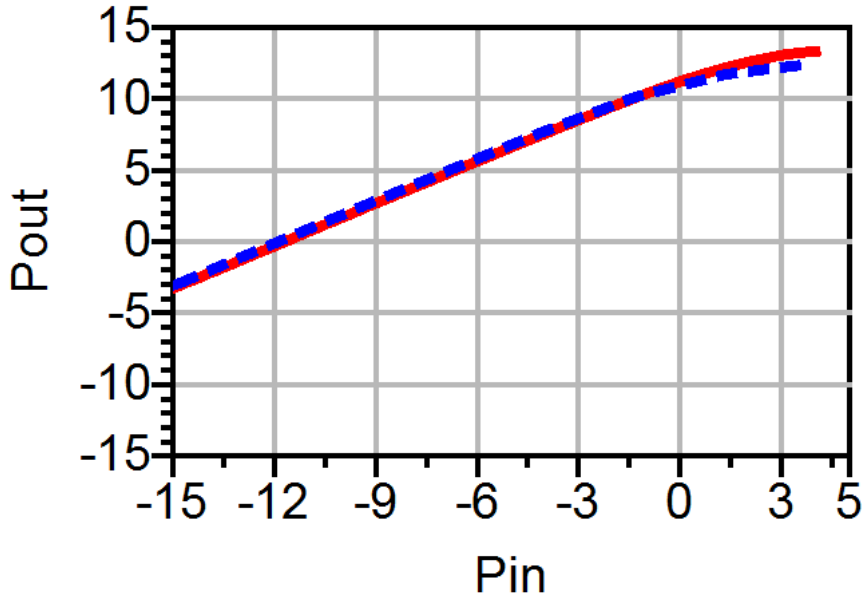


Figure 8.2: Output Power Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

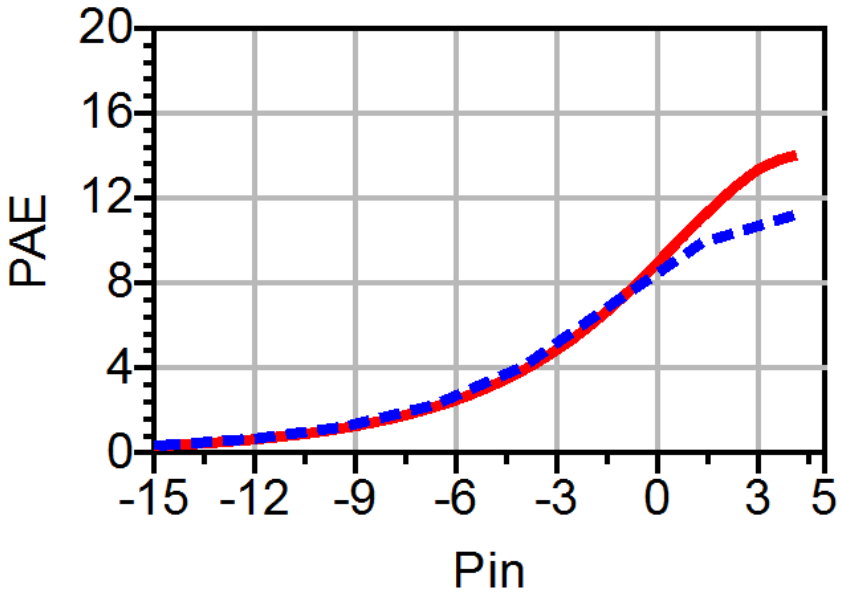


Figure 8.3: Power Added Efficiency Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

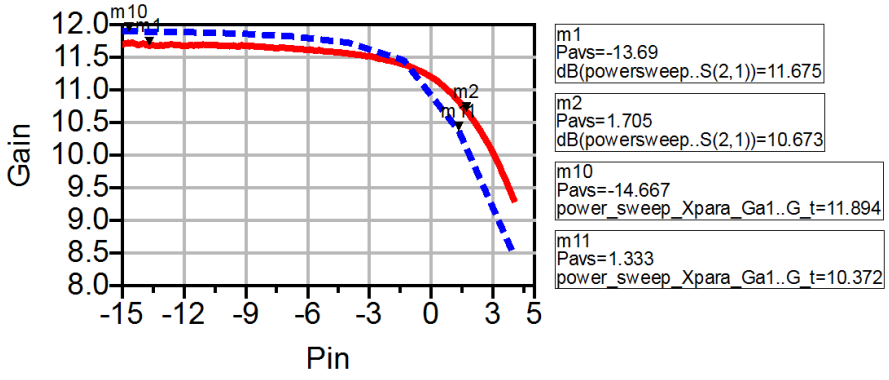


Figure 8.4: 1 dB Compression Point Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

8.1.2 Comparison Results on Gali-S66+ HBT Power Amplifier

This section contains the comparison results between PNA-X X-parameters model and VNA measurements on Gali-S66+ HBT Power Amplifier. Firstly, PA Gain vs. Pin, Pout vs. Pin, and PAE vs. Pin comparisons are shown in Figures 8.5, 8.6, and 8.7, respectively. Then PA 1 dB compression point

comparison is shown in Figure 8.8.

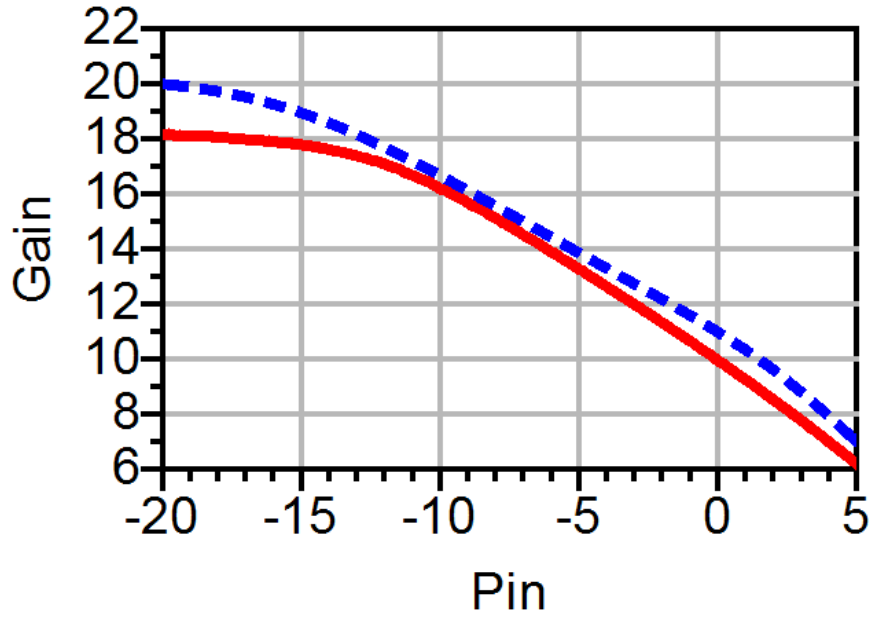


Figure 8.5: Gain Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

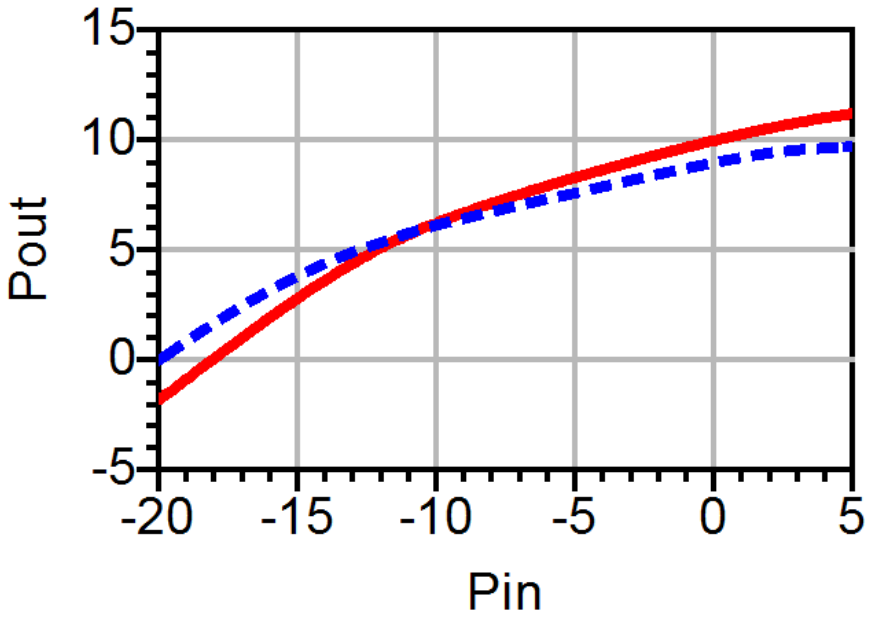


Figure 8.6: Output Power Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

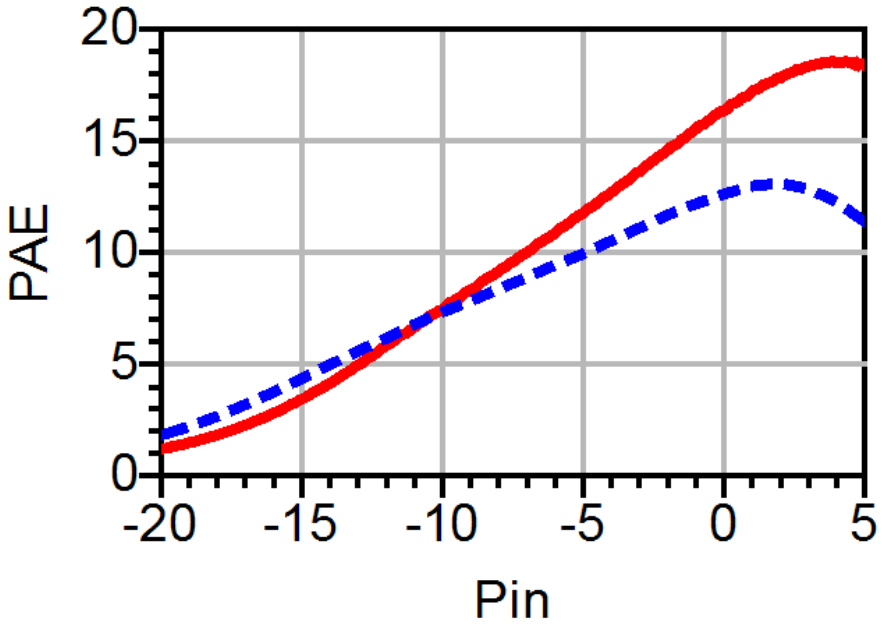


Figure 8.7: Power Added Efficiency Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

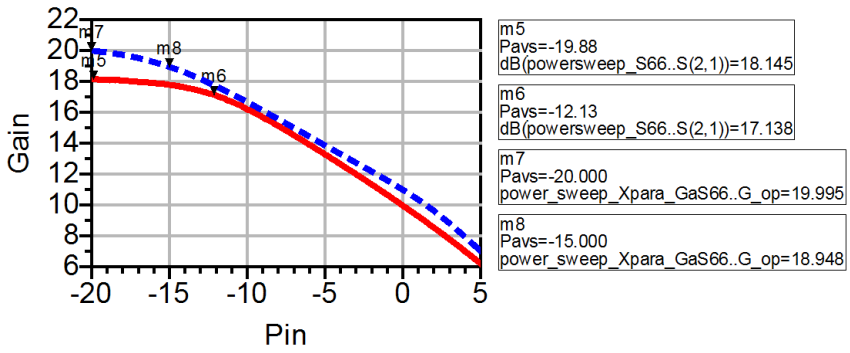


Figure 8.8: 1 dB Compression Point Comparison on VNA Measurement (Red) vs. X-Parameters Model (Blue Dot)

From the above comparisons, both amplifiers have good comparison results between VNA measurement and PNA-X X-parameters model. This indicates X-parameters can serve as a great model for characterizing power amplifiers.

8.2 Comparing PNA-X X-Parameters Model with PSA Measurements

8.2.1 Comparison Results on Gali-1+ HBT Power Amplifier

This section contains the comparison results between PNA-X X-parameters model and PSA measurements on Gali-1+ HBT Power Amplifier. Firstly, power spectrum vs. frequency comparison is shown in Figure 8.9. Then, two-tone third-order IMD IIP3/OIP3 is compared in Table 8.1. Lastly, circuit model simulation of ACPR under NB-CDMA digitally modulated signal is shown in Figure 8.10; measurement result is displayed in Figure 8.11; and the comparison between simulation and measurement is summarized in Table 8.2.

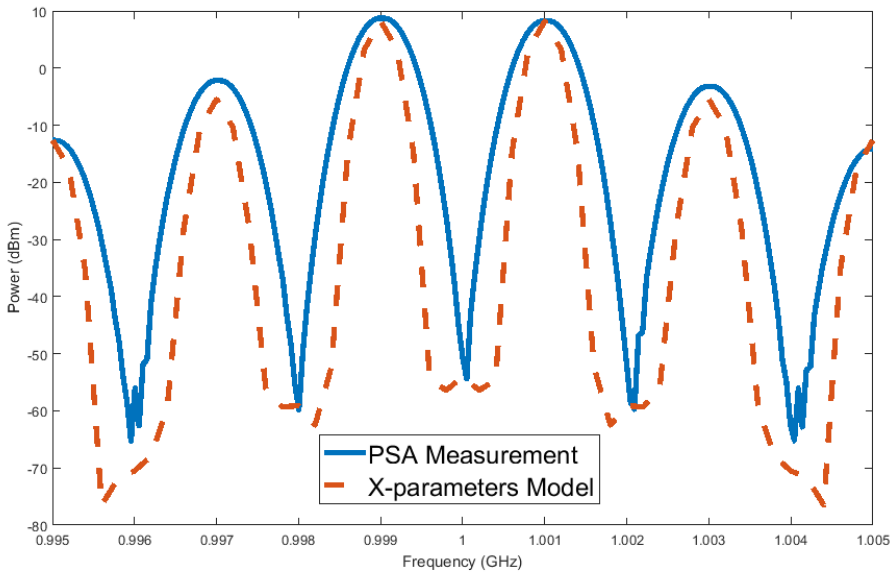


Figure 8.9: Power Spectrum Comparison on PSA Measurement vs. X-Parameters Model

Table 8.1: IIP3 and OIP3 Comparison on PSA Measurement vs. X-Parameters Model

Models	IIP3	OIP3
PSA Measurements	7.5 dBm	18.0 dBm
X-Parameters model	5.0 dBm	15.0 dBm

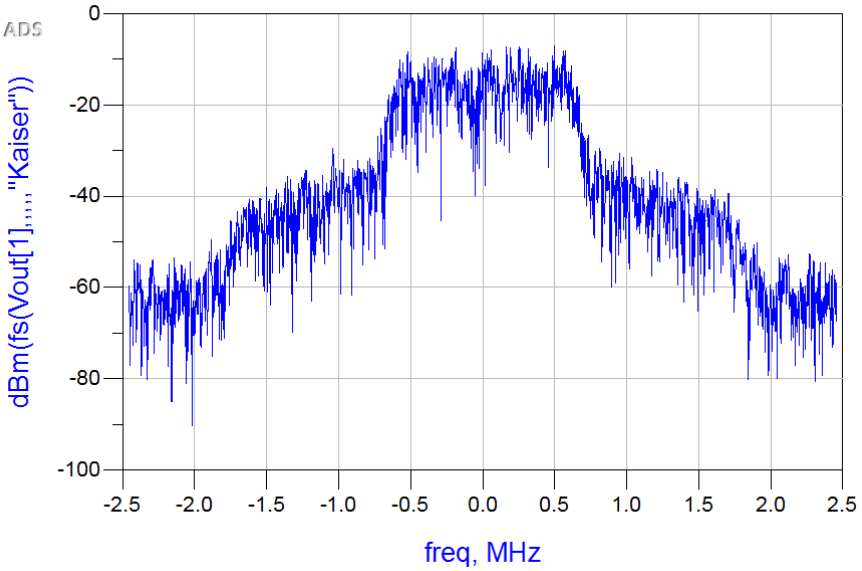


Figure 8.10: X-Parameters Model of ACPR under NB-CDMA Digital Modulated Input Signal at -10 dBm

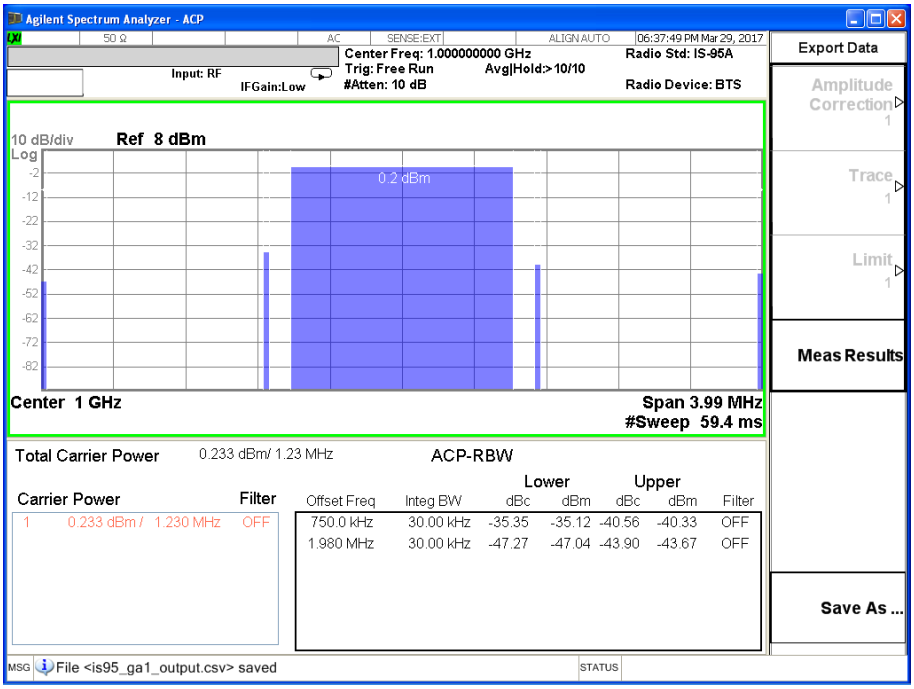


Figure 8.11: Gali-1+ ACPR under NB-CDMA Digital Modulated Input Signal at -10 dBm

Table 8.2: NB-CDMA Comparison on PSA Measurement vs. X-Parameters Model

Models	ACPR1 lower	ACPR1 upper
PSA Measurements	-35.35 dBc	-40.56 dBc
X-Parameters Model	-40.16 dBc	-40.16 dBc

8.2.2 Comparison Results on Gali-S66+ HBT Power Amplifier

This section contains the comparison results between PNA-X X-parameters model and PSA measurements on Gali-S66+ HBT Power Amplifier. Firstly, power spectrum vs. frequency comparison is shown in Figure 8.12. Then, two-tone third-order IMD IIP3/OIP3 is compared in Table 8.3. Lastly, circuit model simulation of ACPR under NB-CDMA digitally modulated signal is shown in Figure 8.13; measurement result is displayed in Figure 8.14; and the comparison between simulation and measurement is summarized in Table 8.4.

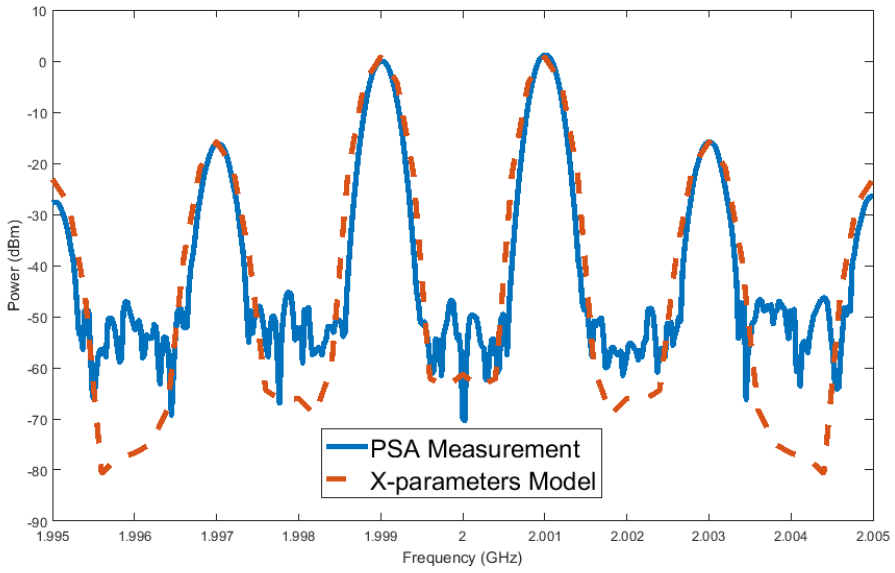


Figure 8.12: Power Spectrum Comparison on PSA Measurement vs. X-Parameters Model

Table 8.3: IIP3 and OIP3 Comparison on PSA Measurement vs. X-Parameters Model

Models	IIP3	OIP3
PSA Measurements	-8.5 dBm	11.5 dBm
X-Parameters model	-10.3 dBm	9.7 dBm

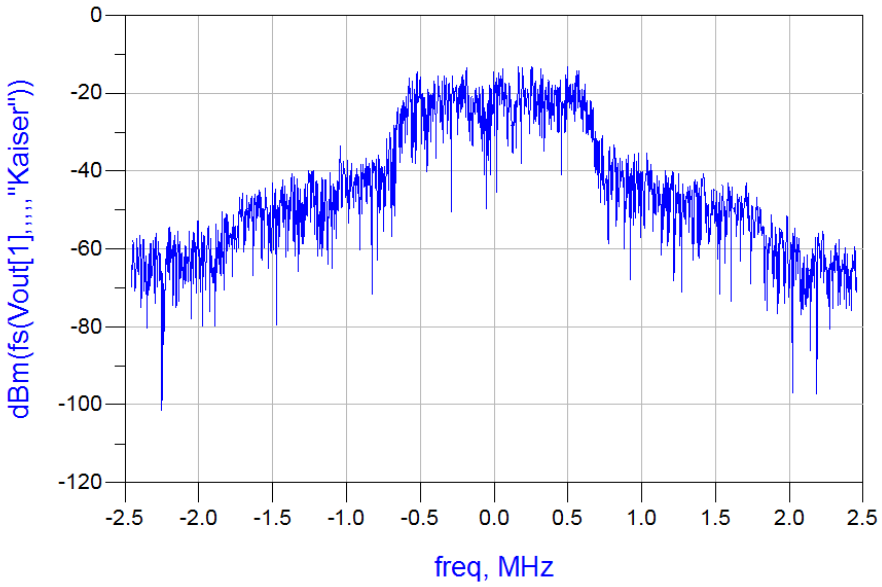


Figure 8.13: X-Parameters Model of ACPR under NB-CDMA Digital Modulated Input Signal at -13 dBm

Figure 8.14: Gali-S66+ ACPR under NB-CDMA Digital Modulated Input Signal at -13 dBm

Table 8.4: NB-CDMA Comparison on PSA Measurement vs. X-Parameters Model

Models	ACPR1 lower	ACPR1 upper
PSA Measurements	-35.35 dBc	-40.56 dBc
X-Parameters Model	-38.50 dBc	-38.50 dBc

From the above comparisons, both amplifiers have good comparison results between PSA measurement and PNA-X X-parameters model. This also indicates X-parameters can serve as a great model for power amplifier.

CHAPTER 9

CONCLUSION

Thus far, in this thesis, the fundamental knowledge of various types of power amplifier has been introduced; the basic measurement of class A power amplifier has been described; and an in-depth class E output impedance matching network has been designed. Chapter 1 states the motivation for this thesis. Chapters 2 and 3 characterize eight major classes of power amplifier. Chapter 4 introduces the design procedures of a standard class E power amplifier output matching network. Chapter 5 describes the measurement theory and implementation of characterizing a power amplifier. Chapters 6 and 7 present the measurement results, performed both on VNA and PSA, of two class A power amplifiers. Chapter 8 introduces X-parameters to model the behavior of those two class A power amplifiers.

One lab in ECE451 has been reorganized or redesigned based on this thesis (listed in the Appendix A). This course is highly recommended to future students who would like to research in RFIC.

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APPENDIX A

ECE 451 LAB 10 – POWER AMPLIFIER MEASUREMENTS USING VECTOR NETWORK ANALYZER

A.1 Introduction

This experiment [1] contains two portions: measurement and simulation of nonlinear characteristics of a power amplifier. You will learn how to measure the key figure-of-merit (FOM) of a power amplifier using the vector network analyzer (VNA) and prove the limitation of S-parameters in characterizing a nonlinear device. We will be using an evaluation board (TB-409-1+) for a monolithic power amplifier (Gali-1+) in this experiment. In the first part, you will measure the S-parameters of the amplifier module to verify the small-signal parameters match with the data-sheet. Additionally, you will use ADS simulation to prove the limitation of S-parameters in nonlinear device measurements. In the second part, you will perform a power-sweep on the VNA to characterize the 1-dB compression point for the amplifier and simulate the nonlinear behavior using the Harmonic Balance simulator in ADS. Lastly, you will compare the simulated 1-dB compression point with the measured data and check if there is an agreement between those two.

[1] This experiment is mainly adopted from this thesis and inspired by the ECE 451 previous lab manual.

A.2 Background

Over the years, the wireless communication market has experienced remarkable development since the first handheld phone introduced by Motorola. Nowadays, the smartphone is one of the most indispensable personal items, with a wide variety of applications that can benefit our daily life. Consequently, the thirst to achieve better wireless transceiving system design, with a low market cost, has gradually become the primary goal of modern RFIC manufacturers.

In all RF transceivers, the power amplifier (PA) plays a key role in driving the antenna on the transmitting end, while low-noise amplifier boosts the receiving end signal. Together these components account for the basic operation of a duplexed system. Among the various requirements in designing a PA, efficiency and linearity are the two most important characteristics. In the modern RF industry, engineers are sparing no effort to increase the PAE in order to increase the battery life; however, linearity requirements, such as ACLR for W-CDMA, E-UTRA for LTE, and ACPR for CDMA2K, must be obtained in order to achieve the basic PA functionality [2].

Typically, we design PAs to operate only within their linear region of operation but that results in an inefficient use of the available power. PA design is different than traditional microwave amplifier design as the goal is not to simply use simultaneous conjugate for max power; instead the designer has to satisfy figures-of-merit like power added efficiency (PAE) and TOI points that dictate the level of non-linearity in the amplifier. Since PAs operate under large signal they are often driven into the non-linear regime and thus characterization of the nonlinear behavior is of utmost importance to the RF engineer.

A.3 Pre-Lab

1. What is the physical significance of 1 dB compression point? Why is it a useful metric to characterize non-linear behavior of RF circuits?

[2] Z. Li, "Characterization of various types of power amplifiers," M.S. thesis, University of Illinois at Urbana-Champaign, Champaign, IL, May 2017.

2. What is the physical significance of PAE? Write down the equations to compute it?

3. What is Harmonic Balance? How is it different than traditional SPICE simulation? List some advantages for using Harmonic Balance for studying RF circuits/systems and mention some common potential problems that could arise when using this simulation engine.

4. Briefly talk about PA nonlinear properties.

A.4 Equipment

- Agilent E8358A VNA.
- Agilent 85052D 3.5mm SOLT calibration kit.
- 3.5mm cables.
- N-type to 3.5mm adaptors.

A.5 Small-Signal S-Parameters Measurement Procedure

1. Log into the network analyzer using your NetId and Active Directory Password. The network analyzer software will open as soon as the login is complete.

2. Create the setup as shown in Figure A.1 below. Make sure to press "Output On" before measuring the amplifier's S-parameters in the VNA.

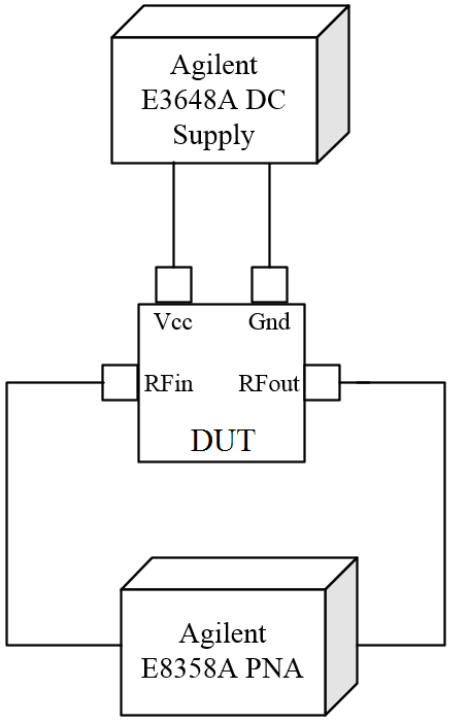

Figure A.1: Vector Network Analyzer Experiment Setup Diagram

3. Click on the yellow Start Button and set it to 300 MHz. Click on green Stop Button and set it to 8 GHz. Next select Sweep < Number of Points and select 1601 points.

4. On the left side of the screen, right click the box that says "S_{11}," go into Format and select "Log Mag." This displays Log-Magnitude for each measured frequency point. Each point is connected by a straight line.

5. To save data select File < Save As. Find a directory on your personal drive, give the file the appropriate name and select "Trace (*.s2p)" as your Save as Type. Sample name can be "PA_SmallSig.s2p".

6. Open ADS, create a new workspace, and import all of these datasets in, giving them the same names as you saved them in above (use the same procedure from previous experiments). See the Notes on Using ADS at the end of the procedure for some advice on dealing with multiple datasets.

7. In the Data Display plot S-parameters of the amplifier and put markers on S_{21} as well as S_{11} for each of the points listed in the data-sheet to compare measured data with manufacturer's data.

A.6 ADS Simulation Setup Using Harmonic Balance Simulator

In this section, we will implement a simple ADS environment for running power sweep simulations.

1. Create new workspace in ADS and call it ECE451_lab10.
2. Create new schematic and call it Power_sweep.
3. We start by importing the .snp measurement file you saved from the VNA. In ADS type S2P in the component search window above the upper left palette.
4. Now in the upper left pallet select Simulation-HB ⇒ HB.
5. Then select Simulation-HB ⇒ PrmSwp.
6. In the upper left pallet select Sources-Freq Domain ⇒ P_nTone.
7. Your schematic should look like the following as shown in Figure A.2.

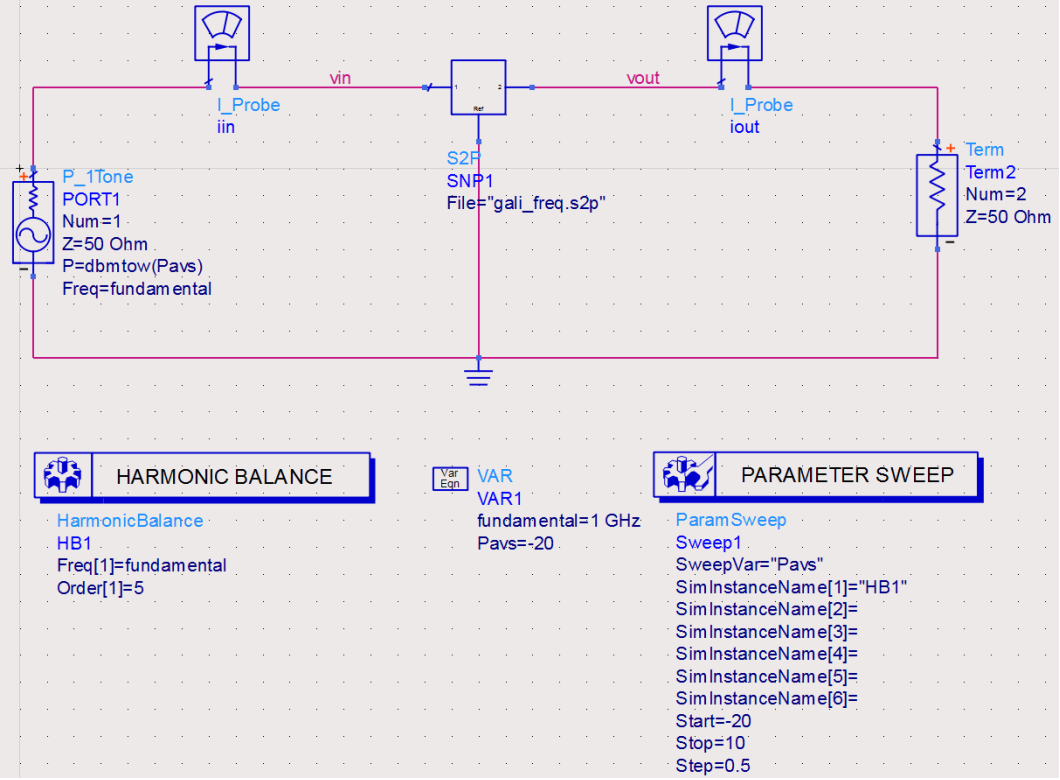

Figure A.2: Harmonic Balance Simulation Schematic

8. Add equations as shown in Figure A.3.

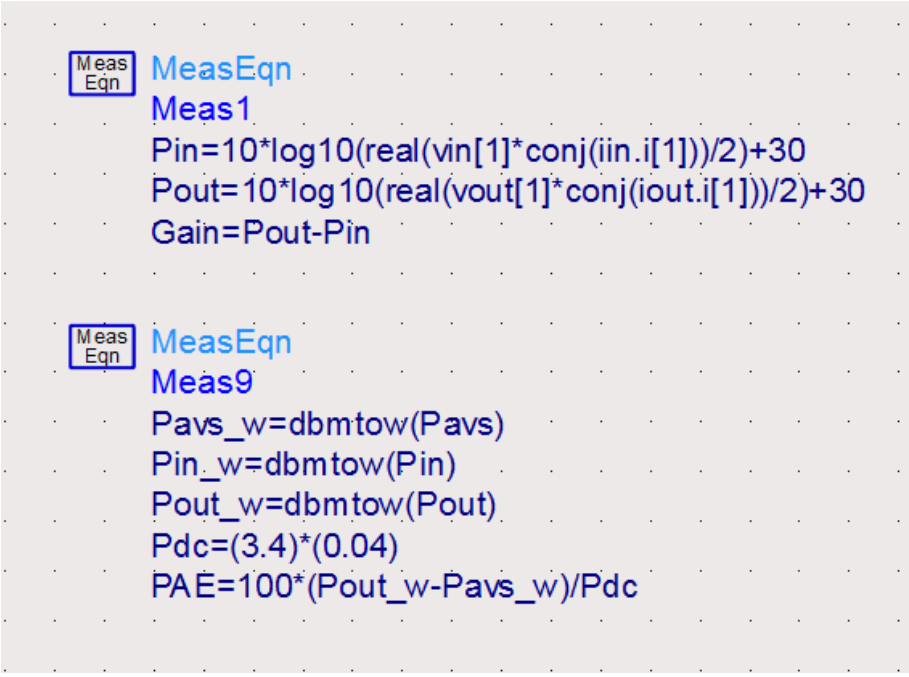

Figure A.3: Necessary Equations for HB Simulation

9. Before Simulation, go to Simulate ⇒ Simulate Settings from top menu and change the Dataset name to Power_sweep_Spara as shown in Figure A.4.

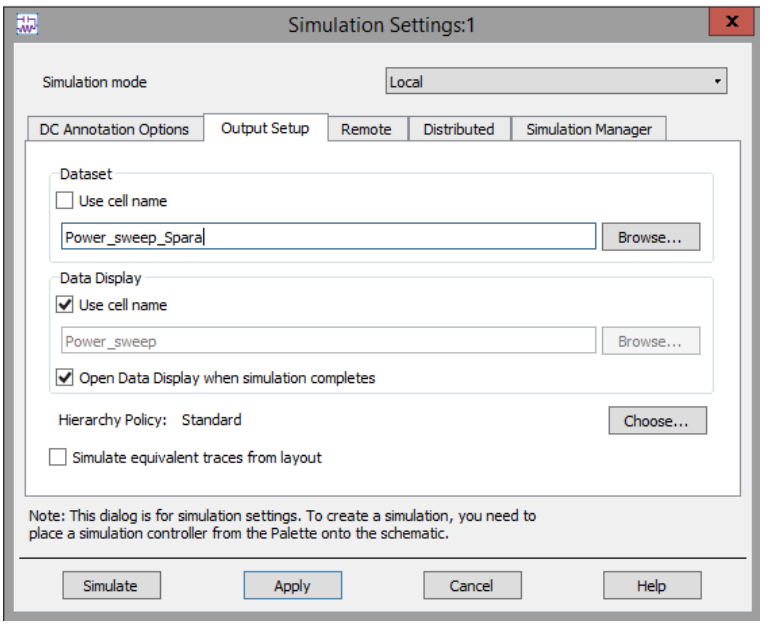

Figure A.4: Simulation Settings

10. Plot the Gain in ADS data display (DDS) window and change the Y-scale from auto to 10∼13 with a 0.5 interval.

11. Your Gain plot should be a straight line if everything was performed correctly. However, is this reasonable? Let's answer the question after performing the next experiment.

A.7 1-dB Compression Point Measurement Procedure

1. Prepare the PNA for a Power Sweep:

   (a) Log into the Agilent E8357A PNA. Start up the Network Analyzer software if it doesn't start automatically.

   (b) Set the network analyzer to perform a power sweep from -20 to +10 dBm at 1 GHz by selecting "Sweep>Sweep Type" and choosing "Power Sweep" as the Sweep Type.

(c) Perform a 2-port SOLT calibration through the Calibration Wizard. Choose the 85052D 3.5mm Calibration Kit.

2. Set up the Amplifier:

   (a) The amplifier we are using in this class needs to be biased by a 12 V dc source. **Do not** push the "output on/off" button at this time. You will need to connect the +25V and ground/COM of the power supply to the +12 and GND connections of the amplifier.

   (b) Connect port 1 of the PNA to the RF_{in} of the amplifier and port 2 of the PNA to RF_{out} of the amplifier.

   (c) Now turn on the output of the power supply by pushing the "Output on/off" button and look at the PNA output. Right click using the mouse on the PNA screen and select AUTO SCALE. Plot the S_{21} and Your PNA image should look similar to Figure A.5.

Figure A.5: P_{out} vs. P_{in}

3. Measure your 1 dB gain compression point:

(a) View the log magnitude of S21 on the PNA. Set the markers to measure the 1 dB gain compression input power. You can add multiple markers by selecting "Marker-Select Marker" choosing the marker you want to select. Use one marker to indicate the max Pout and the other marker to find the input power that gives a -1 dB output power. Record this 1dB gain compression Pout and Pin.

(b) Save your SnP file as "PA_Power_Sweep.s2p".

A.8 Comparison Between S-Parameters and Power Sweep Data Using ADS

1. Before importing "PA_Power_Sweep.s2p" data to the ADS, we need to make a small change to the snp file. Change the dBm unit to Hz (cause ADS can only read this unit), and delete Power Sweep after the semicolon as shown in Figure A.6.

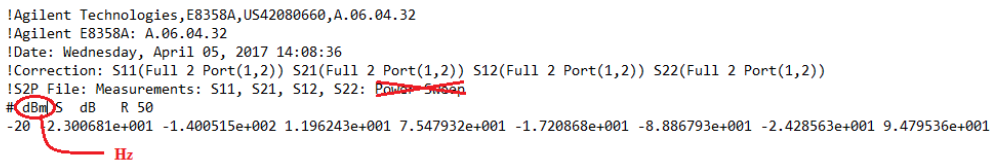

Figure A.6: A Method to Import Power Sweep Snp File to ADS

2. Now you can import your snp file to the data display window from last section (in my case: Power_sweep.dds).

3. Plot the new S_{21} to Gain plot.

4. Your plot should look similar to Figure A.7. Now, clearly, amplifier gain of small signal S-parameters measurement is linear throughout the sweeping power range; however, amplifier gain starts to compress at -5 dBm in the large signal power sweep measurement. This phenomenon is due to the nonlinear nature of the power amplifier. Therefore, to characterize the behavior of the power amplifier, especially at relatively high input/output power, an S-parameters model is not enough. In next lab, we will introduce another parameter called *X-parameters*, which is a large signal parameter meant to characterize nonlinearity.

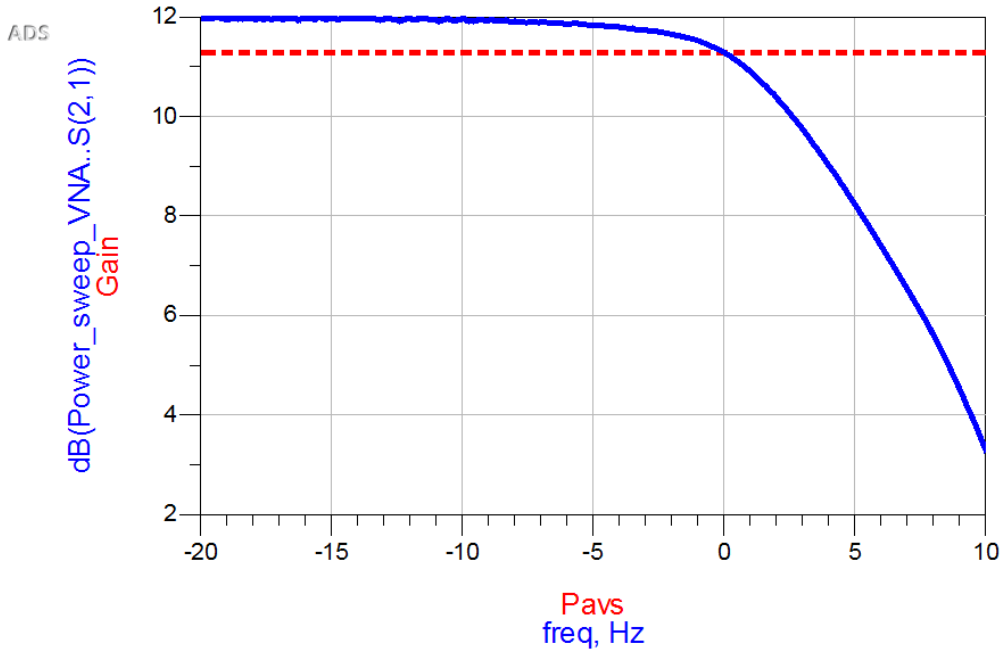

Figure A.7: A Comparison Between Small and Large Signal Measurement

5. In the same data display window, plot the PAE and the output power of the VNA measurement by using the equations in Figure A.8. Make sure to use the correct dataset file name in equations (in here powersweep.. should be replaced).

```
Eqn Pout = powersweep..freq + dB(powersweep..S(2,1))

Eqn PAE = 100*(dbmtow(Pout)-dbmtow(powersweep..freq))/(3.4*0.04)
```

Figure A.8: Equations to Write in Data Display Window

A.9 Harmonic Balance Simulation Using Circuit Model in ADS

In this section, you will use the circuit model provided by your TA to perform an HB simulation and compare it with your measured power sweep data from VNA.

1. Re-open your S-parameters simulation schematic and change the S2P component to the circuit symbol (with a 12 V dc source) provided by your TA as shown in Figure A.9.

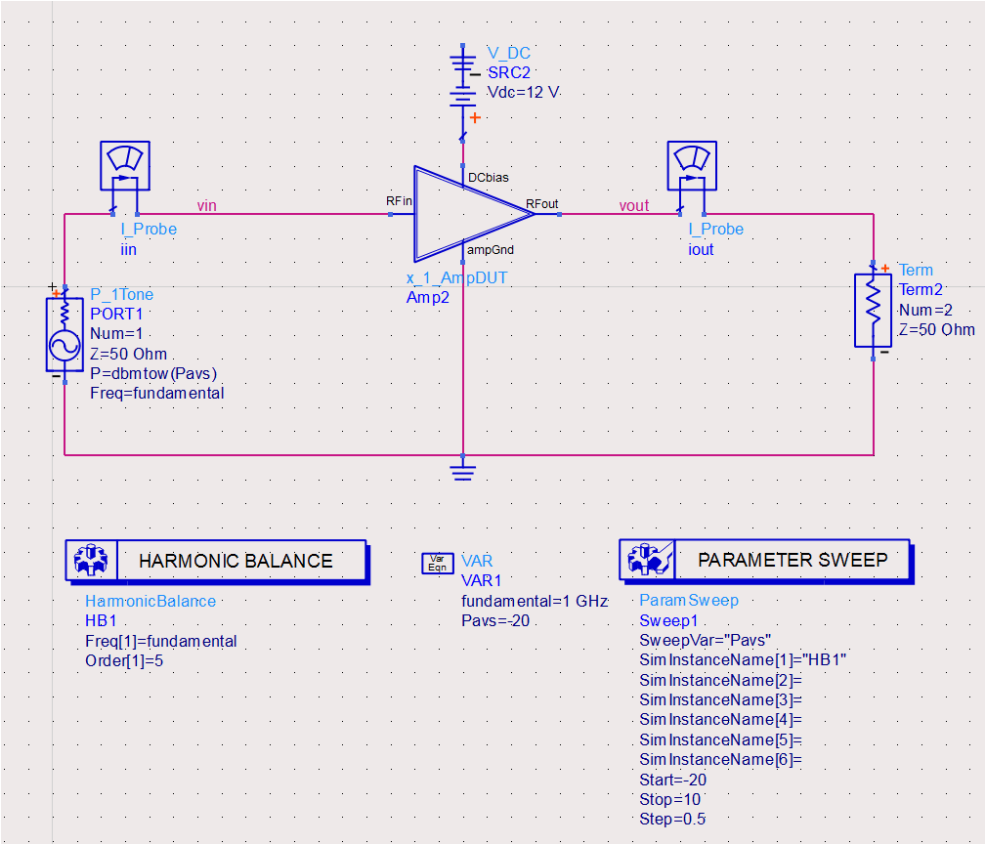

Figure A.9: Harmonic Balance Simulation Schematic with Circuit Model

2. Before Simulation, go to Simulate ⇒ Simulate Settings from top menu and change the Dataset name to Power_sweep_Ckt as shown in Figure A.10.

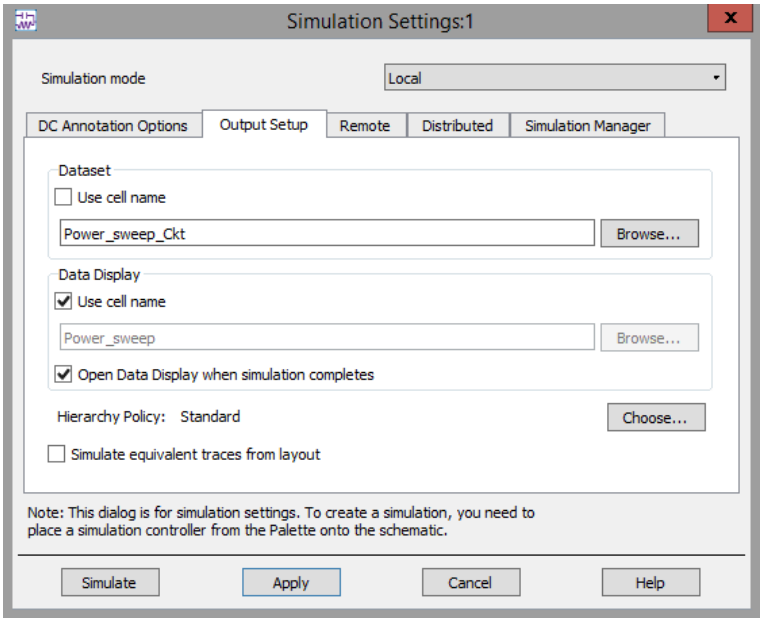

Figure A.10: Simulation Settings

3. After simulation, plot Gain from VNA power sweep measurement and circuit model HB simulation on the same graph and compare. Note that you need to choose the correct dataset from the drop down menu. Your plot should be similar to Figure A.11.

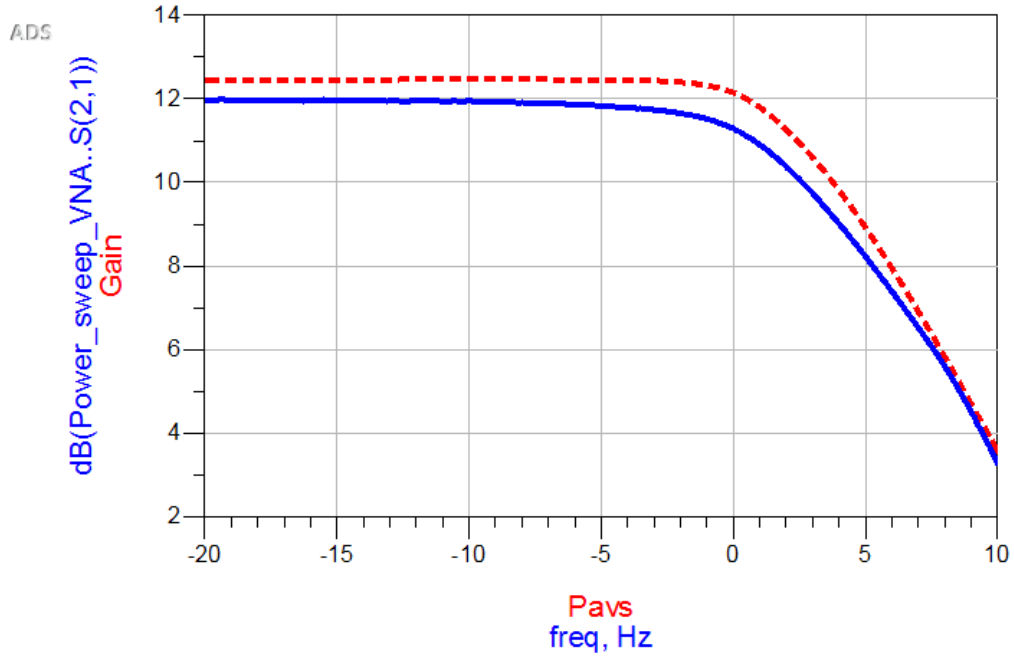

Figure A.11: Gain Comparison Between Circuit Model Simulation (Red Dot) and Power Sweep Measurement (Blue line)

4. Do the same for plotting Pout and PAE.

A.10 Conclusion

1. Compare your S-parameters (S_{11}, S_{21} and S_{22}) small signal measurements with manufacturer's data-sheet. What may cause discrepancies? Compare all frequencies listed on the datasheet.

2. Why are we not able to simulate the P1dB point from the S-parameter data measured on the VNA using Harmonic Balance simulation?

3. Can S-parameters help characterize non-linear behavior in amplifiers? If not, what potential shortcomings do you see in the S-parameter formalism?

4. Hand in all plots in your lab report.

APPENDIX B

BLOCK DIAGRAM OF A SUPERHETERODYNE TRANSCEIVER

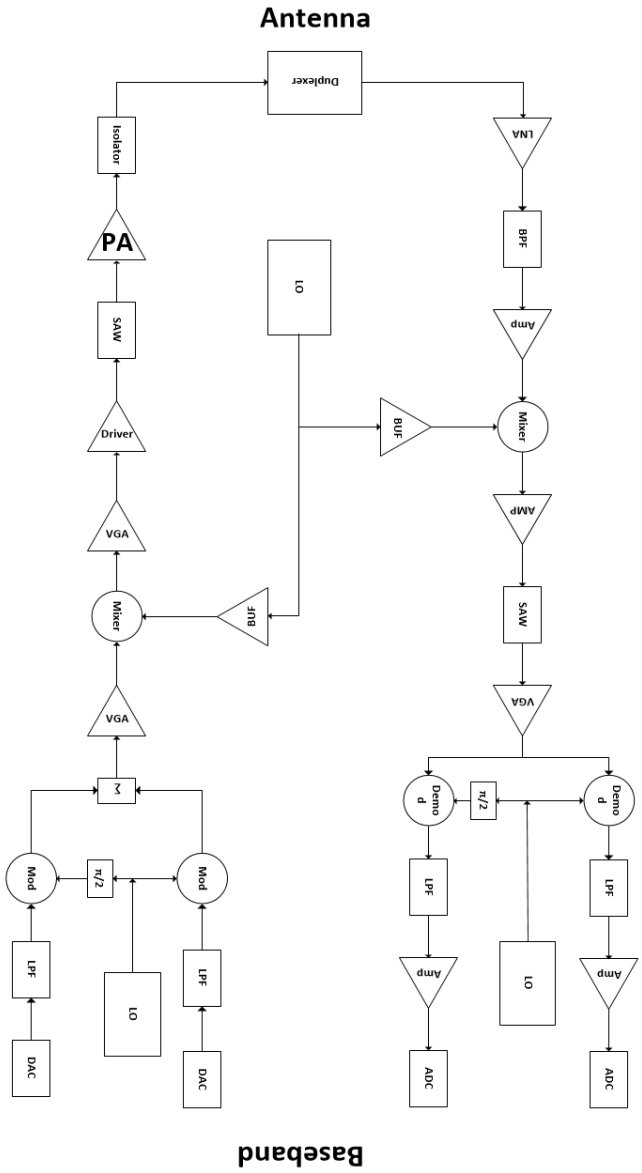

Figure B.1: Block Diagram of a Superheterodyne Full-Duplexer Transceiver