CHARACTERIZATION OF CHANNEL SIMULATION METHOD WITH JITTER AND EQUALIZATION EFFECT ON EYE DIAGRAM

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BY

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THESIS

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ABSTRACT

The detail of how transient brutal-force channel simulation and the edge-based bit-by-bit simulation perform for the signal propagating through the channel is discussed in this thesis. The efficient and accurate eye diagram generated from bit-by-bit mode simulation is presented. And the eye diagram representation involving the jitter and equalization on transmitter and receiver end is considered.

To my parents, for their love and support.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Over the past decades signal analysis field has been addressed significantly as the urgent demand for multi giga-per-second data rate transfer. A large file copied from a PC internal drive to an external USB drive, a dense and CPU-consuming simulation running in the computer and a multi-task processing in your phone should happen at a glance. Back to the 1980s, when the first IBM PC named XT to come with ST506 internal hard drive disk, introduced by Shugart Technology, now as one of the lead hard drive companies Seagate Technology, its data transition rate was only 5 Mbps with the maximum 10 megabytes storage. 40 years later, in 2020, the Seagate hard drive can easily achieve 6 Gbps transfer rates under SATA III cable, over 1200 times faster in a 40-year revolution. Not only researchers but also people living in daily life are benefited by data and information transmitted at a high speed rate in today's complex environment.

Figure 1.1: IBM Personal Computer XI

As high speed data rate keeps increasing, the high speed link modeling technique and simulation accuracy become more stringent. At 6 Gbps, the unit interval (UI) is only 166.7 ps for a non-return-to-zero (NRZ) signal. This timing budget is shared by the transmitter (TX), receiver (RX) and channel (CH), where the three major components of a high speed link are. According to [1], the transmitter and channel each will degrade about 30 percent of the UI, so the left 40 percent of UI will be received at the receiver end. Then, if considering all the voltage offsets and timing jitters, it is a challenge to meet a UI of 166.7 ps at 6 Gbps. When the higher data rate approaches, more difficult a required UI would be to reach. Therefore, accurate modeling techniques and simulation are critical for designing high speed links properly. Intersymbol interference (ISI) is another issue raised up while the faster data rate, due to the low pass nature of the channel. To counteract the effect of intersymbol interference, several equalization techniques have been well-developed such as feed-forward equalization (FFE), continuous-time linear equalization (CTLE) and decision-feedback equalization (DFE). By placing different equalizers at either transmitter side or receiver end, an open and larger eye will be expected to see from the eye diagram.

The high speed serial link is composed of three parts: the transmitter, the interconnect/channel and the receiver. The information of the interconnect is normally described by scattering parameters since it is a linear time-invariant (LTI) system. The transmitter and the receiver are usually described in the transistor-level, and sometimes the behavioral model can also be used in a high-level design. Once the digital inputs feed into the transmitted driver, the corresponding outputs are expected from the receiver output end. And the technique to determine whether the signal is qualified to pass is through the eye diagram at a certain bit error rate (BER). The wording of such input-output phenomenon is apparent, however the signal processing inside the whole link, especially under the high speed circumstance such as 10 Gbps or above, is not trivial. The commercialized high speed link simulators are widely available in simulation tools such as ADS and Cadence. Then, this thesis is to investigate the simulation theory behind the link simulator and analyze the jitter and equalization.

1.2 Scope of Thesis

This thesis is organized as follows. Chapter 2 explains the channel simulation methods for the process of the eye diagram generation. Chapter 3 introduces the effects of various jitter on the eye diagram. Then, chapter 4 discusses how equalization works and its effects on the eye diagram.The conclusions and future work are summarized in Chapter 5.

CHAPTER 2

CHANNEL SIMULATION METHOD OVERVIEW

The transient analysis or time-domain analysis has been applied significantly in the circuit system world. Simplistically, it means by giving a time-domain input and initial condition, trying to compute an output waveform in the time domain (a function of time). All different channel simulation methods are based on transient analysis. In current time, there are three types of channel simulation methods: transient brutal-force simulation, by-by-bit mode simulation and statistical mode simulation, being used widely during the high speed link signal analysis to generate the eye diagram. The fundamental and original one is transient brutal-force simulation and two other advanced simulation modes, bit-by-bit and statistical, were invented later in the 2000s.

2.1 Transient Brutal-Force Simulation

In general, the way to compute output response in computer programs requires numerical integration methods such as Backward Euler method, Forward Euler method and Trapezoidal method to generate outputs at discrete time steps [2]. However, under the discussion of this thesis, the help of S-parameters simplifies the transient analysis process.

2.1.1 S-Parameter

The S-parameter set represents the input and output ports relationship of the network system, described by the linear combinations of the voltage and current at particular ports. Fig. 2.1 shows the S-parameter for a two-port network system.

By definition, S_{ij} the subscript "j" stands for the input port that is excited,

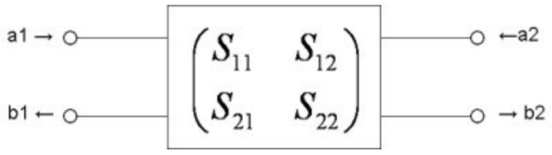


Figure 2.1: Two-port s-Parameter network.

and the subscript "i" stands for the output port or receiver port. Thus S_{21} refers to the power wave ratio of the amplitude of the reflected wave from port two to the amplitude of the incident wave on port one. Then, S_{21} also represents the transmission coefficient or power gain ratio of the network system. The definition of all S-parameter terms are shown in Fig. 2.2.

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a2=0} = \frac{reflected\ power\ wave\ at\ port1}{incident\ power\ wave\ at\ port1}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a2=0} = \frac{transmitted\ power\ wave\ at\ port2}{incident\ power\ wave\ at\ port1}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a1=0} = \frac{reflected\ power\ wave\ at\ port2}{incident\ power\ wave\ at\ port2}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a1=0} = \frac{transmitted\ power\ wave\ at\ port1}{incident\ power\ wave\ at\ port2}$$

Figure 2.2: Two-port s-Parameter definition.

Therefore in high speed link analysis, a linear transmission line, two-port network system, can be characterized by the S-parameter model, which then can be used during the circuit design and frequency domain simulation.

2.1.2 Channel Impulse Response

In a linear and time-invariant (LTI) system, the information of its impulse response can completely characterize this system. Knowing the corresponding impulse response and any input, the output can be calculated directly in terms of impulse response and input. Applying this idea to the channel,

which is a LTI system, the channel output waveform can be easily found if the channel impulse response is given.

Then, the output waveform function in frequency and time domain can be expressed as Eqn. 2.1 and Eqn. 2.2.

$$Y(\omega) = H(\omega)X(\omega) \tag{2.1}$$

$$y(t) = h(t) * x(t) = \int_{-\infty}^{+\infty} h(t-\tau)x(\tau) \tag{2.2}$$

The output of the channel is simply the convolution of the input waveform to the channel with the channel impulse response. Equivalently, in the frequency domain, any LTI system including the channel can be characterized by the system's transfer function, which is a Fourier transform of the impulse response. As a result, the output waveform in frequency domain is the product of the transfer function and the input in frequency domain. The completed relationship between the time and frequency domain is shown in Fig 2.3.

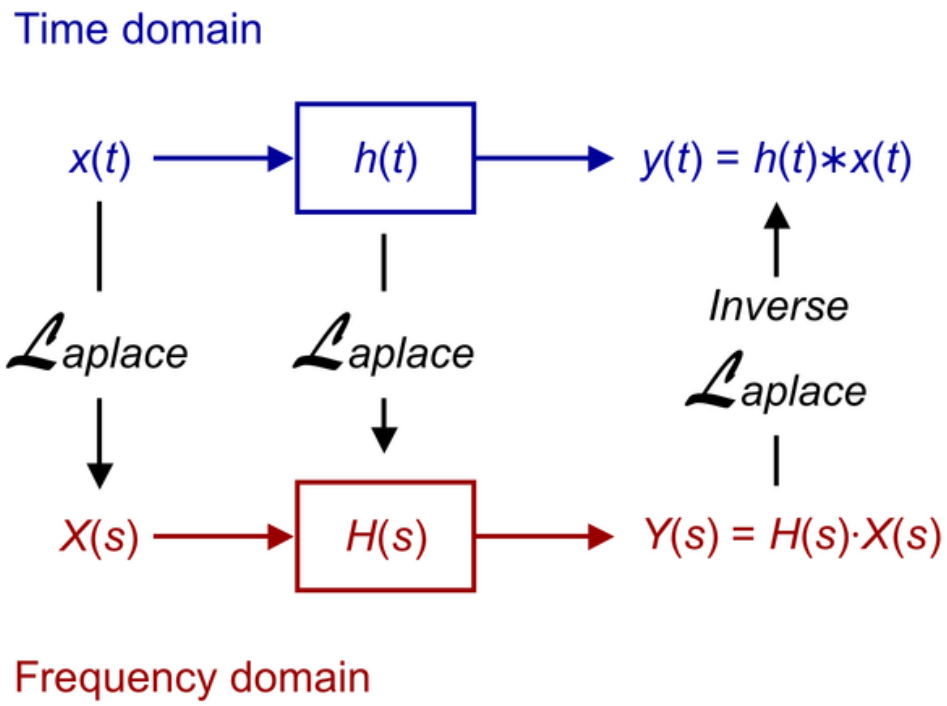


Figure 2.3: Relationship between the time domain and the frequency domain.

In this thesis, the USB 3.1 link as shown in Fig 2.4 from Advanced Design System (ADS) workspace is provided to perform the channel simulation, so the S-parameter information is obtained through the measurement in ADS. As mentioned before, S_{21} is a measure of the signal coming out of port 2 to the stimulus entering from port 1, which has the same property of the transfer function, thereby being used to derive the impulse response of the channel by the inverse Fourier transform. The S_{21} channel loss is shown in Fig 2.5a and its corresponding impulse response is calculated and plotted in Fig 2.5b.

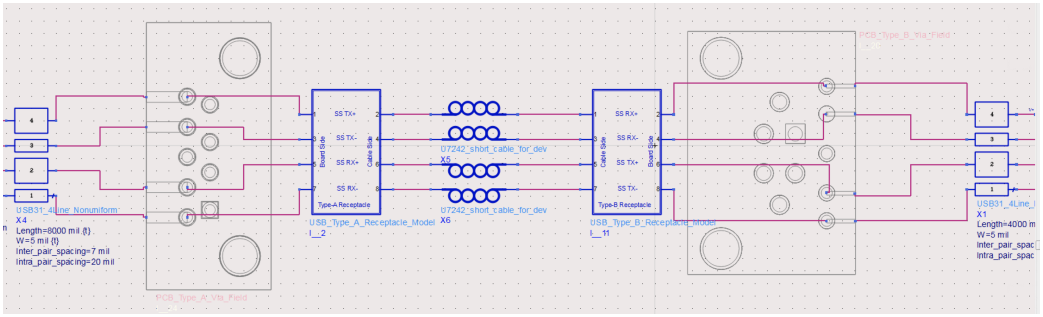
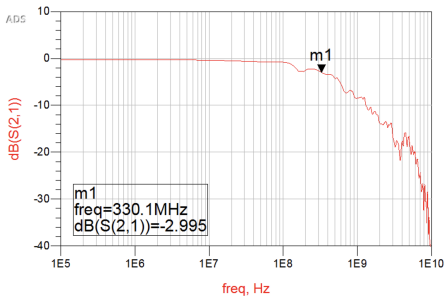
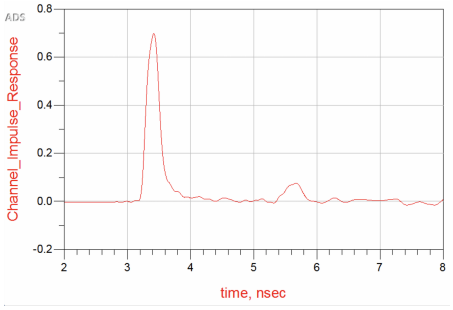


Figure 2.4: A typical USB 3.1 link with vias and type A/B receptacles.



(a) Channel loss (S21) of USB 3.1 link.



(b) Impulse response of USB 3.1 link.

Figure 2.5: Channel Characteristic in frequency and time domain.

The input data is generated by a pseudorandom bit sequence (PRBS) generator and the impulse response is obtained from S-parameter, so the transient channel output is calculated through the convolution between the input data and impulse response. Fig 2.6 displays the generation process.

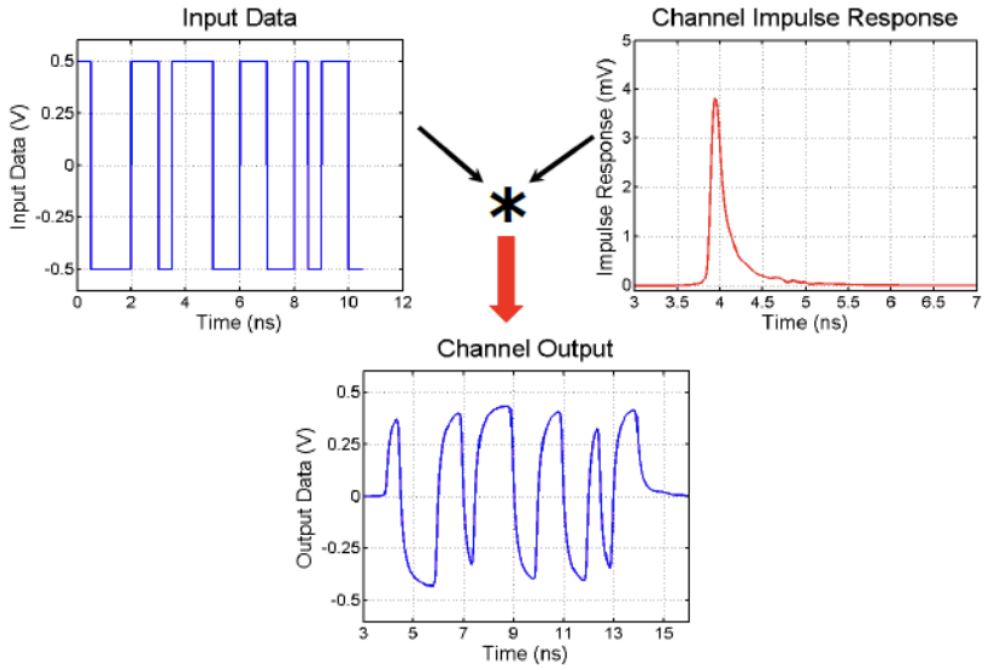


Figure 2.6: Channel transient response.

2.1.3 Eye Diagram

Once the output waveform is established, an eye diagram should also be presented. Eye diagram is a straightforward tool used in the high speed link to evaluate the high speed system performance [3] [4]. It is constructed by slicing the transient signal waveform from the receiver into the size of two unit intervals (UI) and then overlapping every section on top of each other (Fig 2.7). Therefore, the horizontal axis has the range of two symbols in time and the vertical axis describes the voltage magnitude of the receiver signal. The Fig. 2.8 shows an eye diagram example of 5 Gbps 200-bit data pattern generated from the traditional transient simulation. The eye opening in the center part of the eye diagram represents the "clearness" of the signal. The larger the eye opening, more margin there would be for timing and voltage

requirements and the receiver is easier to resolve the signals into digital 1/0.

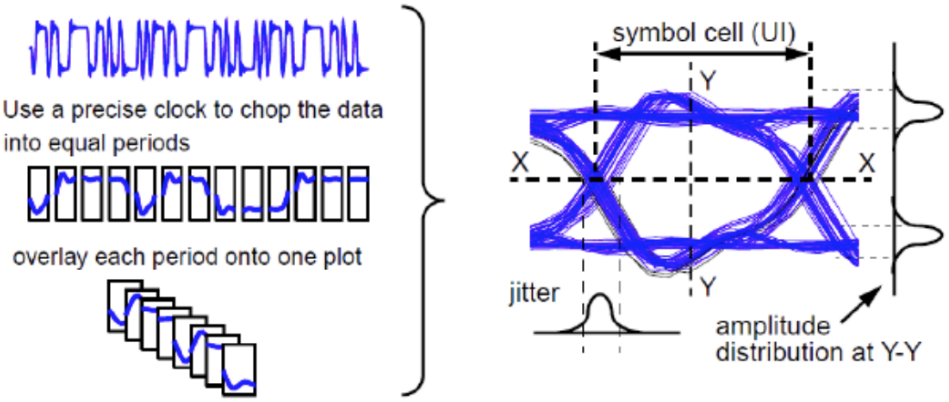


Figure 2.7: Eye diagram.

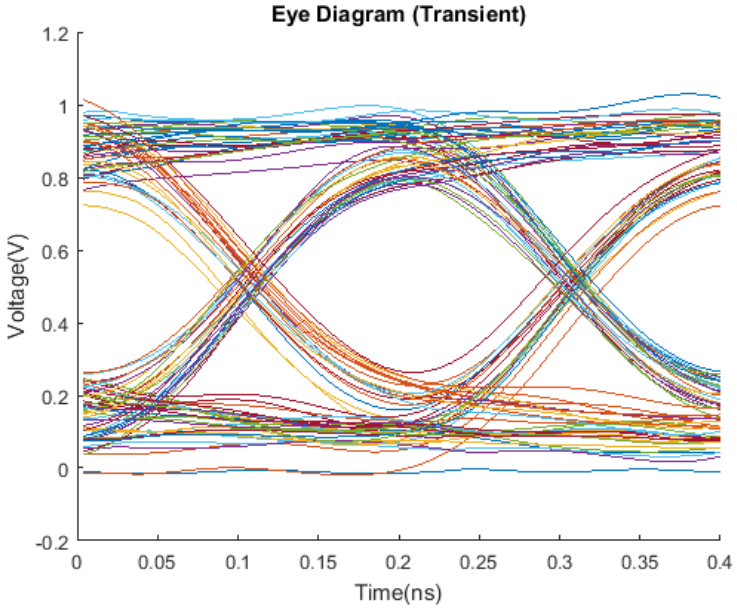


Figure 2.8: Transient eye diagram for 5 Gbps 200-bit data sequence.

2.1.4 Distortions

Conceptually, distortions lead to a closed eye and indistinguishable signals for the receiver. Such distortions are majorly from the nonlinearity property of the channel. Two forms of distortion will happen in non-ideal interconnect: amplitude distortion and phase distortion. Amplitude distortion is due to the low-pass feature of the transmission line. High frequency components are distorted unevenly compared with the low frequency parts. Phase distortion is due to the signal dispersion that the phase velocity is dependent on frequency so phase varies while traveling in the frequency domain. The typical result is that the interconnect will cause the data to have a closed eye due to the low-pass nature of the interconnect channel. Then the purpose of the equalizer is to counter this low-pass effect so that the frequency response of the channel would be flat. More details about the equalizer will be introduced in Chapter 3. And another type of timing distortion called jitter will also be discussed in Chapter 4.

2.2 Bit-by-Bit Mode Simulation

In the previous section, the channel output and the eye diagram are obtained through the traditional transient simulation, as the result of convolving the impulse response and the whole input bit sequences. However, this method might not be the best choice, when an enormous number of input bits are involved, because of time-consuming runtime. Bit-by-bit mode is thus developed to speed up the process.

2.2.1 Edge Response

If the transmitted signal settles within much less one bit period and if the channel is nearly linear and time-invariant, then the voltage at the channel output can be accurately estimated by the superposition of the edge responses. Let's define the edge response more precisely by considering an example of a rising edge response from a 0 to 1 transition input, noted in Fig. 2.9. When a digital input transits from zero to one, the output after the channel will naturally rise from V_{low} to V_{high} and this rising edge output

is defined as $V_r(t)$. V_{low} and V_{high} are the steady-state low and high values. Then, the channel delay is defined as delay D, as shown in Fig. 2.9, which is the time difference between the beginning voltage point of the input and output right before the rising starts during the transition.

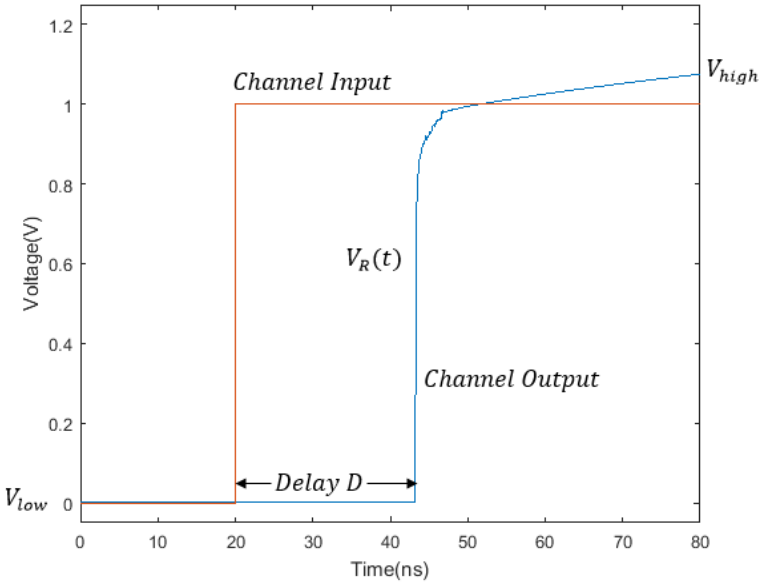


Figure 2.9: Rising edge response with features noted.

The Fig. 2.10 presents the rising edge and falling edge after removing the channel delay and these edges will be used to superpose the output waveform based on two consecutive bits from input bit sequence.

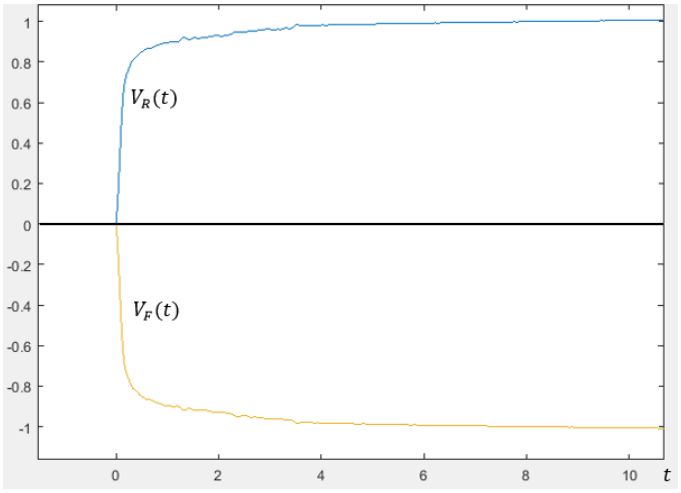


Figure 2.10: Rising and falling edge response.

When the k^{th} bit is 0 and the $(k+1)^{th}$ bit is 1, the rising response must happen on the output waveform between the corresponding time interval of k^{th} and $(k+1)^{th}$ bit.

$$y(t) = \sum_{k=1}^{N} V_r(t - kT) \tag{2.3}$$

Where $y(t)$ is the output waveform, the coefficient k represents the k^{th} bit position, N represents the total number of bits, and T is the time interval of each bit. Basically, one rising edge needs to be added right after the kT time position of the output waveform.

Similarly, when the k^{th} bit is 1 and the $(k+1)^{th}$ bit is 0, the falling response must happen starting from the time corresponding to the k^{th} bit.

$$y(t) = \sum_{k=1}^{N} V_f(t - kT) \tag{2.4}$$

Since the $V_f(t)$ is defined in the negative domain, adding such pattern will bring the previous V_{high} tail from the rising response to a zero-level tail in output waveform.

At the cases of continuous 0 bits and 1 bits, the output waveform will remain its pattern without adding either rising response or falling response.

2.2.2 Example

An example of edge-by-edge superposition is shown below. The input bit pattern is 0100 and each bit takes $T = 1$ ns. Our k here will be 1 to 5 and the transient time t is from 0 to 5 ns. The first bit has to be considered individually first. If the first bit is 1, then I need to pre-set a constant V_{high} at the first time interval for the output waveform, which means

$$y(t) = \begin{cases} V_{high}, & 0 < t \leq T \\ V_{low}, & T < t < nT \end{cases}$$

Similarly, when the first bit is 0,

$$y(t) = V_{low},\ 0 < t < nT$$

Here, in the example, the first bit is 0 so V_{low} is pre-set in the first 1 ns at output waveform, $y(t) = V_{low}, 0 < t \leq 1$ ns.

Following the algorithm description above, the first bit ($k = 1$) is 0 and the second bit 1, then $y(t) = V_r(t-1)$, shown as blue plot in the Fig. 2.11. The rising edge response is filled to the output waveform staring from 1ns till 4ns. The second bit ($k = 2$) is 1 and the third bit is 0, then $y(t) = V_r(t-1) + V_f(t-2)$, shown in Fig. 2.11. The falling edge response is added in from 2ns to 4ns. In the end, the third and four bits are 0, the output waveform from 3ns to 4ns is unaltered being V_{low}. When all 4 bits are considered by adding all rising and falling edges in Fig. 2.11, the final summation plot is shown as Fig. 2.12.

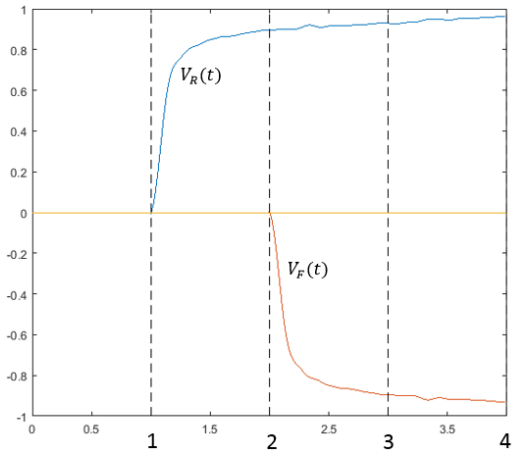


Figure 2.11: Rising edge response at 1ns and falling edge response at 2ns.

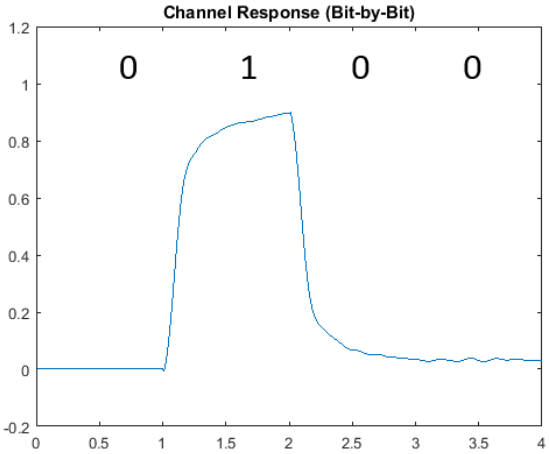


Figure 2.12: Channel response at 0100.

Another example of bit sequence 101001 is shown in Fig. 2.13. Adding $V_f(t-1)$ when seeing the first 10 bit sequence, adding $V_r(t-2)$ when seeing the first 01 bit sequence, adding $V_f(t-3)$ when seeing the second 10 bit sequence, and adding $V_r(t-4)$ when seeing the second 01 bit sequence.

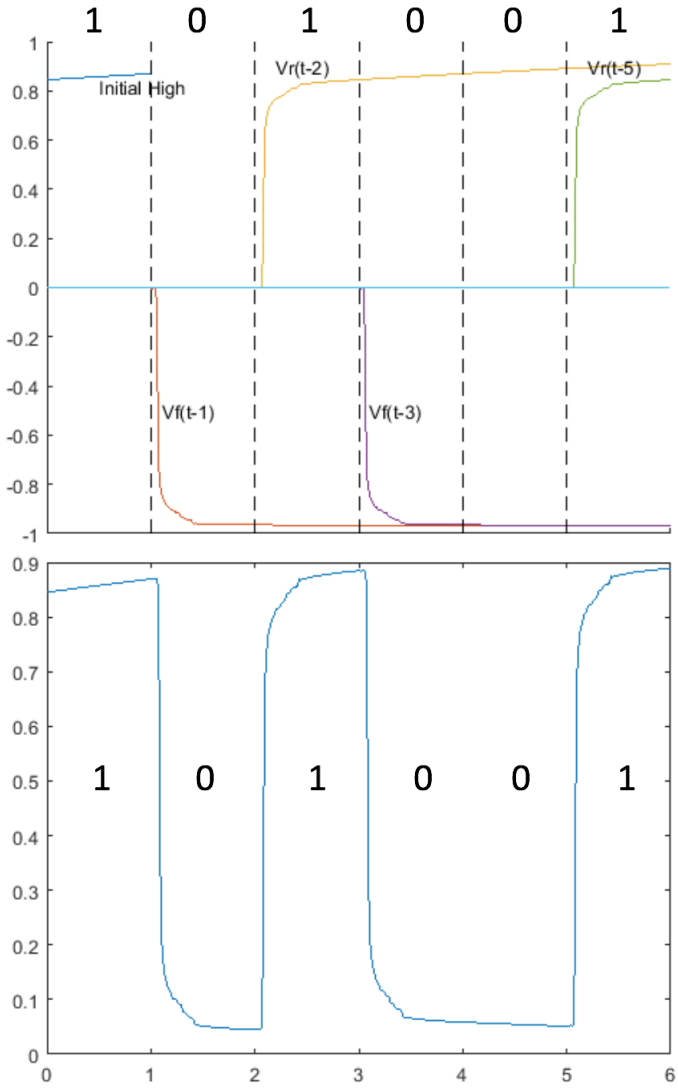


Figure 2.13: 101001 Example.

CHAPTER 3

JITTER EFFECT ON EYE DIAGRAM

Jitter is defined as the timing edges deviating from their ideal positions, an unwelcome phenomenon happening in all electrical systems [5]. Especially in the high speed link system, a small timing deviation might still be a significant portion of the signal interval because of the fast transition and short unit interval. Then the jitter-induced errors corrupt the signals and even the clock to fail the proper signal transmission. As a consequence, the tighter controllability of the jitter for the high speed link system is needed to prevent the signal failure from the non-ideality, and the deeper understanding of the jitter characteristics is vital for the high speed link system designer to meet the design requirements. In this chapter, jitter classification and their effect on the eye diagram will be introduced.

3.1 Jitter Classification

The total jitter firstly can be classified into two catagories, deterministic jitter (DJ) and random jitter (RJ). The deterministic jitter is further separated into more types: periodic jitter (PJ), data-dependent jitter (DDJ) and duty-cycle dependent jitter (DCD). The hierarchy diagram of the jitter tree is shown in Fig .3.1.

3.2 Deterministic Jitter

Deterministic jitter is the jitter that is repeatable and predictable, being further subdivided in the following paragraphs, based on the characteristics of the jitter and the root causes.

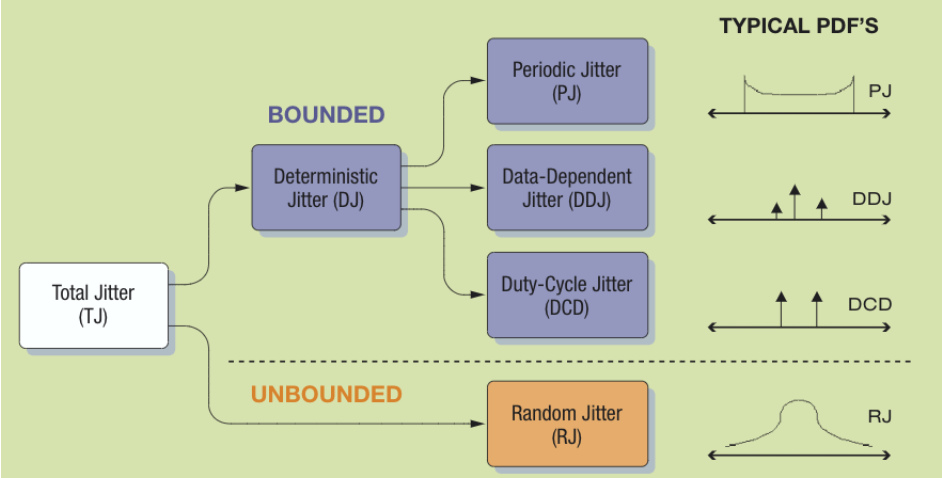


Figure 3.1: Jitter hierarchy.

3.2.1 Periodic Jitter

Jitter that repeats in a sinusoidal fashion is called periodic jitter or sinusoidal jitter [6]. Typically, the sinusoidal form, Eqn. 3.1 is used to define the periodic jitter. ω is the angular frequency, A is the amplitude and ϕ_0 is the initial phase.

$$PJ(t) = Acos(\omega t + \phi_0) \tag{3.1}$$

As shown in Fig. 3.2, the periodic jitter is in a sinusoidal shape, adding to the original signal to produce the jittered-signal by amount of timing shift based on the amplitude of the sinusoidal wave. By convention, periodic jitter is uncorrelated to the repeated data pattern but is normally related to the external sources. The jitter correlated to the repeated data is discussed in the next section. External deterministic noise sources such as switching power supply noise and strong RF carrier can lead to the periodic jitter.

An eye diagram with 5GHz, 0.2ns UI, 0.1ns rising and falling time for a pure signal is shown in Fig. 3.3. The eye is widely open without any distortion and jitter.

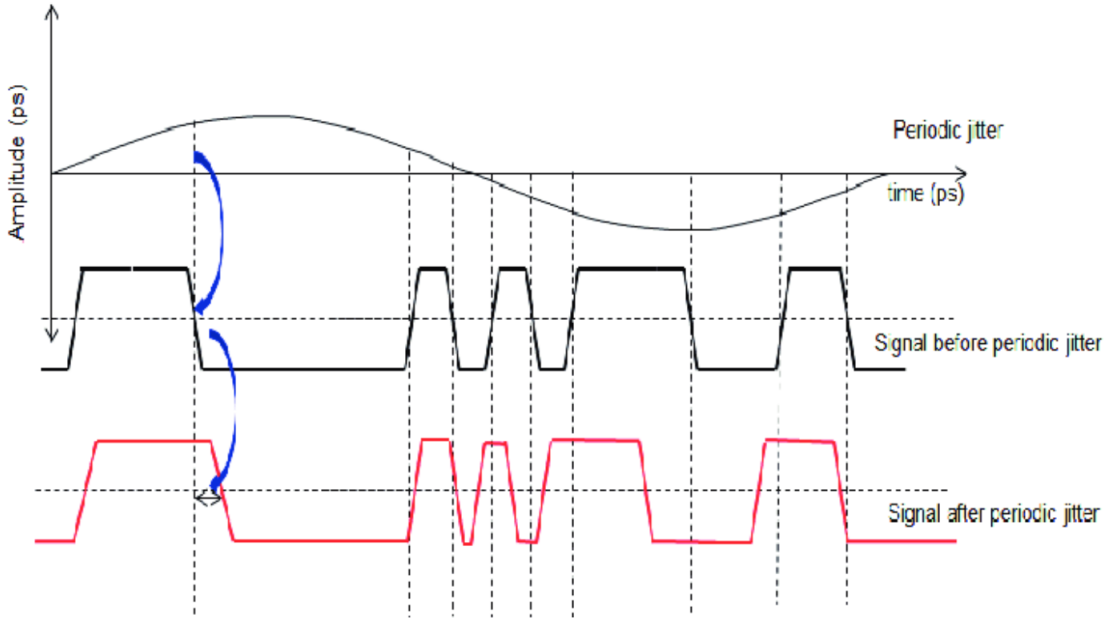


Figure 3.2: Periodic jitter added to signal.

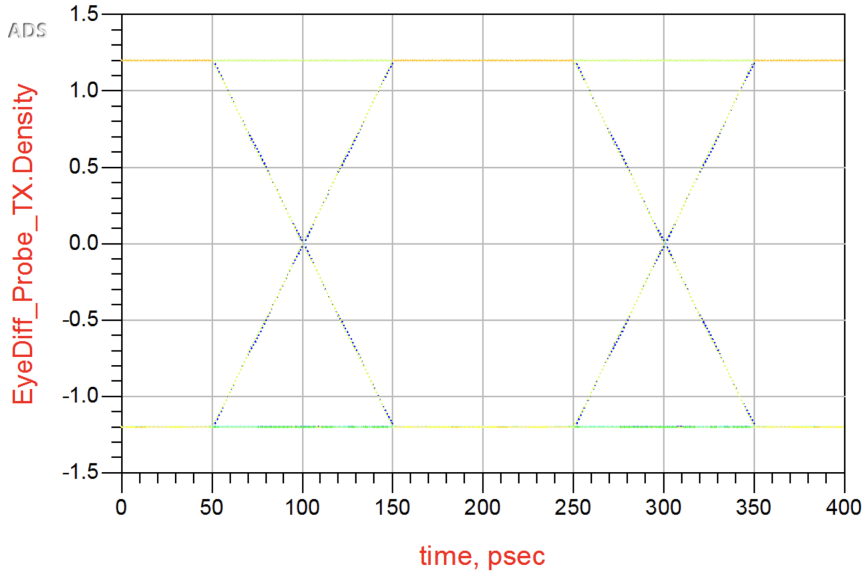


Figure 3.3: Eye diagram with 5GHz, 0.2ns UI, 0.1ns rising and falling time.

Applying a periodic jitter with amplitude 0.04ns (0.2UI) and frequency 2.4GHz to this original signal, the new eye diagram is shown in Fig. 3.4. The eye width is dramatically shrunk to about the half size of previous eye opening but the eye height is kept.

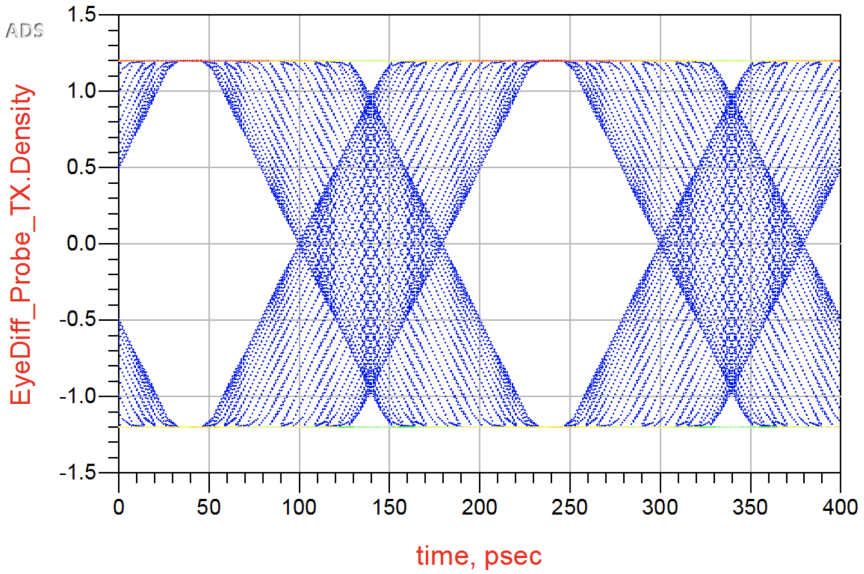


Figure 3.4: Eye diagram with 0.2UI and 2.4GHz periodic jitter.

3.2.2 Data-Dependent Jitter

Jitter that is correlated to the bit sequence of the data stream is called data-dependent jitter (DDJ). In an LTI system, data-dependent jitter is easy to model as the ideal data pattern is the input to the LTI system. Data-dependent jitter is measured from the output waveform as the timing deviation of the transition edges from the ideal transition edges. The maximum difference among those edges timing deviation $\Delta_{t1}, \Delta_{t2}...\Delta_{tn}$ defines the peak-to-peak value of the data-dependent jitter. Fig. 3.5 shows data-dependent jitter estimation through the LTI system.

From the discussion about LTI system in chapter 1, $V_o(t) = V_i(t) * h(t)$. Since the DDJ is the element measured from the output, the causes of DDJ can be traced back to the input $V_i(t)$ and the impulse response $h(t)$. As we know, the impulse response represents the characteristic of the channel. If the output signal is exactly the same as the input waveform, the lossless channel with unlimited bandwidth is required and then $V_o(t) = V_i(t)$ with zero DDJ.

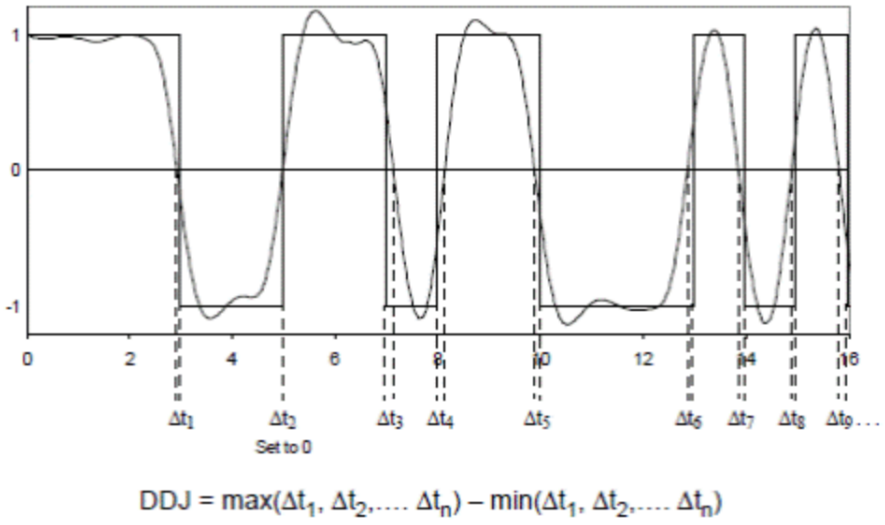


Figure 3.5: Data-dependent jitter.

However, the bandlimited channel leads to the slow transition from zero-to-one or one-to-zero and generates the timing deviation at edges. Another cause is the input bit sequence itself. The higher the bit rate, the switching between zero and one happens much frequently and rapidly that pushes the channel to response faster. The researcher J. Buckwalter [7] unified these two factors and derived the analytic format of the DDJ for the first order system as shown below:

$$t_{DDJ} = \frac{\tau}{2} \ln \frac{1+\alpha}{1-\alpha+\alpha^2} \tag{3.2}$$

α represents $e^{-T/\tau}$ where $\tau = RC$ in the first order low pass system and its inverse $\frac{1}{\tau}$ represents the cur-off frequency of the system or the bandwidth. T is the bit transmission time, then $\frac{1}{T}$ is the bit rate.

3.2.3 Duty-Cycle Dependent Jitter

Jitter that is associated with a rising or falling edge and measured from the mean deviation from the ideal is called duty-cycle dependent jitter (DCD) [8]. There are two common causes of DCD:

- The asymmetrical rising edges differ from its falling edges.
- The threshold offset for a waveform is higher or lower than it should.

The corresponding two causes are shown in the Fig. 3.6.

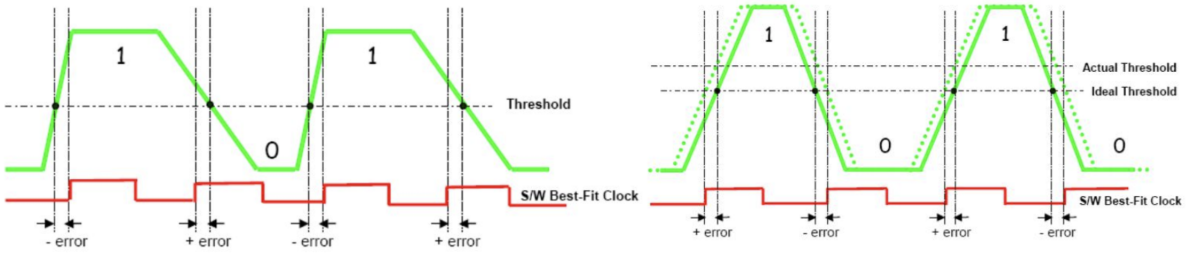


Figure 3.6: Duty-cycle jitter due to asymmetrical edges and threshold offset.

When applying 0.2UI DCD jitter into signal, the eye diagrams of this change before and after channel are plotted in Fig. 3.8. The left eye diagram is the input PRBS with 0.2UI DCD jitter. Originally, the zero-crossing point is at 100 psec and 0 V, but now it shifts to 120 psec and about 0.5 V. For the eye opening after the channel, 0.2UI DCD jitter slightly reduces the opening.

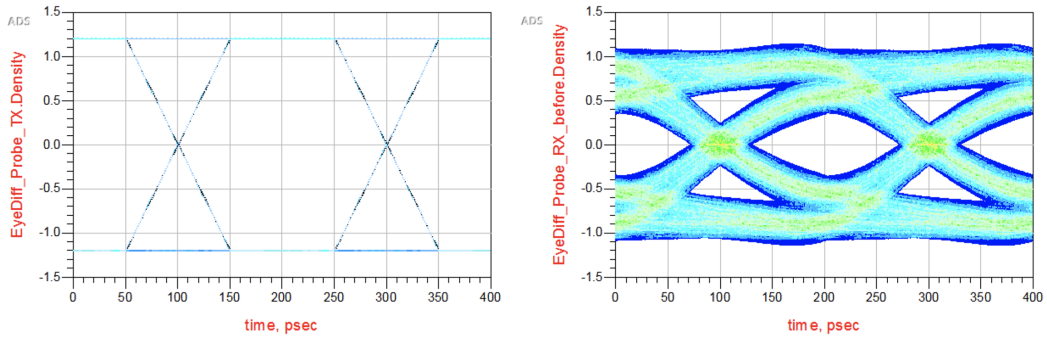


Figure 3.7: Eye diagrams before and after channel without jitter.

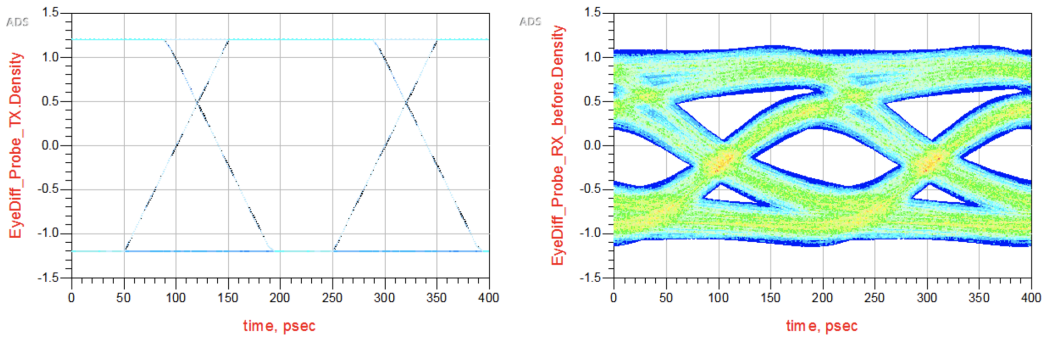


Figure 3.8: Eye diagrams before and after channel with 0.2UI DCD jitter.

While increasing DCD jitter to 0.5UI, the zero-crossing point disappears and the eye no longer exists, shown in Fig. 3.9. This is because the level-one bit width decreases from 100 psec to 0 psec.

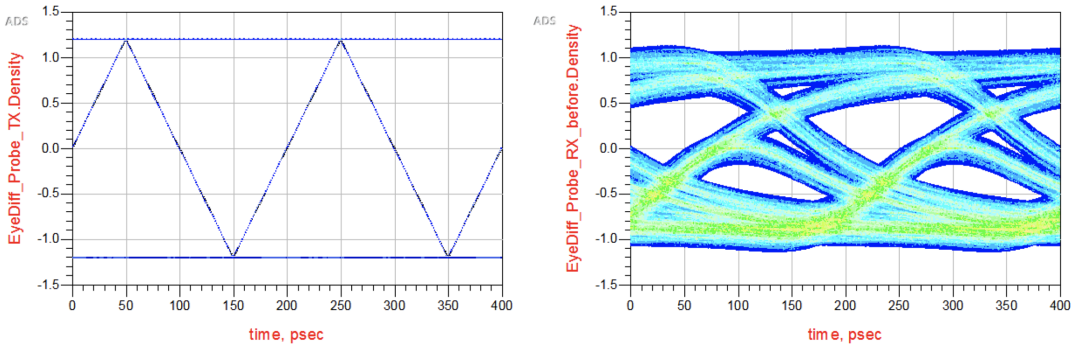


Figure 3.9: Eye diagrams before and after channel with 0.5UI DCD jitter.

3.3 Random Jitter

Unlike the deterministic jitter, random jitter is an unpredictable jitter and caused by the unbounded jitter sources. Theoretically, a random process can have any kind of distribution, but the random jitter normally has a Gaussian distribution model because the sources of these types of jitter are thermal noise, 1/f flicker noise or shot noise, where it fits into a bell curve. The Gaussian random jitter model is defined by Eqn. 3.3.

$$PDF_{RJ}(\Delta t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(\Delta t-\mu)^2}{2\sigma^2}} \tag{3.3}$$

This function is characterized as unbounded because its PDF tail approaches zero until the jitter variable Δt approaches infinity at both ends. The means of the Gaussian function is μ and its standard deviation is σ, where are two parameters to decide the random jitter. Normally, the mean μ is assumed to be 0 so left only one parameter to tune. The effect of σ on eye diagrams is shown below in Fig. 3.10 and Fig. 3.11. The larger the σ, the smaller the eye opening would be.

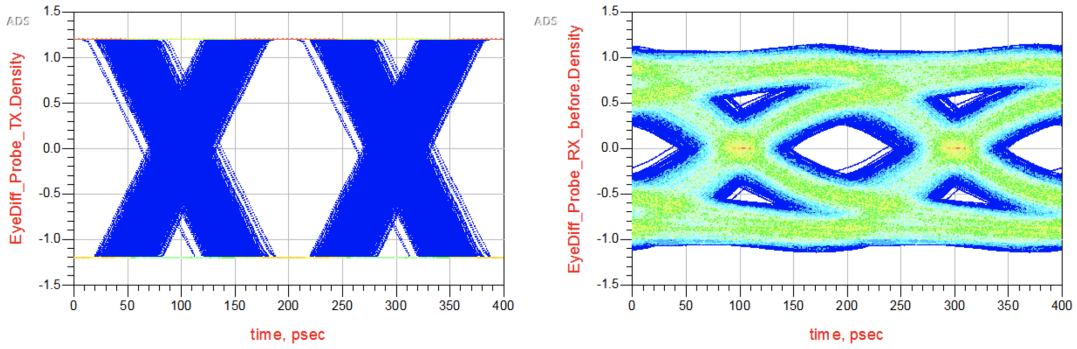


Figure 3.10: Eye diagrams before and after channel with σ=0.05UI random jitter.

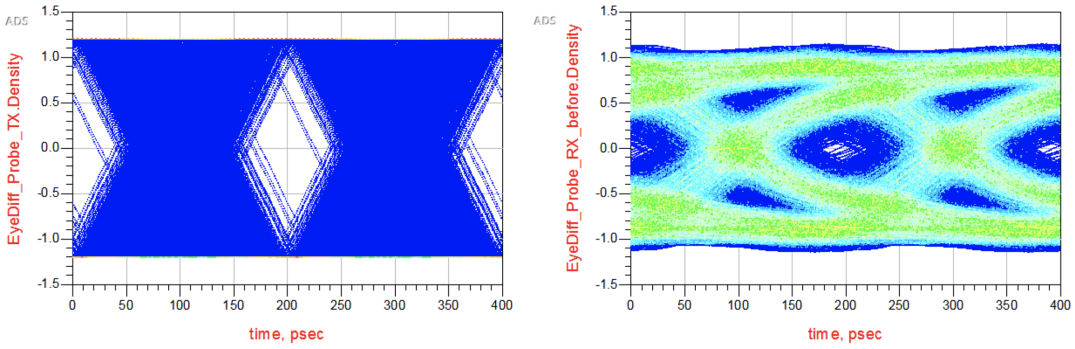


Figure 3.11: Eye diagrams before and after channel with σ=0.1UI random jitter.

CHAPTER 4

EQUALIZATION EFFECT ON EYE DIAGRAM

In chapter 2, a distorted eye has always been generated due to the non-ideal characteristic of the transmission line, such as crosstalk and losses. When increasing the signal speed to higher Gbps, the more significant impact will be seen as the eye is approaching to close, leaving both time and voltage margin degraded. The low-pass nature of the transmission line leads to the distortion. In chapter 3, various jitters that can happen in the transmitter front end, receiver end and interconnect during the transmission, has been discussed. However, signal integrity and timing issues can be reduced by the equalization, a circuit technique to compensate for these non-ideal effects. In this chapter, different types of equalizer will be introduced and how they overcome the signal integrity issue will be discussed.

4.1 Interconnect

Before heading into the detail of equalizers, some properties of the interconnect need to be addressed first. In chapter 2, channel impulse response is used to characterise the channel system in time domain, nevertheless signal integrity engineers are more familiar with the channel in frequency domain or the transfer function. As seen from the channel in Fig. 4.1, the amplitude is declining while the frequency approaches 330 MHz. This channel behaves the same as a low pass filter at cut-off frequency 330 MHz. The ideal channel passes signals from transmitter to receiver without distortion and its transfer function should be constant along all frequencies. So the basic idea of equalization is to recover the low-pass channel to a flat amplitude channel by boosting the high frequency attenuation parts. This can be expressed mathematically as: $H_{eq}(f)$. The transfer function of ideal equalizer is inverse of the channel transfer function so becoming a high pass filter.

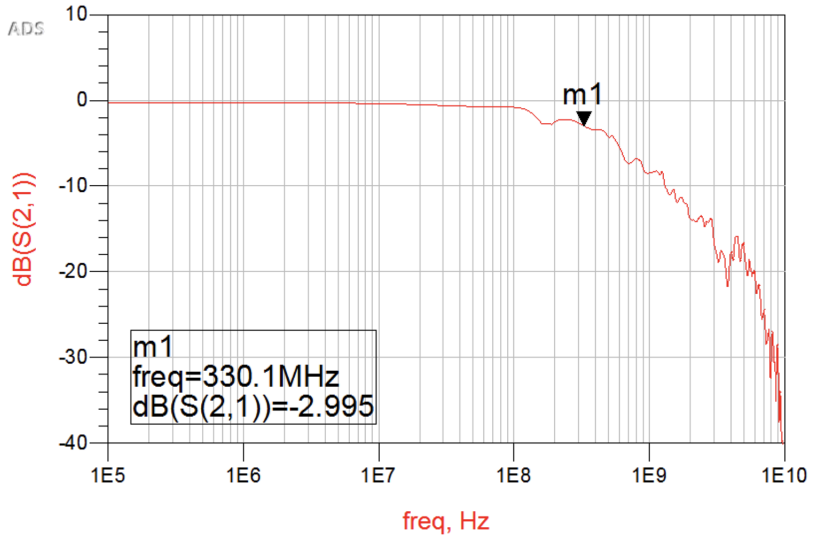


Figure 4.1: Low pass filter channel.

4.2 Transmitter Equalization

4.2.1 Pre-emphasis FIR Equalizer

The channel equalization can be placed at either transmitter side or receiver side. One type of transmitter equalization technique is called transmitter pre-emphasis, which is based on the architecture of a finite impulse response (FIR) filter. Before entering the channel transmission, the signal is "pre-distorted" in the favor of boosting the high frequency transitions relative to low frequency parts to compensate for the channel loss at high frequency. In the frequency perspective, the high-pass filtering effect applies to the signal. In the time domain, the high-frequency content happens during the rapid transition changes between bits, such as sudden rise and fall 010 in the pattern 00010111 after a series of constant bits. Vice versa, the low-frequency content in time domain represents in consecutive 0s or 1s that no change is made. Fig. 4.2 shows an example of signal after transmitter pre-emphasis, where the edges have significantly increased amplitude than the constant portion, corresponding to the high frequency boosting.

In order to achieve this boosting effect, the transmitter pre-emphasis is implemented by a multi-taps FIR filter (Fig. 4.3), which input propagates through the unit delay, is multiplied by the filter tap coefficient and then summed to the output. The taps before current time are pre-cursor taps

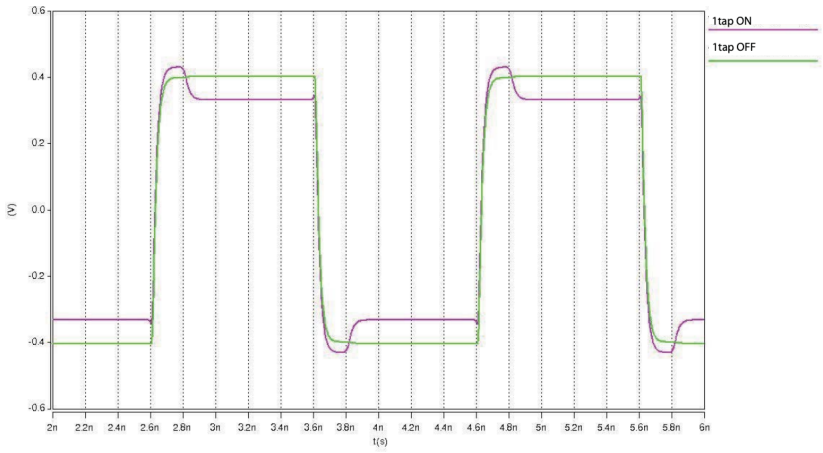


Figure 4.2: Pre-amphasis on and off.

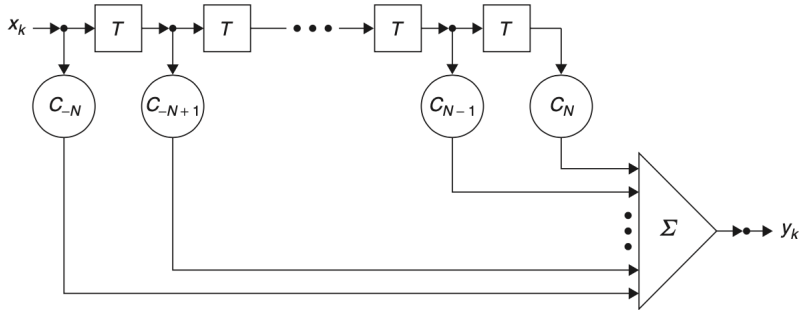


Figure 4.3: Finite impulse resposne filter (FIR).

and the taps after are called post-cursor taps. For a single post-cursor tap case, shown in Fig. 4.4, the original signal after lossy channel has a long tail extending to adjacent intervals, which refers to inter-symbol interference (ISI). Applying one unit interval delay and inversion with a proper weight to the original signal to obtain a new weighted compensation signal. Then, the summation of these two signals shrinks the extension or tail, thereby reducing the ISI and adjacent amplitude of nearby intervals [9].

Typically, the FIR filter uses one pre-cursor and two post-cursors to perform transmitter pre-emphasis. The pre-cursor taps are used to compensate for dispersion related phase distortion. Normally one tap is enough. The post-cursor taps counteract the ISI caused by the amplitude distortion, where the desired number of taps depends on the channel quality. Usually, two post-cursor taps are sufficient.

As you can see, the FIR filter based equalization technique achieves the

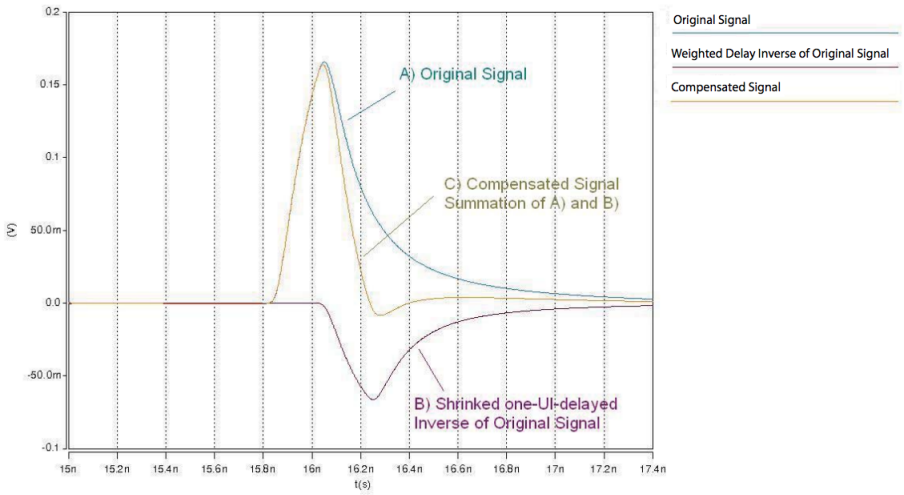


Figure 4.4: ISI compensation with pre-emphasis.

channel equalization by amplifying the high frequency contents of the signal beforehand in a time perspective, unlike CTLE that provides a high pass filter directly to the channel. Although the goal of these two methods is to ensure relative same loss at both low frequency and high frequency, CTLE views the system in a frequency domain and performs a high pass filtering effect to the low pass channel. FIR filter equalization manipulates or "pre-emphasis" the signal, either before or after channel, to relieve the channel loss at the high frequency, where the equalization is done in a time domain.

4.3 Receiver Equalization

4.3.1 Continuous-Time Linear Equalizer

As stated previously, the channel will attenuate the signal more in higher frequencies than lower frequencies. The continuous-time linear equalizer (CTLE) operates in a linear analogy system to counteract this low-pass effect of the channel by attenuating the low frequency parts and amplifying from Nyquist frequency to higher frequencies at the receiver end. The combination of channel and CTLE will bring the signal to a similar amplitude level till the required higher frequency state. For instance, the channel-only signal starts to drop at 0.33GHz, but with the help of CTLE the signal will not attenuate

until 2.9GHz. A constant and wider signal response level is built to reduce inter-symbol interference (ISI) and improve eye-diagram performance. The Fig. 4.5 simply shows this behavior.

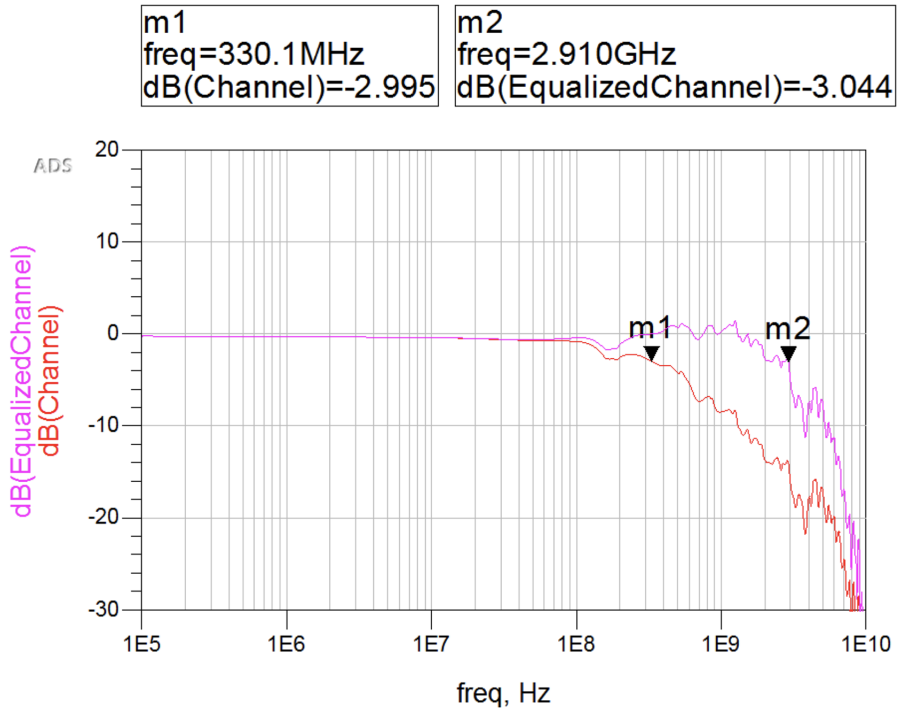


Figure 4.5: CTLE flats the channel amplitude.

CTLE is normally modeled by a two-pole and one-zero transfer function (Eqn. 4.1). Depending on the property of the channel and the design requirements, the placements of poles and zero are selected accordingly. Ideally the zero and the first pole should be placed closely for a good CTLE performance. The zero location determines the position where the boosting starts. The first and second poles affect the frequency location where the peak happens and normally making the midpoint of two poles to be the Nyquist frequency is preferable.

$$H(f) = \frac{GP_1P_2}{Z_1}\frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)} \tag{4.1}$$

If the required bit rate is 5 Gbps, then the Nyquist frequency needs to be 2.5GHz. Three examples of targeting at 2.5GHz Nyquist frequency with different boosting levels are shown below.

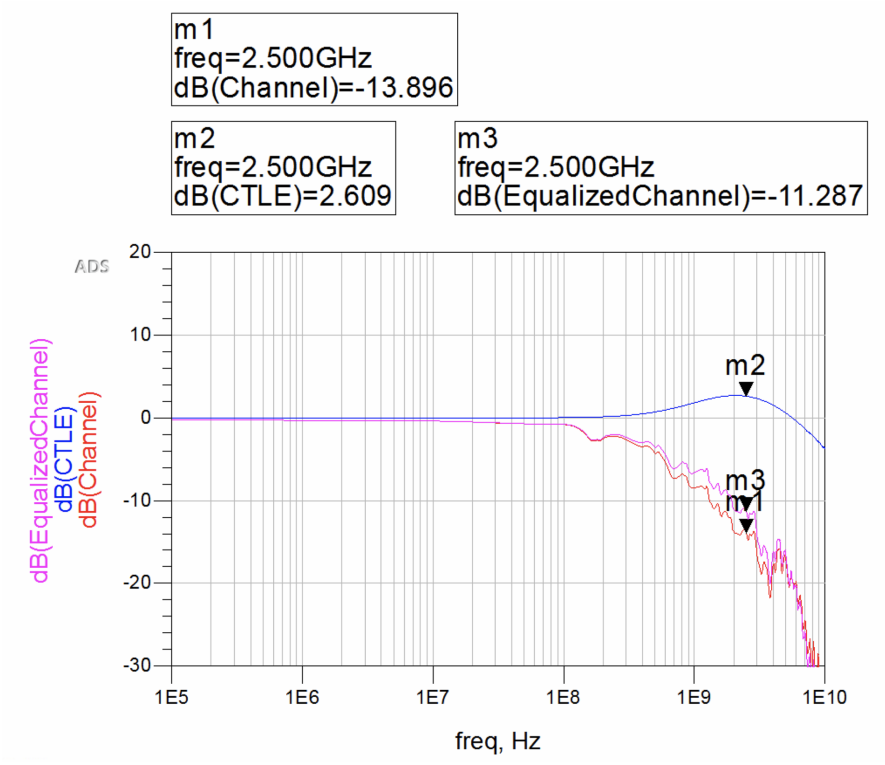


Figure 4.6: CTLE with 2.6dB gain at 2.5GHz.

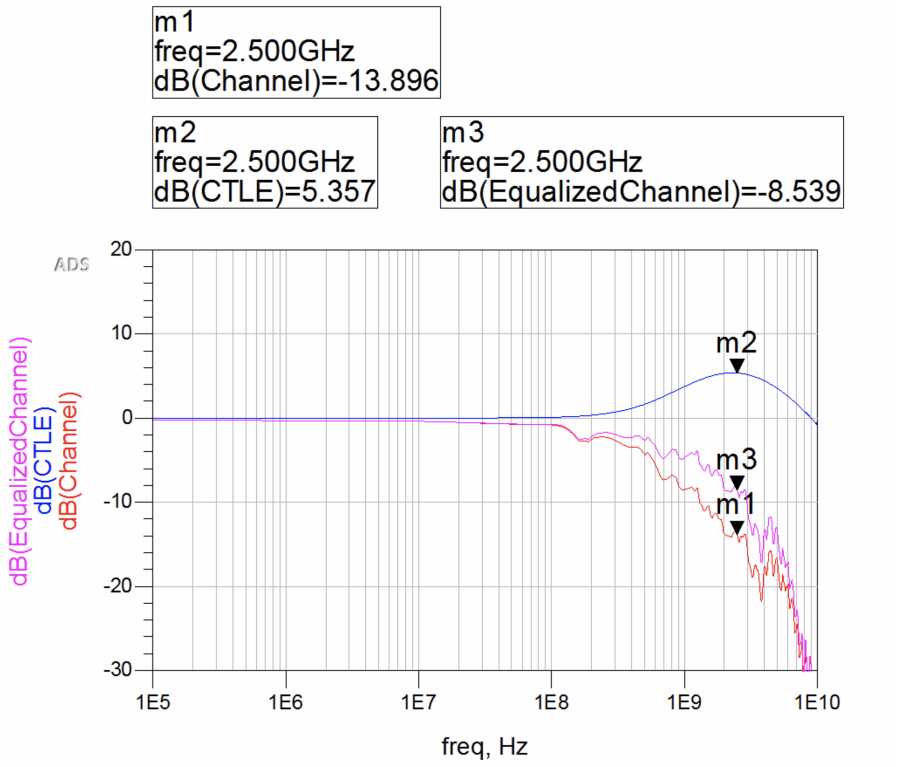


Figure 4.7: CTLE with 5.4dB gain at 2.5GHz.

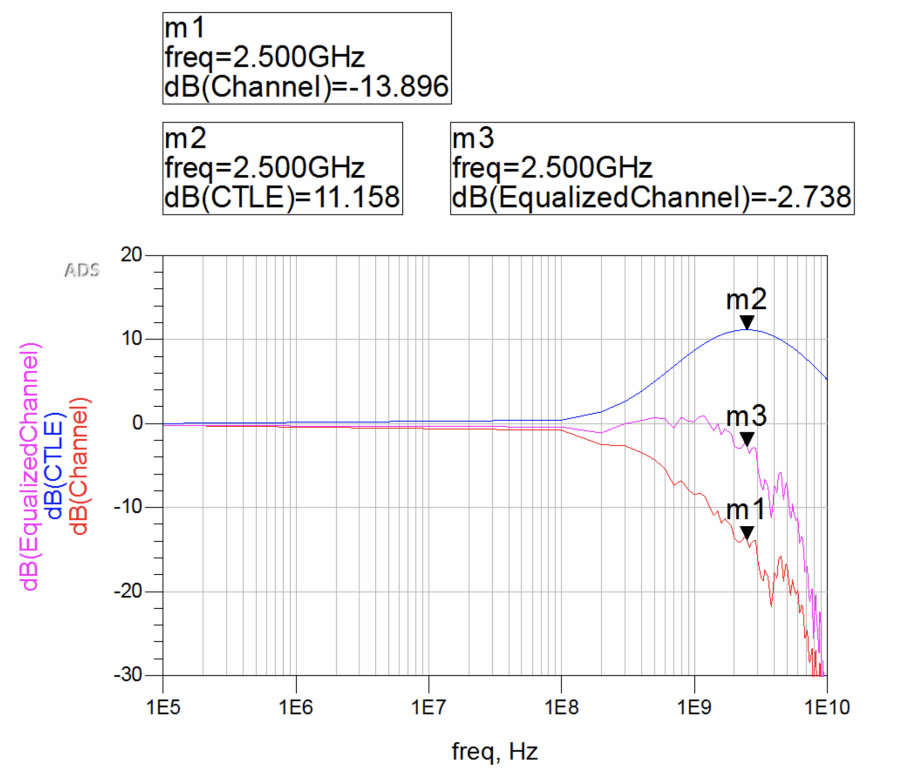


Figure 4.8: CTLE with 11.2dB gain at 2.5GHz.

Different gains are decided by choosing different pole-zero values as shown in Table 4.1. The first pole is set to be $10^{0.2} \approx 1.58$ GHz and the second pole is chose to be $10^{0.6} \approx 3.98$ GHz, where leading to the center point as 2.78 GHz that is close to the required 2.5GHz. Then, the placement of zero is used to tune the gain accordingly.

Table 4.1: Pole-zero positions for different gain

Gain (dB)	G	$P_1(2 \times 10^9\pi)$	$P_2(2 \times 10^9\pi)$	$Z_1(2 \times 10^9\pi)$
2.6	1	$10^{0.2}$	$10^{0.6}$	$10^{-0.05}$
5.4	1	$10^{0.2}$	$10^{0.6}$	$10^{-0.2}$
11.2	1	$10^{0.2}$	$10^{0.6}$	$10^{-0.5}$

The following plots, Fig. 4.9, Fig. 4.10 and Fig. 4.11, are the eye diagram comparison of the signal after channel and the signal after the channel with CTLE case.

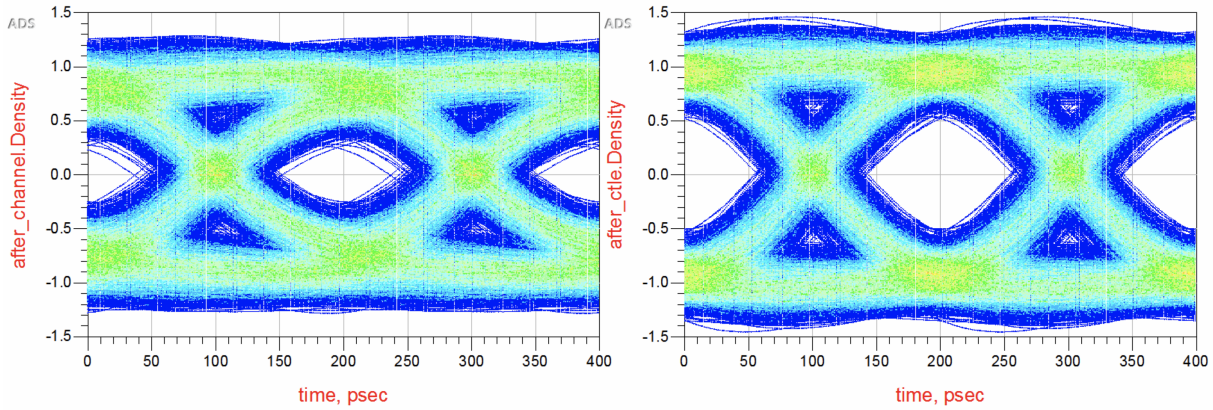


Figure 4.9: Eye diagram after channel and channel+CTLE with 2.6dB gain.

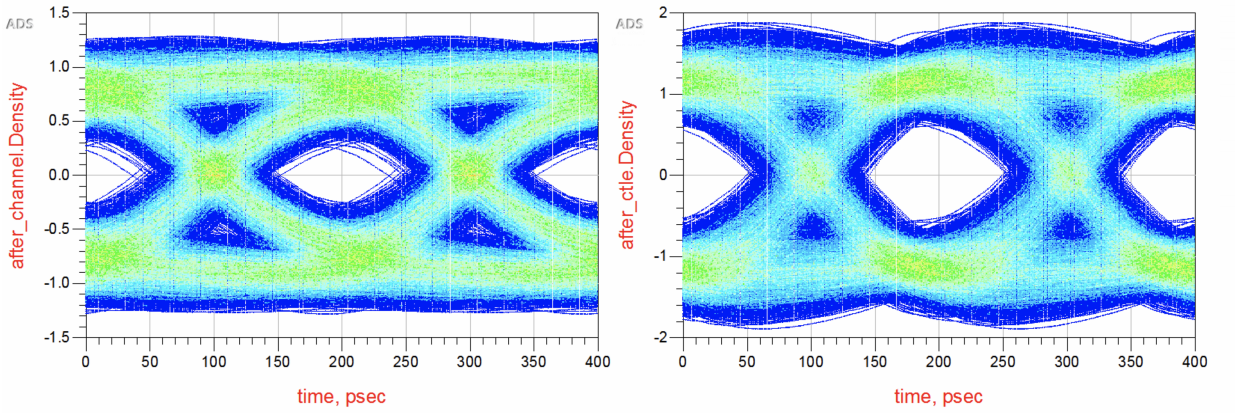


Figure 4.10: Eye diagram after channel and channel+CTLE with 5.4dB gain.

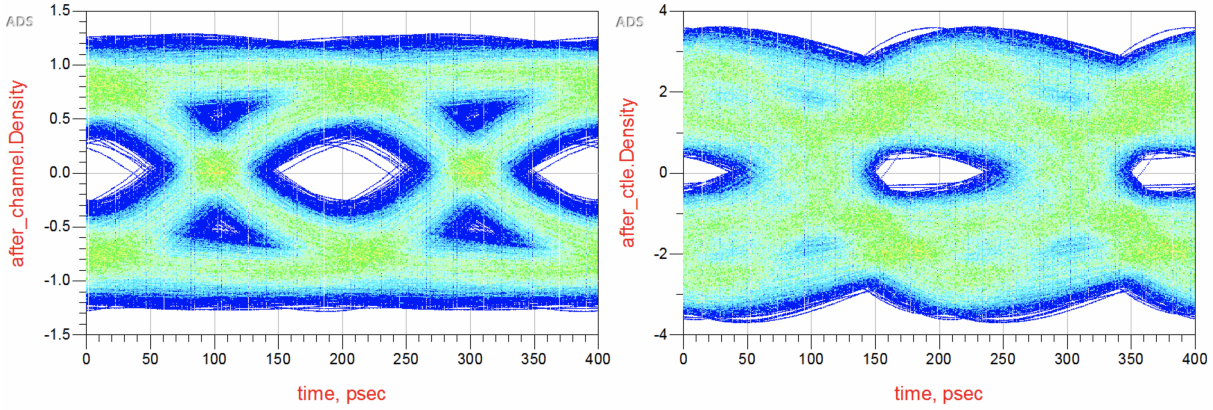


Figure 4.11: Eye diagram after channel and channel+CTLE with 11.2dB gain.

The Table 4.2 illustrates the values of the eye width and the eye height in different CTLE.

Table 4.2: Comparison of the eye opening

CTLE Gain (dB)	Eye Width (psec)	Eye Height (V)
0	99	0.441
2.6	118	1.019
5.4	125	1.101
11.2	99	0.373

4.3.2 Feed-Forward Equalizer

FFE is the equalization at the receiver end that has exactly the same architecture of transmitter pre-emphasis by FIR filter. The main purpose of FFE is to reduce the amplitude of the pre-cursor and normally it accompanies with the DFE to deliver the best equalization effect. The following plots, Fig. 4.12, Fig. 4.13 and Fig. 4.14, are the eye diagram comparison of the signal after channel and the signal after the channel with FFE case.

Table 4.3: Comparison of the eye opening

FFE Taps	Eye Width (psec)	Eye Height (V)
0 pre-tap + 0 post-tap	103	0.283
1 pre-tap + 1 post-tap	104	0.306
1 pre-tap + 2 post-tap	134	0.745
1 pre-tap + 3 post-tap	134	0.739

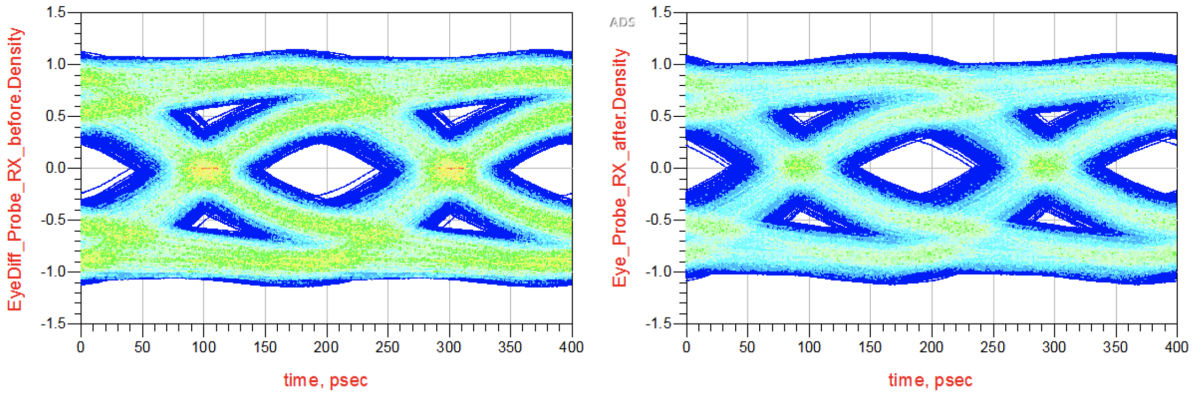


Figure 4.12: Eye diagram after channel and channel + 1 pre-tap and 1 post-tap FFE.

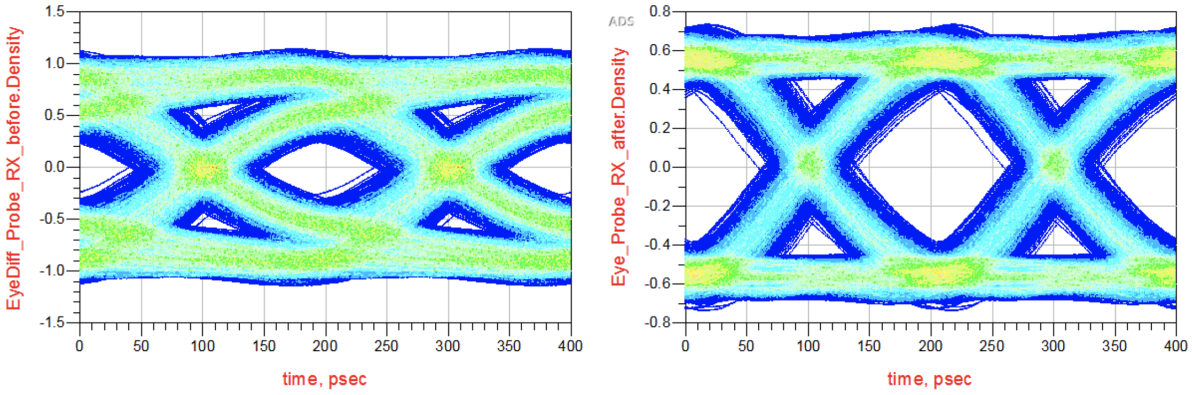


Figure 4.13: Eye diagram after channel and channel + 1 pre-tap and 2 post-tap FFE.

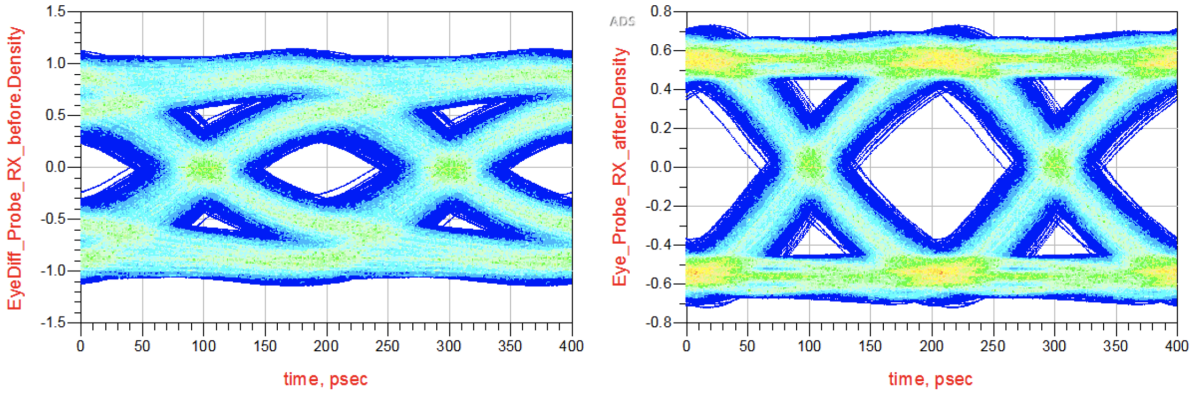


Figure 4.14: Eye diagram after channel and channel + 1 pre-tap and 3 post-tap FFE.

4.3.3 Decision Feedback Equalization

In fact, the linear equalization discussed previously intends to create an inverse transfer function of the channel to balance the strong attenuation at certain high frequency regions, which in terms of higher gain in that same band. Since the linear equalizer does not distinguish the noise and signal, both noise and signal represented in the high frequency band are filtered or enhanced. The performance of the linear equalization alone might not be superior, so the decision feedback equalization is there to mitigate the noise.

A decision feedback equalization (DFE) is a filter that uses the feedback of detected symbols to remove the ISI from the input to estimate the output. The completed block diagram of the receiver equalization consists of a linear equalizer, a slicer (symbol detector) and a DFE [10]. The DFE itself actually is a FIR filter. The input to the DFE is a series of logic 0 or 1 decisions from previously detected symbols. Similar to FIR filter, each decision will be weighted accordingly and then summed to be the DFE output in Fig. 4.15

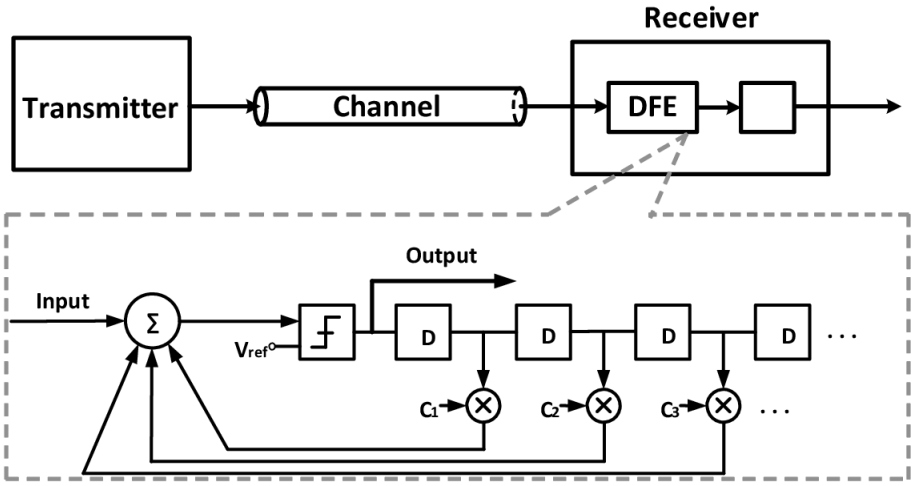


Figure 4.15: Block diagram of DFE.

In DFE, depending on the size of ISI at post-cursor location, the number of post-cursors required is different. Logically, the larger the ISI propagates, more post-cursors will be needed to relief the ISI effect. The following plots, Fig. 4.16, Fig. 4.17 and Fig. 4.18, are the eye diagram comparison of the signal after channel and the signal after the channel with DFE case.

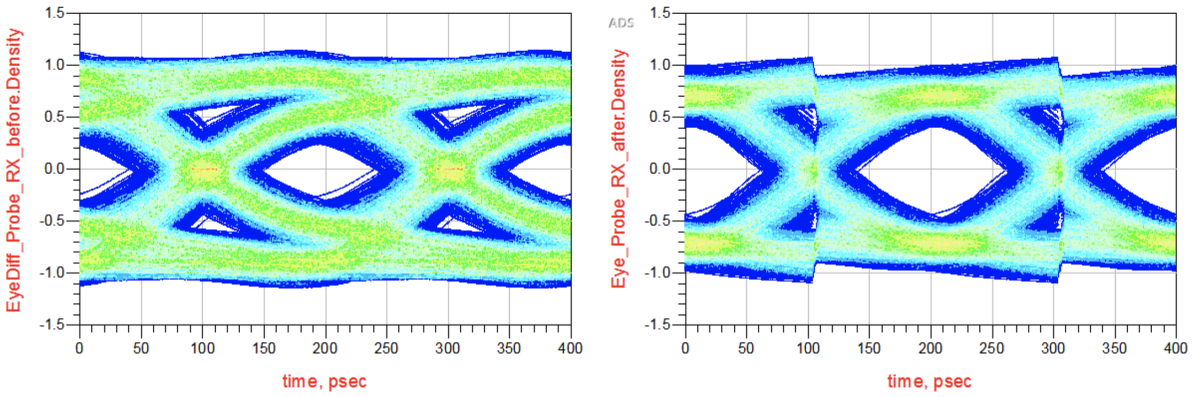


Figure 4.16: Eye diagram after channel and channel + 1 post-tap DFE.

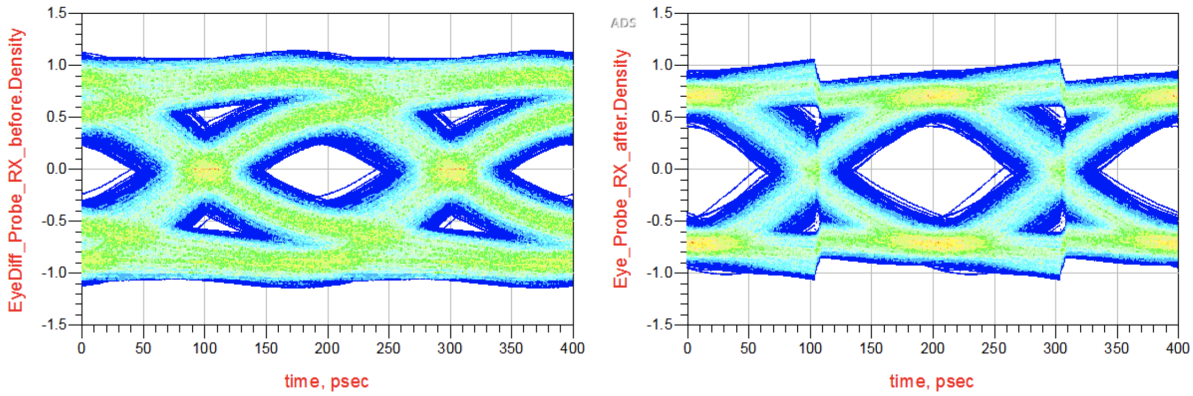


Figure 4.17: Eye diagram after channel and channel + 2 post-tap DFE.

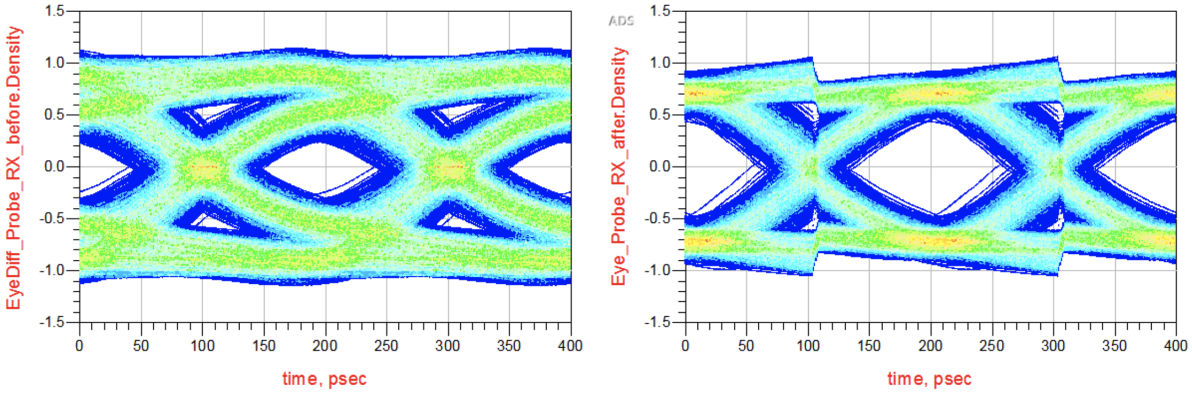


Figure 4.18: Eye diagram after channel and channel + 3 post-tap DFE.

As expected, under the help of DFE, the eye opening region is much larger than the original eye. Only 1 post-tap is sufficient to open the eye properly. Although the second or the third post-tap can still make the eye opening, the eye size change is not as obvious as the change jumped from non-equalized eye to 1 post-tap DFE eye.

Table 4.4: Comparison of the eye opening

DFE Taps	Eye Width (psec)	Eye Height (V)
0 post-tap	103	0.283
1 post-tap	133	0.841
2 post-tap	137	0.929
3 post-tap	138	0.954

CHAPTER 5

CONCLUSION

REFERENCES

[1] M. P. Li, M. Shimanouchi, and H. Wu, "Advancements in high-speed link modeling and simulation (an invited paper for cicc 2013)," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, 2013, pp. 1–8.

[2] I. Hajj, *Computational Methods In Circuit Simulations*. Champaign, IL: CreateSpace Independent Publishing Platform, 2016.

[3] P. Hanumolu, G. Wei, and Y. Moon, "Equalizers for high-speed serial links," *International Journal of High Speed Electronics and Systems*, vol. 15, no. 2, pp. 429–458, 2005.

[4] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-speed Digital Designs*. Hoboken, NJ: John Wiley Sons, 2009.

[5] "Understanding and characterizing timing jitter," White Paper, Tektronix, 2003.

[6] Y. Chang and D. Oh, "System-level modeling and simulation of periodic jitter in high-speed links," in *19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems*, 2010, pp. 117–120.

[7] J. Buckwalter, B. Analui, and A. Hajimiri, "Predicting data-dependent jitter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 9, pp. 453–457, 2004.

[8] M. Marcu, S. Durbha, and S. Gupta, "Duty-cycle distortion and specifications for jitter test-signal generation," in *2008 IEEE International Symposium on Electromagnetic Compatibility*, 2008, pp. 1–4.

[9] "Understanding the pre-emphasis and linear equalization features in stratix iv gx devices," Application Note, Altera Corporation, 2010.

[10] C. Zhang, G. Jeon, Y. Choi, Y. Kim, and K. K. Kim, "An area efficient 4gb/s half-rate 3-tap dfe with current-integrating summer for data correction," in *2016 IEEE 25th North Atlantic Test Workshop (NATW)*, 2016, pp. 6–11.